Monday (August 28th)

#	Time	
*	08:00	**REGISTRATION STARTS**

Monday: Tutorial 1

#	Time	Title and Tutorialist
*	08:30	**EXPLOITING DYNAMIC AND PARTIAL RECONFIGURATION FOR FPGAS . TOOLFLOW, ARCHITECTURE AND SYSTEM INTEGRATION** **J. Becker, M. Hübner**, University of Karlsruhe - Germany

Monday: Tutorial 2

#	Time	Title and Tutorialist
*	14:00	**ROBUST LOW POWER COMPUTING IN THE NANOSCALE ERA** **Todd Austin**, University of Michigan - USA

Monday: Tutorial 3

#	Time	Title and Tutorialist
*	16:50	**FORMAL VERIFICATION FOR REAL-WORLD DESIGNS** **Valeria Bertacco**, University of Michigan - USA

Tuesday (August 29th)

#	Time	
*	08:00	**CONFERENCE OFFICIAL OPENING** Organizing committee

#	Time	Speaker
K1	08:50	**Reiner Hartenstein**, Kaiserslautern University of Technology - Germany

Tuesday: Invited Talk 1

#	Time	Title and Authors
*	11:40	**LOW MAINTENANCE VERIFICATION** **Valeria Bertacco**, University of Michigan - USA

Tuesday: Session 1: RECONFIGURABLE ARCHITECTURES

#	Time	Title and Authors
1.1	14:00	**REDEFIS - A SYSTEM WITH A REDEFINABLE INSTRUCTION SET** V. M. Goulart Ferreira, L. Gauthier, T. Kando, T. Matsuo, T. Hashinaga and K. Murakami
1.2	14:20	**ASYNCHRONOUS CIRCUITS DESIGN ON RECONFIGURABLE DEVICES** M. Renato, G. Sartori, R. Ribas and A. Reis
1.3	14:40	**FPGA ARCHITECTURE FOR OBJECT SEGMENTATION IN REAL TIME** J. Oliveira, A. Printes, R. Freire, E. Melcher and I. Silva
1.4	15:00	**IMPLEMENTATION OF DISPATCHING ALGORITHMS FOR ELEVATOR SYSTEMS USING RECONFIGURABLE ARCHITECTURES** D. M. Muñoz-Arboleda, C. H. Llanos, M. Ayala-Rincón and R. P. Almeida

Tuesday: Invited Talk 2

#	Time	Title and Authors
*	15:50	**RAZOR: A LOW-POWER PIPELINE BASED ON CIRCUIT-LEVEL TIMING SPECULATION** **Todd Austin**, University of Michigan - USA

Tuesday: Session 2: DYNAMIC RECONFIGURATION

#	Time	Title and Authors
2.1	16:50	**DYNAMIC TASK BINDING FOR HARDWARE/SOFTWARE RECONFIGURABLE NETWORKS** T. Streichert, C. Haubelt and J. Teich
2.2	17:10	**INFRASTRUCTURE FOR DYNAMIC RECONFIGURABLE SYSTEMS: CHOICES AND TRADE-OFFS** L. Möller, R. Soares, E. Carvalho, I. Grehs, N. Calazans and F. Moraes
2.3	17:30	**Mapping of Image Processing Systems to FPGA Computers based on Temporal Partitioning and Design Space Exploration** P. S. do Nascimento, M. E. de Lima, S. M. da Silva and J. L. Seixas

Wednesday (August 30th)

#	Time	Title and Speaker
K2	08:30	**BIOMIMETIC MEMS AND NEMS SENSING PLATFORMS-ICARUS REVISTED** **Marc Madou**, UC-Irvine - USA

#	Time	Title and Speaker
K3	10:10	**HIGH PERFORMANCE SILICON MEMS FOR NICHE MARKET APPLICATIONS** **Andres Lagos**, Colibrys Ltd. - Neuchâtel - Switzerland

Wednesday: Session 3: NETWORK ON CHIP

#	Time	Title and Authors
3.1	11:20	**DYNAMIC ROUTING ALGORITHM BASED ON ANT COLONY FOR MINIMIZING HOT SPOT IN NOC** M. Daneshtalab
3.2	11:40	**APPLICATION DRIVEN TRAFFIC MODELING FOR NOCS** L. Tedesco, A. Mello, L. Giacomet, N. Calazans and F. Moraes
3.3	12:00	**AREA AND PERFORMANCE OPTIMIZATION OF A GENERIC NETWORK-ON-CHIP ARCHITECTURE** M. Véstias and H. Neto

Wednesday: Session 4: LOW POWER AND ANALOG DESIGN

#	Time	Title and Authors
4.1	14:00	**AN ULTRA LOW-POWER CLASS-AB SINH INTEGRATOR** S. Haddad and W. Serdijn
4.2	14:20	**ULTRA LOW-VOLTAGE ULTRA LOW-POWER CMOS THRESHOLD VOLTAGE REFERENCE** L. Ferreira, T. Pimenta, R. Moreno and W. Noije
4.3	14:40	**A TEST CHIP FOR AUTOMATIC MOSFET MISMATCH CHARACTERIZATION** H. Klimach, M. Schneider and C. Galup-Montoro
4.4	15:00	**POWER CONSTRAINED DESIGN OPTIMIZATION OF ANALOG CIRCUITS BASED ON PHYSICAL GM/ID CHARACTERISTICS** A. Girardi and S. Bampi

Wednesday: Session 5: ANALOG AND MIXED SIGNAL DESIGN

#	Time	Title and Authors
5.1	15:50	**BIAS CIRCUIT DESIGN FOR LOW-VOLTAGE CASCODE TRANSISTORS** P. Aguirre and F. Silveira
5.2	16:10	**A DIFFERENTIAL SWITCHED-CAPACITOR AMPLIFIER WITH PROGRAMMABLE GAIN AND OUTPUT OFFSET VOLTAGE** F. Lacerda, S. Pietri and A. Olmos
5.3	16:30	**4GHZ CONTINUOUS-TIME BANDPASS DELTA-SIGMA MODULATOR FOR**

		DIRECTLY HIGH IF A/D CONVERSION A. Mariano, D. Dallet, Y. Deval and J.-B.Begueret
5.4	16:50	**HIGH SPEED RECEIVER AMPLIFIER DESIGN USING CURRENT FEEDBACK AMPLIFIER AND CURRENT CONVEYORS** G. Kaushik and D. Nagchoudhuri
5.5	17:10	**A GENERAL DOMAIN CMOS COMPANDING INTEGRATOR** A. Cunha and A. Niknejad

Thursday (August 31th)

Thursday: Session 6: MODELING, SYNTHESIS AND FORMAL VERIFICATION

#	Time	Title and Authors
6.1	08:30	**ENERGY AWARE MULTIPLE CLOCK DOMAIN SCHEDULING FOR A BIT-SERIAL, SELF-TIMED ARCHITECTURE** H. Giefers and A. Rettberg
6.2	08:50	**ASPECT-ORIENTED DESIGN IN SYSTEMC: IMPLEMENTATION AND APPLICATIONS** D. Deharbe and S. Q. de Medeiros
6.3	09:10	**SAEPTUM: VERIFICATION OF ELAN HARDWARE SPECIFICATIONS USING THE PROOF ASSISTANT PVS** M. Ayala-Rincón and T. M. Sant'Ana
6.4	09:30	**A FAST SAT SOLVER ALGORITHM BEST SUITED TO RECONFIGURABLE HARDWARE** R. Zuim, J. T. de Sousa and C. Coelho
6.5	09:50	**FAST DISJOINT TRANSISTOR NETWORKS FROM BDDS** L. Junior, F. Marques, T. Cardoso, R. Ribas and A. Reis

Thursday: Invited Talk 3

#	Time	Title and Authors
*	10:40	**ADAPTIVE EMBEDDED SYSTEMS: RUN-TIME RECONFIGURABLILITY AND OTHER FUTURE TRENDS** **J. Becker (IEEE Senior Member), M. Hübner (IEEE Student Member)**, University of Karlshure - Germany

Thursday: Session 7: EMBEDDED SYSTEMS

#	Time	Title and Authors
7.1	11:20	**MDA-BASED APPROACH FOR EMBEDDED SOFTWARE GENERATION FROM A UML/MOF REPOSITORY** F. do Nascimento, M. Oliveira, M. Wehrmeister, F. Wagner and C. E. Pereira
7.2	11:40	**HARDWARE SUPPORT IN A MIDDLEWARE FOR DISTRIBUTED AND REAL-TIME EMBEDDED APPLICATIONS** E. T. Silva Jr, F. Wagner, E. Freitas and C. E. Pereira
7.3	12:00	**ADVANTAGES OF JAVA PROCESSORS IN CACHE PERFOMANCE AND POWER FOR EMBEDDED APPLICATIONS** A. Beck, M. Rutzig and L. Carro

Thursday: Session 8: DIGITAL AND LOW POWER DESIGN

#	Time	Title and Authors
8.1	14:00	**EXPLOITING GENERAL COEFFICIENT REPRESENTATION FOR THE OPTIMAL SHARING OF PARTIAL PRODUCTS IN MCMS** E. Costa, P. Flores and J. Monteiro
8.2	14:20	**A CELL LIBRARY FOR LOW POWER HIGH PERFORMANCE CMOS VOLTAGE-MODE QUATERNARY LOGIC** R. Silva, H. Boudinov and L. Carro
8.3	14:40	**ON-LINE OPTIMIZATION OF FPGA POWER-DISSIPATION BY EXPLOITING RUN-TIME ADAPTION OF COMMUNICATION PRIMITIVES** K. Paulsson, M. Hübner and J. Becker
8.4	15:00	**BYZFAD: A LOW SWITCHING ACTIVITY ARCHITECTURE FOR SHIFT-AND-ADD MULTIPLIERS** M. Mottaghi, A. Kusha and Z. Navabi

#	Time	Title and Speaker
K4	15:50	**MODELING OF ADVANCED SEMICONDUCTOR DEVICES** **Siegfried Selberherr**, TU-Wien - Austria

Thursday: Session 9: TEST AND VERIFICATION

#	Time	Title and Authors
9.1	17:10	**SINGLE EVENT TRANSIENTS IN DYNAMIC LOGIC** G. Wirth, I. Ribeiro, M. Vieira and F. Kastensmidt
9.2	17:30	**CRYPTOGRAPHY CORE TOLERANT TO DFA FAULT ATTACKS** C. R. Moratelli, M. Lubaszewski and E. Cota
9.3	17:50	**DESIGN AT HIGH LEVEL OF A ROBUST 8-BIT MICROPROCESSOR TO**

		SOFT ERRORS BY USING ONLY STANDARD GATES R. Bastos, F. Kastensmidt and R. Reis
9.4	18:10	**EVALUATION OF SEU AND CROSSTALK EFFECTS IN NETWORK-ON-CHIP SWITCHES** A. Frantz, F. Kastensmidt, L. Carro and E. Cota
9.5	18:30	**USING A SOFTWARE TESTING TECHNIQUE TO IDENTIFY REGISTERS FOR PARTIAL SCAN IMPLEMENTATION** M. Krug, M. Moraes and M. Lubaszewski
9.6	18:50	**USING NEXUS COMPLIANT DEBUGGERS FOR REAL-TIME FAULT INJECTION ON MICROPROCESSORS** A. Fidalgo, M. Gericota, G. Alves and J. Ferreira

Friday (September 1st)

Friday: Session 10: PHYSICAL AND ANALOG DESIGN

#	Time	Title and Authors
10.1	10:40	**QUADRATIC PLACEMENT FOR 3D CIRCUITS USING Z-CELL SHIFTING, 3D ITERATIVE REFINEMENT AND SIMULATED ANNEALING** R. Hentschke, G. Flach, F. Pinto and R. Reis
10.2	11:10	**EFFECTS OF DIGITAL SWITCHING NOISE ON ANALOG VOLTAGE REFERENCES IN MIXED-SIGNAL CMOS ICS** D. Bonomi, G. Boselli, G. Trucco and V. Liberali
10.3	11:40	**A BAND-PASS GM-C FILTER DESIGN BASED ON GM/ID METHODOLOGY AND CHARACTERIZATION** F. Cortes, E. Fabris and S. Bampi

#	Time	
*	14:00	**PORTFOLIO**

#	Time	Title and Speaker
*	15:00	**CLOSURE SESSION** Organizing committee