ESCOLA POLITÉCNICA DA UNIVERSIDADE DE SÃO PAULO
Engenharia de Sistemas Eletrônicos – PSI
Av. Prof. Luciano Gualberto, travessa 3, no. 158
Cidade Universitária – São Paulo – CEP: 05508-900
Telefone: (11) 3091-5668 Fax: (11) 3091-5664

IEEE SOLID-STATE CIRCUITS SOCIETY
445 Hoes Lane, Piscataway
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CALL FOR PARTICIPATION – IEEE SSCS DL TOUR

THE IEEE SOLID-STATE CIRCUITS SOCIETY INVITES YOU TO PARTICIPATE AT FIFTH DISTINGUISHED LECTURER TOUR IN SOUTH AMERICA (IEEE REGION 9). IT WILL BE HOSTED BY **SOUTH BRAZIL AND MONTEVIDEO SSCS** CHAPTERS.

1ST DAY: in SÃO PAULO

DATE: OCTOBER 5TH, 2010

LOCAL: ANFITEATRO – ENGENHARIA ELÉTRICA DA ESCOLA POLITÉCNICA DA UNIVERSIDADE DE SÃO PAULO

Av. Prof. Luciano Gualberto, 158, trav.3, Cidade Universitária, São Paulo

Program:

9:00h Open Session: participation of Prof. Dr. José Roberto Cardoso, Director of Escola Politécnica da USP, and Eng. Alessio Bento Borelli, President of IEEE South Brazil

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9:10h - 1st Invited Distinguished Lecturer
Dr. **David Kuochieh Su** - Atheros Communications, Santa Clara, CA/USA

Talk on: Challenges in designing CMOS wireless System-on-a-chip

10:30 – 10:50 Coffee break

10:50 – 12:10 - 2nd Invited Distinguished Lecturer
Dr. **Stefan Rusu** - Intel Corporation, Santa Clara, CA/USA
Talk on: Microprocessor Design in the Nanoscale Era

12:10 – 14:00 Lunch
14:00 – 15:20 - 3rd Invited Distinguished Lecturer
Prof. Dr. **Franco Maloberti** - University of Pavia, Pavia, Italy

Talk on: **Power Efficient Data Converters**

15:20 – 15:40 - Coffee break
15:40 – 17:00 - 4rd Invited Distinguished Lecturer
Dr. **Ekanayake Ajith Amerasekera**, Kilby Research Labs, Texas Instrument Inc. Dallas, Texas, USA
Talk on: Ultra Low Power Electronics in the Next Decade

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17:00 Closing session

Responsible:
PROF. DR. **WILHELMUS A.M. VAN NOIJE**
IEEE SSCS Chair – South Brazil
FULL PROFESSOR - ESCOLA POLITÉCNICA DA USP
Email: noije@lsi.usp.br

Contato: Sra. Silvana – email: Silvana@lsi.usp.br, tel. +11-30915589

Vamos transmitir via internet por um site IP-TV, e esperamos que tenha qualidade apreciável. Segue o link onde será transmitido o vídeo: http://pt-br.justin.tv/a/sitco#/w/424310736

2nd DAY: MONTEVIDEO, URUGUAY ON OCTOBER 7TH, 2010
RESPONSIBLE: PROF. FERNANDO SILVEIRA – IEEE SSCS Member, URUGUAY
Email: silveira@fing.edu.uy
More info at http://iie.fing.edu.uy/eamta2010/sscsdltour

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Detalhes sobre as palestras e biografia dos palestrantes:

- 1st Invited Distinguished Lecturer

Challenges in designing CMOS wireless System-on-a-chip

David Su, VP of Analog/RF Engineering, Atheros Communications, Santa Clara, CA, USA

Abstract

This talk describes the challenges in designing CMOS systems-on-a-chip for wireless communications. RF transceiver building blocks for signal amplification, frequency translation, and frequency selectivity are examined with special emphasis on low noise amplifier, power amplifier, mixer, and frequency synthesizer. System-on-a-chip integration issues are also discussed.

David Su is the VP of Analog/RF Engineering at Atheros Communications, engaging in the design of CMOS wireless SoC. Prior to joining Atheros, he worked at Hewlett-Packard Company designing CMOS mixed-signal/RF integrated circuits. Dr. Su is an IEEE fellow and a consulting professor at Stanford University. He has been a JSSC associate editor and is currently the ISSCC wireless subcommittee chair. He holds a Ph.D. degree from Stanford University as well as MS and BS degrees from the University of Tennessee, Knoxville.

- 2nd Invited Distinguished Lecturer

Microprocessor Design in the Nanoscale Era

Stefan Rusu, Sr. Principal Engineer, Intel Corporation, Santa Clara, CA, USA

Abstract

This presentation covers the latest trends in high-performance microprocessor design, including multi-core designs, process technology directions, power and leakage reduction techniques, as well as an update on packaging and thermal modeling.

Stefan Rusu received the MSEE degree from the Polytechnic University in Bucharest, Romania. His industry experience includes over 18 years with Intel Corporation and 6 years at Sun Microsystems. He is presently a Senior Principal Engineer in Intel's Microprocessor Development Group leading the technology and special circuits design for the Xeon® Processor family. He has authored over 90 papers on VLSI circuit technology and holds 34 U.S. patents. He is an IEEE Fellow and a member of the Technical Program Committee for ISSCC, ESSCIRC and A-SSCC conferences. Stefan is an Associate Editor of the IEEE Journal of Solid-State Circuits and a Distinguished Lecturer of SSCS.

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- 3rd Invited Distinguished Lecturer

Power Efficient Data Converters

Franco Maloberti - University of Pavia, Pavia, Italy

Abstract:

Portable and nomadic systems require developing power effective and power aware design methodologies for either analog or digital circuits. For data converters, low power and optimal resolution imply a favorable allocation of the noise budget. The noise comes from different sources: quantization, sampling, clock jitter, spur interference and board interference. The distribution of the available noise budget, that becomes lower and lower as the supply diminishes, depends on the specification of the system and it may require one or more extra-bits in the data converter. The noise budget issue is new; it was rarely faced in the past when power was just a concern for limiting the chip temperature. The growing relevance of power efficiency is demonstrated by the great attention on the figure of merit (FoM) of data converters that, in the past few years, has been reduced by almost two orders of magnitudes. The presentation will show that obtaining power effectiveness is a matter of trade-offs between architecture, design methodologies, and implementation of circuits. Advancements in technology challenge data converter design. In addition to a reduced supply voltage, the worsening of transconductance and output resistance degrades the intrinsic gain and makes it difficult to design high gain op-amps. Noise, both thermal and 1/f, also increases. Moreover, accuracy and linearity of passive and active components is problematic at minimum features. All those limits must be understood and accounted for to ensure effective data converters design. After discussing the above general issues this presentation will describe the design of significant achievements and illustrate their experimental verifications. The given design examples, pertaining data converters operating in different regions of conversion speed and resolution, are a power effective sigma-delta for DVB-H, an ultra low-power SAR and a high speed power effective pipeline-SAR. The digital assisted technique is then briefly discussed.

Prof. Franco Maloberti received the Laurea degree in physics (summa cum laude) from the University of Parma, Parma, Italy, in 1968, and the Doctorate Honoris Causa in electronics from the Instituto Nacional de Astrofisica, Optica y Electronica (Inaoe), Puebla, Mexico, in 1996. He was the TI/J.Kilby Chair Professor at the A&M University, Texas and the Distinguished Microelectronic Chair Professor at the University of Texas at Dallas. He was a Visiting Professor at The Swiss Federal Institute of Technology (ETH-PEL), Zurich, Switzerland and at the EPFL, Lausanne, Switzerland. Presently he is Microelectronics Professor, Head of the Micro Integrated Systems Group, University of Pavia, Italy and Honorary Professor, University of Macau, China SAR. His professional expertise is in the design, analysis, and characterization of integrated circuits and analog digital applications,

mainly in the areas of switched-capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analog and mixed A/D design. He has written more then 400 published papers on journals or conference proceedings, four books, and holds 30 patents. Prof. Maloberti was the recipient of the Italian XII Pedriali, in 1992. He was co-recipient of the 1996 Fleming Premium, IEE, the best Paper award, ESSCIRC-2007, and the best paper award, IEEJ Analog Workshop-2007. He received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 IEEE CAS Society Golden Jubilee Medal, and the IEEE Millenium Medal. Dr. Maloberti was Vice-President, Region 8, of the IEEE Circuit and Systems Society (1995-1997), Associate Editor of IEEE-Transaction on Circuit and System-II 1998 and 2006-07, President of the IEEE Sensor Council (2002-2003), member of the BoG of the IEEE-CAS Society (2003-2005) and Vice-President, Publications, of the IEEE CAS Society (2007-2008). He is Distinguished Lecturer of the Solid State Circuit Society and Fellow of IEEE.

- 4rd Invited Distinguished Lecturer

Ultra Low Power Electronics in the Next Decade

Ajith Amerasekera, Director Kilby Research Labs, Texas Instrument Inc. Dallas, Texas, USA

Abstract

We are seeing a shift in electronic technology from centralized and high-touch to ubiquitous and low-touch. Semiconductors are enabling intelligent systems to be developed that enable a more immersive environment expanding the role and applications of electronic technology. Driving this change is the availability of low power electronics for wireless connectivity and performance processing. In the next decade, our ability to develop system-level solutions for energy management, delivery and consumption, will determine the extent to which the application space for electronic technology will grow. Power management techniques developed in the last decade have
focused on process technology and circuit design techniques. As we move to distributed intelligent systems, power reductions of another few orders of magnitude are required. This talk looks at some of the key areas for innovation ranging from ultra-low
power chips for personal and health technology to solutions for energy generation and delivery for autonomous systems.
The constraint for the development and deployment of autonomous systems is access to the energy sources. In most applications advances in battery technology together with some form of harvesting and storage will be possible provided the power requirements
are low. The present battery technology roadmap has a 2x capacity improvement every decade, while the power demand will probably increasse at the rate of 2x every 18 months or so. Key areas for innovation are in RF/analog, where achieving wireless connectivity with high data rates will be a challenge for low power, the need for more performance embedded processing, and the sensor technology, as well as the battery, energy generation,

harvesting, and management. The next decade will see strong cross functional design between multi-scale systems engineers, circuit designers, and software engineers.

Ajith Amerasekera is a TI Fellow and Director of the Kilby Research Labs at TI. He received his PhD in 1986 and then worked at Philips Research Labs, Eindhoven, The Netherlands, on the early submicron semiconductor development. In 1991, he joined Texas Instruments, Dallas in the VLSI Design Labs. He has worked on circuit design and mixed signal IP development for TI's CMOS technologies from 250nm to 32nm. Before taking up the role at the Kilby Labs, Ajith was Chief Technology Officer for TI's ASIC Business Unit and Director of ASIC Technology Strategy. He has 28 issued patents, and has published over 100 papers in technical journals and conferences as well as 4 books on Electronics. Dr. Amerasekera has served on the technical program committees of many international conferences, and was the Technical Program Chair of the 2010 VLSI Symposium on Circuits.