Multi-Chip Module (MCM-D) Using Thin Film Technology

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ABSTRACT

Multi-chip Module (MCM) is a technology that can be applied to silicon and alumina modules allowing advantages in the integration complexity. This paper reports a MCM-D (D for deposition) technology suitable to fabricate passive components using two metal levels and non-photosensitive polymer benzocyclobutene as dielectric. The devices are produced using thin film technology, vacuum metallization, electroless and electrolytic deposition, photolithography process and wet etching. Electrical measurements and focused ion beam (FIB) were used to evaluate the characteristics of the MCM-D structures.

Index Terms: Multi-Chip module; passive components; benzocyclobutene; thin film multilayer.

I. INTRODUCTION

Advances in portable communication devices have produced a great demand for shorter interconnection and high performance packaging. As a result, tridimensional packaging technology (3D) was developed and improved [1-3].

Multi-Chip Module (MCM) is one of such 3D technologies and has several advantages over conventional single-chip approaches. Some advantages are: packaging efficiency, reduced size and improved electrical performance. Different materials and processes have been proposed for MCM applications leading to three types of MCMs: laminated (MCM-L), co-fired ceramics (MCM-C) and thin film processing (MCM-D) [4-6].

The MCM-D technology allowed the interconnection of high-speed digital integrated on circuit applications, producing high-density interconnections to assemble several components in one single module or package [7-10].

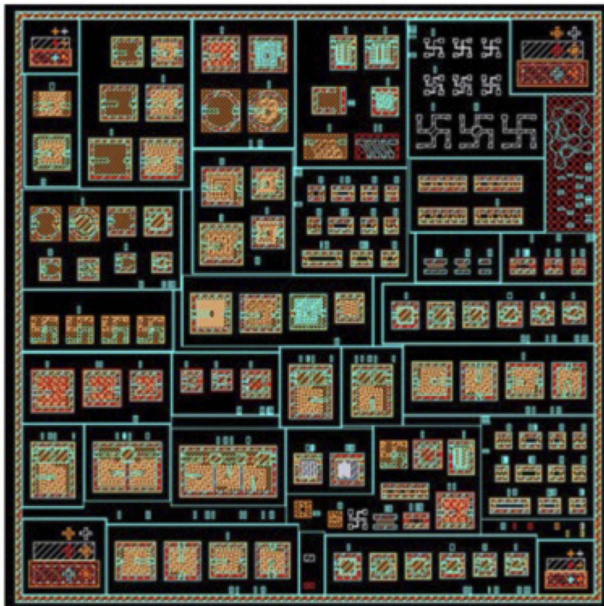
It was previously demonstrated a process sequence of MCM-D passive devices on alumina (Al_2O_3) substrate produced by electrolytic and electroless metallization [11]. The polymer benzocyclobutene (BCB) was used as the dielectric due to its physical properties such as low dielectric constant, thermal stability and its high degree of planarization over a rough substrate [12]. That process required two dielectric levels and four metallization layers. Resistors were fabricated on the lowest thin film layer while inductors and capacitors were on upper layers.

An alternative MCM-D sequence was proposed [13] where the metal layer used for the formation of the resistor contacts is also used for making the conducting lines and the passive components, producing the MCM-D with only one dielectric level. In this paper, authors present the results of this process followed by the discussion of its electrical characterization.

II. EXPERIMENTAL

The MCM-D process developed at Electronic Packaging Division (DEE) of Renato Archer Center for Information Technology (CTI) and Center for Semiconductor Components (CCS) of University of Campinas (UNICAMP) is based on thin film technology to build interconnection structures and passive components onto deposited metals and dielectrics over the substrate.

Fig. 1a presents the new testchip designed for this development and Fig. 1b shows a finished sample. Fig. 2 shows a tridimensional view of MCM-D passive components. The substrates used in the proposed MCM-D were Al_2O_3 (99.6 %) or 8000 Å wet oxidized silicon (SiO_2).



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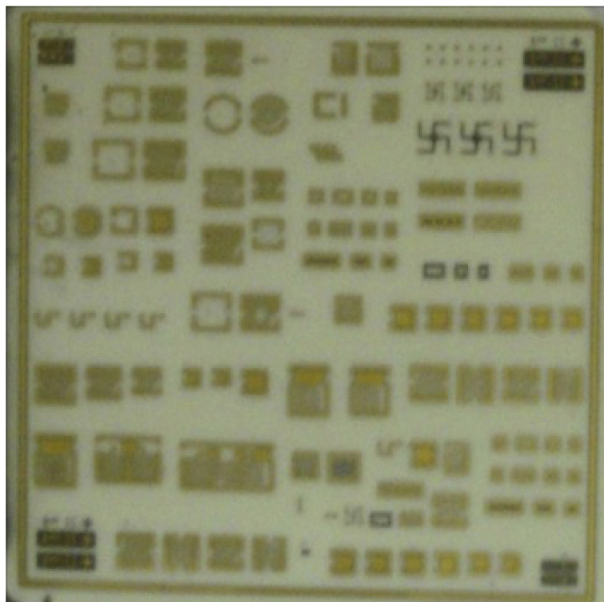

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Figure 1. a) Layout of the testchip and b) photography of one sample.

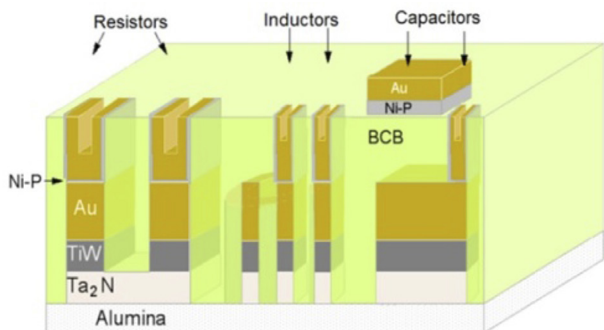


Figure 2. Schematic tridimensional view of the MCM-D (not in scale).

Al_2O_3 wafers were cleaned with neutral detergent Extran MA02 (Merck) in an ultrasonic bath at 60°C and the Si wafer using RCA procedure. The substrates were cleaned in deionized water and dried with a nitrogen flush (N_2).

Thin films of tantalum nitride (TaN -1000 Å), titanium tungsten (TiW-300 Å) and gold (Au -1000 Å) were deposited by reactive DC sputtering (Sputron II - Balzers) onto the substrates sequentially, i.e., without breaking the vacuum from one deposition to another. TaN reactive deposition was performed at 200°C (substrate temperature) by means of a Ta target etched by Argon (Ar) plasma in a N_2 atmosphere to produce the alloy. The base pressure for TaN deposition was about 10^{-6} mbar, while partial pressures during deposition were 8×10^{-5} mbar for N_2 and 4×10^{-3} mbar for Ar. The sputtering was performed at 1.0 kV with depositions rate: 1.6, 1.0 and 18.2 Å/sec respectively for TaN, TiW and Au.

After that, the Au layer was thickened by an electrolytic commercial solution (Auruna 553 - Umicore) up to 1 μm. The temperature during the thickening process was kept at 70°C with mechanical agitation during the deposition. In the electrolytic process, the thickness is controlled by deposition time and current density. For this procedure, the deposition rate is about 0.1μm/min using the current density of 0.2 A/dm^2.

The devices were patterned by a two step photolithography (Karl Suss MJB3) and wet etching process. First, the layers TaN, TiW and Au were etched in a solution containing HF (48%), HNO_3 (65%) and DI H_2O (1:1:4); H_2O_2 (30% v/v) and Umicore 645 respectively to define the components (capacitors, inductors and filters) area. Second, the Au and TiW were etched from the resistors to define the contact pads.

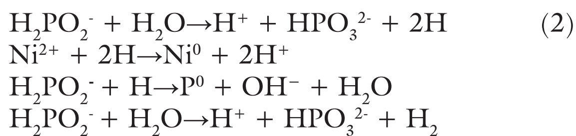
BCB polymer (Cyclotene 3022-35 - Dow Company) was spin coated at 2000 rpm during 30 sec and cured in a N_2 atmosphere at 250°C for 1 hour in an oven. BCB surface was treated on a plasma environment (Precision Etcher 8300 A - Applied Materials) to improve adhesion of the second metal layer (NiP/Au). The experimental parameters of the discharge were: 10 sccm Ar, 90 sccm O_2, and pressure of 50mTorr, power density of 500 W and treatment time of 4 minutes.

After the treatment, a nickel-phosphorus (Ni-P)/Au hard mask was patterned as third photolithography step (lift-off) to define the interconnection vias on the polymer.

To build the Ni-P/Au hard mask, it is necessary to create a Sn/Pd seed layer onto the BCB using a process similar to the one proposed by Garrilow [14] with adaptations [15] using a two-step process. The sample was immersed successively in tin (Sn^{2+}) and palladium (Pd^{2+}) solutions three times. The Sn^{2+}

adsorbed on the surface reduced the ions Pd^{2+} (eq. 1) [16]. The Pd^0 atoms form clusters that act as seed layer for the catalytic electroless Ni-P deposition. A non-commercial autocatalytic solution of electroless Ni-P, similar to the one presented Dubin *et. al*. [17-18] was used. The solution were composed of: $NiCl_2$, NaH_2PO_2, $CH_3C_2O_2Na$, NH_4Cl and $Pb(NO_3)_2$. Deposition temperature was 60°C with mechanical agitation and deposition rate was about 0.1μm/min. The main reactions induced by the bath are shown in (eq. 2) below [19].

$$Pd^{2+} + Sn^{2+} \rightarrow Sn^{4+} + Pd^0 \qquad (1)$$



$$\begin{aligned} &H_2PO_2^- + H_2O \rightarrow H^+ + HPO_3^{2-} + 2H \qquad (2)\\ &Ni^{2+} + 2H \rightarrow Ni^0 + 2H^+\\ &H_2PO_2^- + H \rightarrow P^0 + OH^- + H_2O\\ &H_2PO_2^- + H_2O \rightarrow H^+ + HPO_3^{2-} + H_2 \end{aligned}$$

The Au layer onto the Ni-P was deposited using the commercial electroless bath Dip Gold 512 at 90°C during 5 min. After liffting-off the vias apertures on the Ni-P/Au hard mask, the BCB was etched in RIE (Reactive Ion Etch) equipment with the following parameters: chamber pressure: 50mTorr; plasma power: 500 W; plasma time: 30 minutes; SF_6 flow rate: 10 sccm and O_2 flow rate: 10 sccm. A new Ni-P and Au layers were finally deposited to interconnect the vias using electroless and electrolytic process using the same procedures already described in early sections, i.e. non-commercial autocatalytic solution for electroless Ni-P and Auruna 553 for Au.

Finally, one last photolithography process was done to pattern the contact pads and the capacitors plate. Fig. 3 presents the sequence with the main process steps to produce the MCM-D.

Electrical measurements were performed using different equipments attached to a probe station. Resistors were characterized using a Hewlett-Packard 4145B and Agilent B1500A network analyzer. Agilent B1500A was also used to characterize the capacitors. Inductors were characterized using a Hewlett-Packard 8510-C network analyzer. Cross sections of the devices were studied using a Focused Ion Beam (FIB) from NOVA 200 Nanolab-FEI Company. The thickness of the films was determined using a Dektak XT scan profiler.

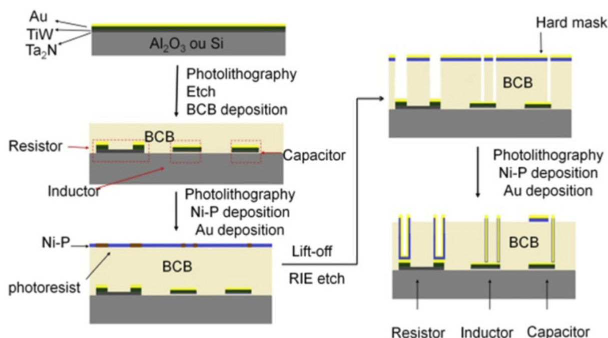


Figure 3. Schematic process steps of the fabricated MCM-D (not in scale).

III. RESULTS AND DISCUSSION

- Interaction between layers

A good adhesion between layers is necessary for the microfabricated devices to achieve a good performance. To evaluate the adhesion it was performed a pull strength test using 3M tape which is compressed to remove residual air and pull after the deposition of Ni-P/Au onto the BCB surface. After the pull test it was observed that no residues from the deposited films were attached on the tape. This means that the activation of the BCB surface was effective and a good adhesion between metal layer and BCB was achieved.

Fig. 4 shows a FIB cross section of one via hole. It can be observed that the Au layers above and below the BCB are connected, due the good conformal deposition achieved on the vias sidewalls creating a continuous path that will allow the electrical measurements.

Fig. 5 shows the thickness profile as extracted from Dektak XT. This measurement was performed on a test structure specifically projected for this purpose and not on the actual devices. Measured film thicknesses are: 1.5 μm from BCB and 1.2 from Ni-P/Au. We also confirmed the high degree of planarization of the BCB as the roughness on this film was only 10 nm on average.

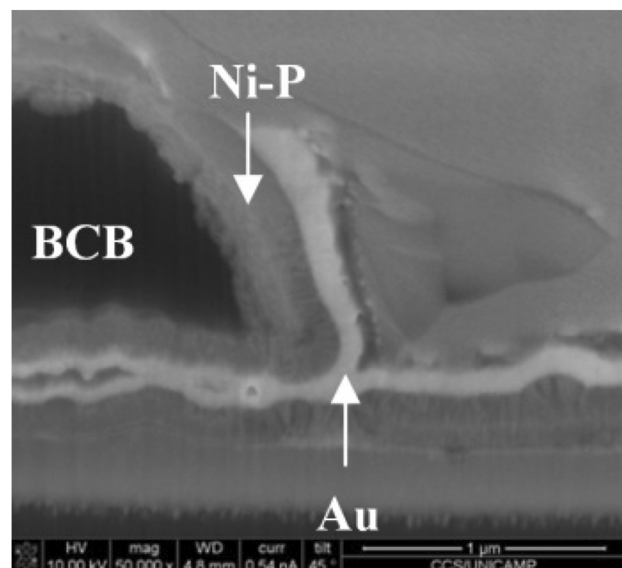


Figure 4. Cross section from the via hole.

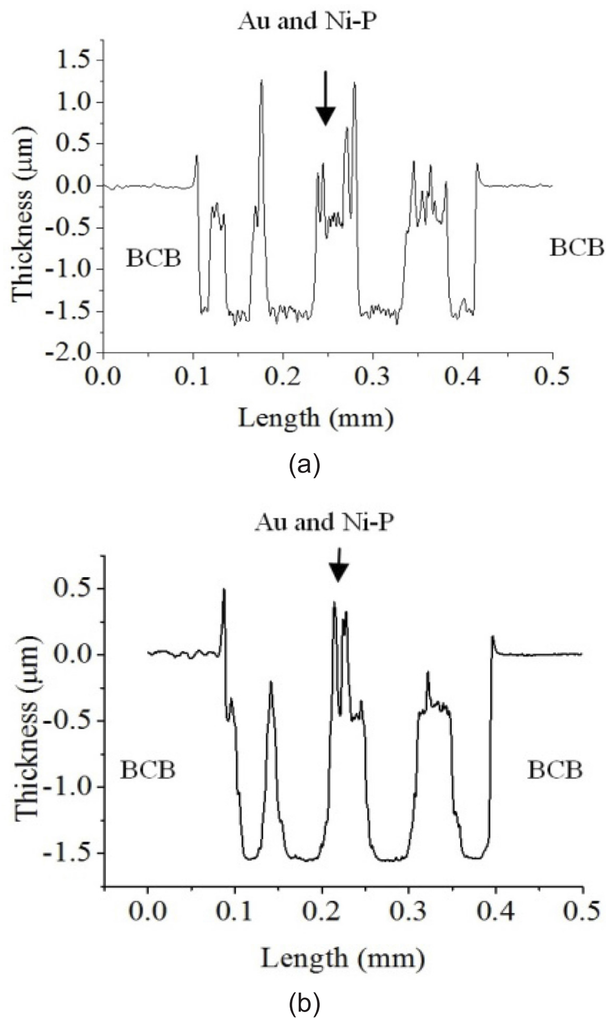
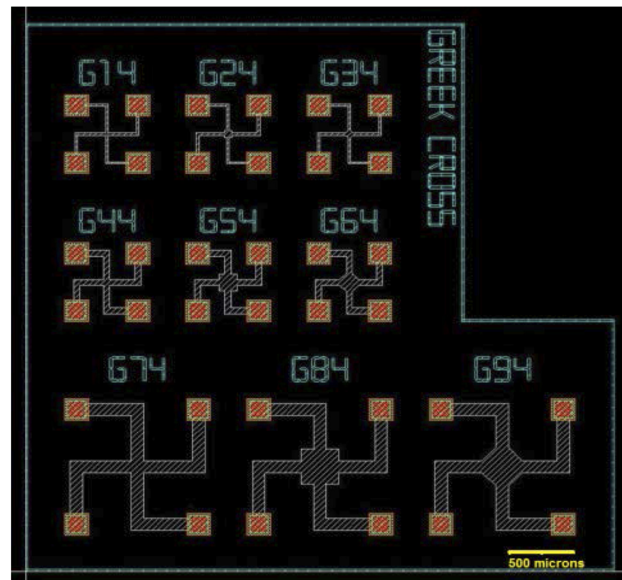


Figure 5. Profile of the films on different substrates (a) Al_2O_3 e (b) Si/SiO_2.



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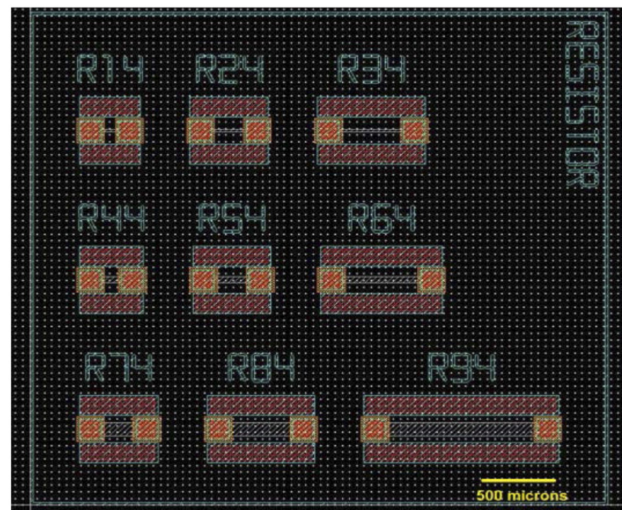

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Figure 6. a) Example of Greek-Cross structures and b) resistors. The tool bar indicate 500 microns.

- Electrical measurements

The testchip was used to evaluate the process steps and define an alternative technology to fabricate MCM-D devices. It was also designed to extend the characterization of the process parameters of the already proven MCM-D integration route and to investigate the new proposed integration approach. From the electrical measurements of embedded passive devices it was possible to evaluate the viability of this integration.

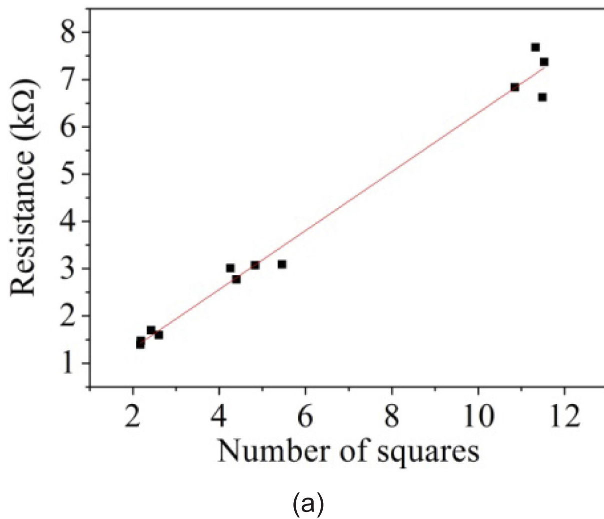
a) Resistance:

In the testchip many structures were designed to study the resistance parameters. Greek-Cross (Fig. 6a) with different geometries and sizes were used to extract the sheet resistance of the TaN film while resistors (Fig.6b) were used to measure the resistivity.

Using $I \times V$ technique it was possible to calculate the resistance against the number of squares for each resistor (Fig. 7). The values obtained are shown in Table I. For Al_2O_3 the values were approximately 560 ohms/□ while Si/SiO_2 provided 120 ohms/□.

Previous works using TaN as the resistance film showed that its mechanical and electrical properties could change depending of the film stoichiometry. The stoichiometry is dependent of the deposition conditions such as the temperature or N_2 pressure [20-22]. That difference could explain the apparently higher resistivity values in comparison with works published before [23-25].

For both substrates considered here the deposition was done at the same time. So the effect of the resistivity five times greater in Al_2O_3 than in Si/SiO_2 could be associated with the roughness of the substrates



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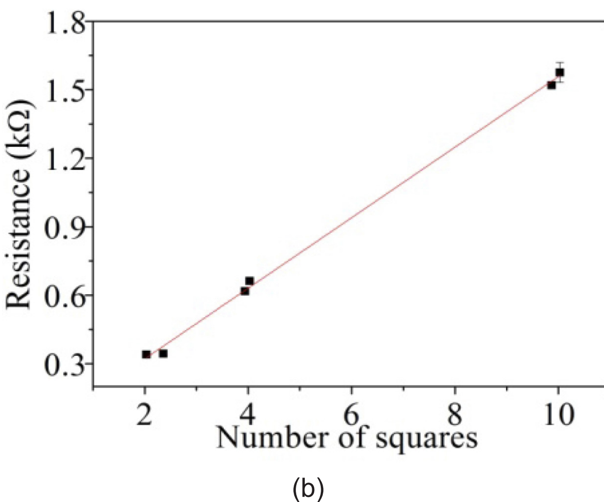

(b)

Figure 7. Resistance per number of squares for resistors fabricated on different substrates: a) Al_2O_3 and b) Si/SiO_2.

Table I: Summary of the resistance results:

	Al_2O_3	Si/SiO_2
Resistivity TaN (mΩ.cm)	6.0 ± 0.8	1.5 ± 0.2
Rs - graphic- resistors (Ω/□)	564 ± 57	123 ± 15
Rs - Van der Pauw - Greek-Cross (Ω/□)	557 ± 76	164 ± 36

[26]. Si/SiO_2 has a roughness average of 37 Å whereas Al_2O_3 has a roughness average of 980 Å. Since the sputtered film is conformal to the surface, this means that the effective length of the devices built onto the Al_2O_3 substrates are much longer that the ones on Si/SiO_2, which explains the observed difference.

Sheet resistance was measured through Greek-Cross structures by the four-terminal Van der Pauw technique. As expected, the geometry or the size of these devices does not produce any difference in the measured value. The value obtained was in close agreement with the indirect resistance calculated from the resistance × number of squares plot (Fig. 7).

b) Capacitors:

Fig. 8 shows the layout of some designed capacitors. BCB is the dielectric for the parallel plate MIM (metal-insulator-metal) capacitors since it has a low dielectric constant (about 2.6) that enables reducing the parasitic capacitance. Moreover, it defines the limit on the capacitance per area that is possible to achieve with this technology.

Capacitances were measured in low frequency range (from 0 to 10MHz). Average measured capacitance and capacitance per unit area are presented in Table II.

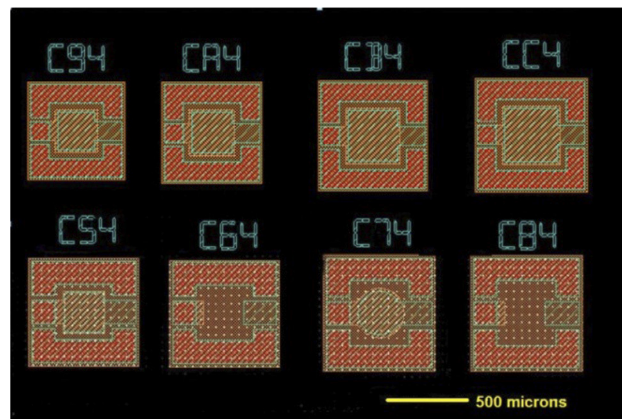

Figure 8. Layout of some capacitors. The tool bar indicate 500 microns.

Table II: Extracted capacitance of MIM capacitors:

Sample	C74	C94	CA4	CC4	C54	C94
Substrate	Si/SiO_2	Si/SiO_2	Si/SiO_2	Si/SiO_2	Al_2O_3	Al_2O_3
Shape	round	square	square	square	square	square
Area (10^{-8} m^2)	5.6	8.3	9.9	17	5.9	8.1
Capacitance (pF)	2.66	3.10	2.81	4.70	1.33	1.04
Capacitance/Area (μF/m^2)	47.9	37.4	28.5	27.6	22.5	12.9

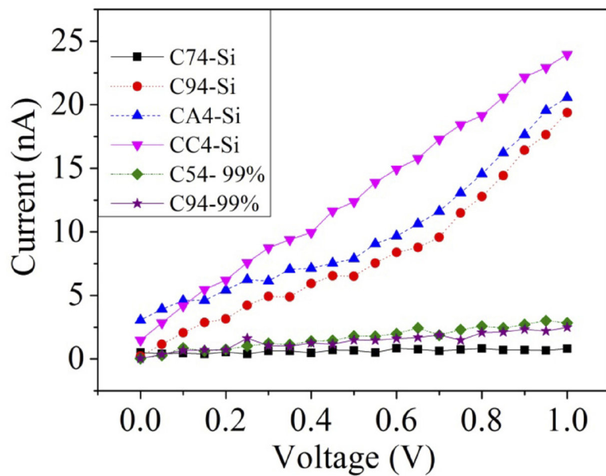

Figure 9. MIM Capacitors leakage current.

Capacitors were built on different sizes and geometries. These are very useful to compare the influence of fringe effects in the final capacitance. These effects are confirmed as the capacitance per unit area decreases (C74-CC4 on Si/SiO_2; C54-C94 on Al_2O_3) with increasing area as the fringe effects are more evident in smaller capacitors.

Capacitors with the same area had higher capacitance on Si substrates than on Al_2O_3 (C74 vs C54-Al_2O_3; C94-Si vs C94-Al_2O_3) due to parasitic capacitances. When comparing the capacitance ratio between both substrates, the round shape (C74) has a smaller value than the square shape (C94) when compared to devices with similar area on the other substrate (i.e. C74-Si(round)/C54-Al_2O_3(square) = 2; C94-Si(square)/C94- Al_2O_3(square) = 2.98), indicating less fringe effects for the round geometry.

Fig. 9 shows that the leakage current was very low indicating a good quality for the BCB film. Some devices however, had an increasing leakage current with ohmic behavior, probably due to pinholes in the BCB. The presence of pinholes in BCB is related with temperature difference in the cure process, which causes solvent bubbles trapped in the film to be released after the cure process is near completion, leaving the pinholes behind.

c) Inductors

Inductors can be used in all stages of an RF IC for input/output matching circuitry and passive filters. They are also convenient loads for active circuits, such as amplifiers where signal excursion and linearity is improved due to the inclusion of this passive device. Although the need for passive inductors can be circumvented by means of active inductors (gyrator) at lower frequencies built with Operational Transconductance Amplifiers (OTAs) and capacitors this kind of implementation is noisy, has high power consumption and is suitable only for low-frequency applications since the frequency response is attached to that of the OTAs [27].

The testchip also included inductors with different shapes and number of turns for comparison, as it can be observed on Fig. 10 and Table III. These devices were characterized by measuring the S-parameter in the frequency range from 0 to 10 GHz. Fig. 11 has a plot of one of this measurements (I-34) in a Smith Chart, as an example.

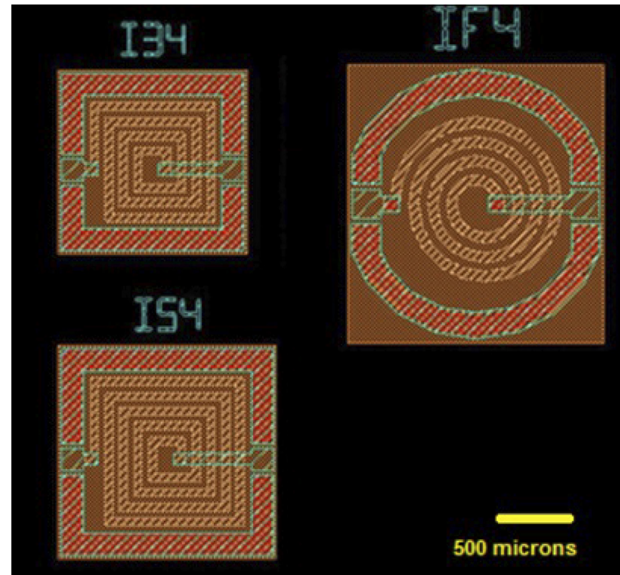

Figure 10. Layout of inductors. The tool bar indicate 500 microns.

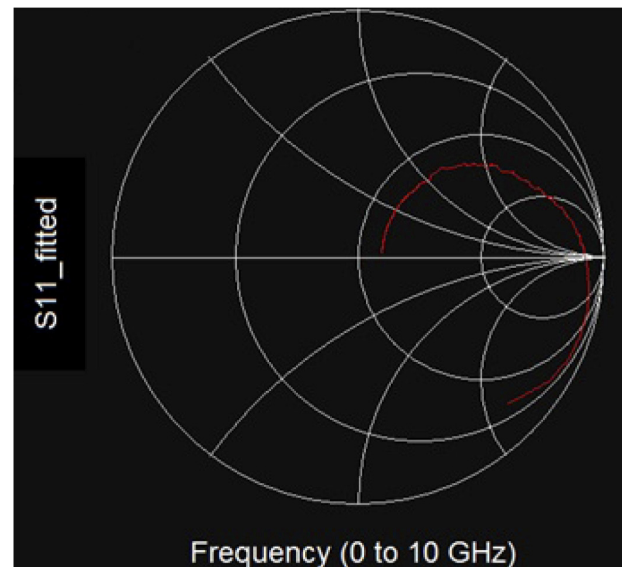

Figure 11. S11 parameter of one inductor I-34 from 0 to 10 GHz.

Table III: Information about the inductors:

Inductor	Shape	Turns	Highest operation frequency (GHz)*	Area (µm)
I54	Square	4.5	1	1200 × 1200
I34	Square	3.5	3	1450 × 1450
IF4	Round	3.5	3	1780 × 1850

*As depicted by the vertical lines in Fig. 12.

Fig. 12 shows the inductance × frequency plot for 3 inductors fabricated on Al_2O_3 substrate, with different shapes and number of turns, and resonant frequency between 3 and 5 GHz.

The square inductor (I-54) had higher inductance value for having more turns than the square inductor (I-34), but also had a worse frequency performance, evidencing that parasitic effects and resistance increase with the number of turns, as shown in Table III.

The round inductor (I-F4) had a smaller inductance value compared with the square inductor with the same number of turns but a higher resonant frequency, probably due to the lower resistance and smaller metal area.

The resistance of inductors was inversely proportional to its frequency performance, increasing insertion loss and resulting in a quality factor (Q) of a few units [28]. This can be solved by increasing the inner space in the inductors' turns, despite the consequent increase in the line resistance [29]. Using narrower lines would also improve the quality factor because the parasitic capacitances would be smaller. These approaches will be used in the design of the next maskset.

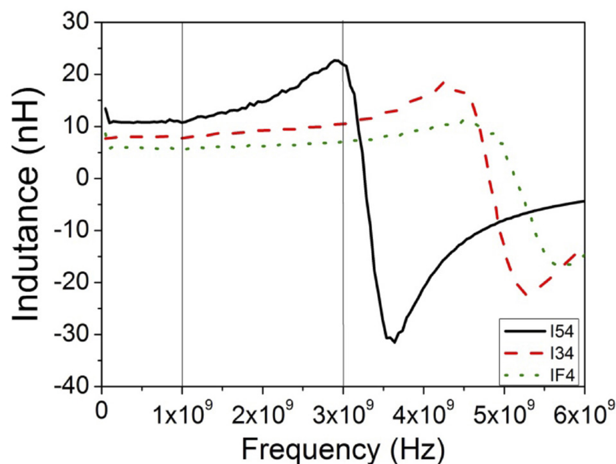

Figure 12. Frequency response of the inductance of three different inductors on Al_2O_3.

Inductors built on Si/SiO_2 substrates had a capacitive behavior in all the measured frequency range, showing a major interference from the substrate on the total parasitic capacitance.

The overall bad performance of inductors is due to the fact that in this mask layout these components are produced directly onto the substrate. While Al_2O_3 substrate has an insulating characteristic, it allowed performing measurements, but the Si-SiO_2-metal layer produces a parasitic capacitance that greatly affected the measurement of the devices. New runs are on the way to include an extra BCB insulating layer to avoid this issue and improve inductors performance.

d) Filters

Passive components in an MCM are also useful to implement RF filters. Low and intermediate frequency filters are of limited use because they need a wider area, but high frequency filters are easily implemented with relatively low area occupancy.

High-pass filters shown in Fig. 13 were designed to demonstrate the use of passive components in filter applications. Most filters were implemented with the series configuration as it uses less area.

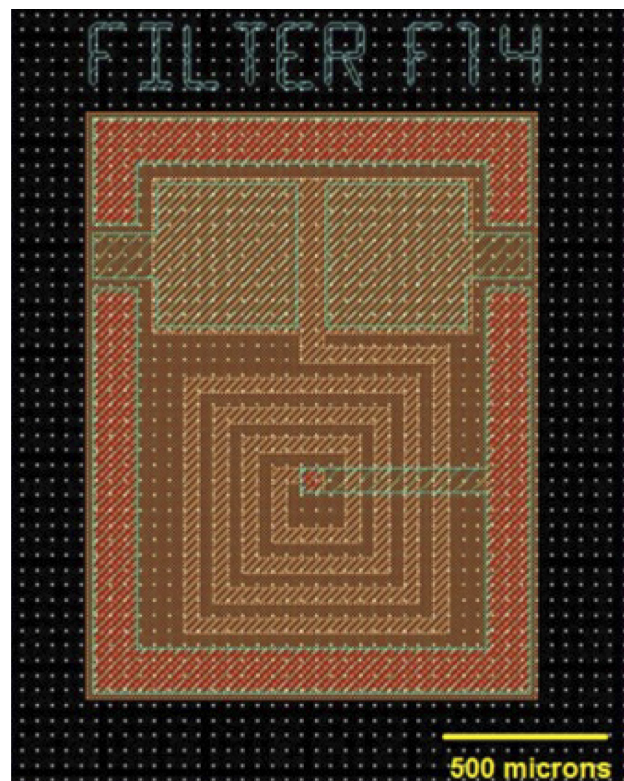

Figure 13. Example of one filter produced. The tool bar indicate 500 microns.

The filter design was made through the use of the free software RFSim99 [30], which were also used to design inductors and capacitors at low frequency.

Fig. 14 has the S21 parameter plotted against frequency for three different filters on Al_2O_3 substrate compared with two simulated results. As the inductors in Si/SiO_2 did not perform well, these filters were not measured. The fabricated filters were originally designed to have cut-off frequencies of 0.9, 1.0 and 1.1 GHz, respectively, while the simulation was based on 1.0 GHz cut-off frequency. It can be observed that the cut-off frequency were very close to the projected, Table IV.

The simulated filter behavior considering ideal components is a little different from the measured curves. On the other hand, using components with real characteristics in the simulation, such as inductors with resonant frequency at 5 GHz as the ones measured in this work (Fig. 12), results are in a good matching with the simulation.

Even with the need for improvement in the quality factor of the passive components, it was shown the possibility of adjusting a filter cut-off frequency by means of a detailed design, which will allow for the development of a filter library.

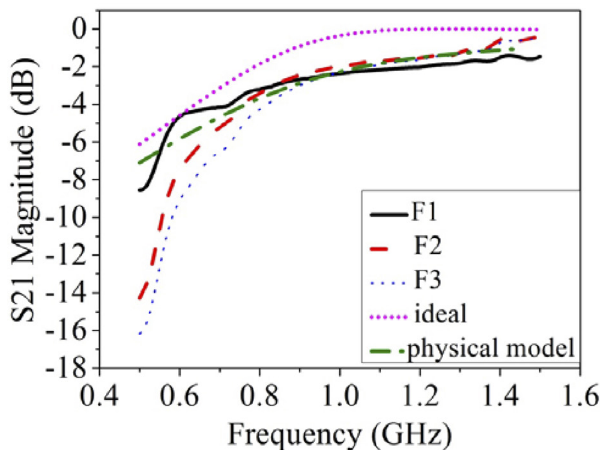

Figure 14. S21 magnitude of filters fabricated on Al_2O_3 substrate.

Table IV: Information about the filters:

Filter	Cut-off Frequency (GHz)	Cut-off Frequency Measured* (GHz)	Total Area (μm)
F14	0.9	0.8	1400 × 1825
F24	1.0	0.8	1300 × 1770
F34	1.1	0.9	1300 × 1740

*As a convention it was established that the cut-off frequency is obtained at the threshold of – 3 dB.

IV. CONCLUSIONS

The development of the MCM-D technology, with several test structures to study process variations and passive components characteristics was effective and also proved that this technology, based on wet process deposition using via holes as contact between layers is capable of producing packaging with good performance.

With the testchip it was possible to prove the viability of the process and to study best ways of implementing passive devices and/or filters. For this technology Al_2O_3 99.6% was more suitable than Si/SiO_2.

The capacitance per area obtained had the same order of magnitude as that commonly found on integrated circuits. Also for the inductors fabricated, it was found that a higher number of turns on device F14 resulted in a slightly higher inductance at the cost of a lesser resonant frequency when compared with that of devices F24 and F34.

ACKNOWLEDGEMENTS

The authors would like to acknowledge CTI Renato Archer (DEE, DMS and DAPE), CCS-UNICAMP, CNPEM (LNNano) for the support on the fabrication and measurement techniques and CNPq, FINEP, FAPESP and INCT Namitec for the financial support.

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