Mitigating MOSFET Radiation Effects by Using the Wave Layout in Analog ICs Applications

Rafael Navarenho de Souza, Marcilei A. Guazzelli da Silveira, and Salvador Pinillos Gimenez

Centro Universitário da FEI, São Bernardo do Campo, São Paulo, Brazil
E-mail: rafaelnds@gmail.com

ABSTRACT

This paper presents an experimental comparative study of the Total Ionizing Dose (TID) effects between the Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFET) manufactured with the Wave (S gate geometry) and the standard layout (CnM). Because of the special geometric characteristic of the gate, drain and source regions of the Wave MOSFET (WnM), this innovative layout proposal for transistors is able to mitigate the TID effects in order to implement in analog integrated circuits (IC) for space and medical applications without causing any additional cost to the Complementary MOS (CMOS) manufacturing process.

Index Terms: Wave layout; Radiation; X-ray; Total Ionizing Dose; TID; Analog Circuits.

I. INTRODUCTION

New materials, multiple-gates and three-dimensional (3D) devices are the subject of intense research and development [1], following the International Technology Roadmap for Semiconductor (ITRS) [2] specifications for future technologies and devices in order to overcome the scaling limits [3-5] and the predictions from Moore's Law [6-7]. However, many of these techniques do not take into account and minimize the radiation effects that produce long-term damage within the oxide layers of the electronic devices, worsening the electrical performance of MOSFET [1]. Many efforts have been made to improve the devices radiation hardness, which mainly can be divided in two categories: one category is related to the optimization of manufacturing process with different materials and technologies [2]; the other one focuses on using non-standard layout for MOSFET [4].

Many techniques have been studied to reduce the TID effect, one way is to extend and overlap the gate oxide to the lateral isolation region of the MOSFET [8], like observed in the Shallow Trench Isolation (STI) technologies where similar method can be applied by pulling back the source and drain regions from the trench edges [9].

An additional proposal is the use of Silicon-On-Insulator (SOI) wafer which isolates the substrate of the operation active region of MOSFET with a buried oxide (BOX) to reduce the power dissipation, the latch-up, the short channel effects (SCE), and the single event effects (SEE) [10]. However, the thick BOX in SOI MOSFET substrates increases the undesired TID effects in these devices, because the ionizing radiation induces positive charges that are trapped in BOX [11- 12].

The Multiple-Gates Field Effects Transistors (MugFET) have been studied and showed to be one of the most promising devices to meet the downscale, however, they have been presented a few years ago, with the issue of the FinFET concept replacing the planar CMOS technology [13], which is a challenge.

In order to meet the downscaling, especially in the sub 20-nm node, the planar ultrathin buried oxide (UTBOX) and thin body SOI (UTB) technologies have been considered as an alternative to replace the Bulk substrate technology [14], for further reducing the SCE and the random dopant fluctuations (RDF) [15]. Besides that, the use of the UTBOX enables a low-power multi-threshold-voltage operation by the use of the back-gate bias [16]. Even though the UTBOX exhibits a significant shifting range of the threshold voltage (V_{TH}), these devices are able to mitigate the TID effects, due to its stronger capacitive coupling effects [17]. Although, the gate oxide becomes thinner and less sensitive to the TID effect, MOSFET manufactured with the Shallow Trench Isolation (STI) is not scaled down in the same proportion to the device size and because of that limits the ionizing radiation tolerance in the Bulk CMOS technology (radiation induced positive charge to be trapped in the STI) [18]. All of these techniques previously considered generate a high cost impact of the CMOS manufacturing process.

In addition to that, the use of Hardness-By-Design (HBD) allows the improvement of the device radiation hardness [18], a very efficient way is to use Enclosed

Layout Transistors (ELT), which completely eliminated the parasitic leakage path of the drain current (I_{DS}) [19]. The ELT is "edgeless", for instance, an annular gate region completely surrounding the drain region, which in turn it is surrounding by the source region [20]. This approach shows to be very effective, enabling the MOSFET to present TID tolerances in multi-Mrad scale [21-22]. The disadvantages for using this approach are the die area and capacitance increase, and the aspect ratio (W/L) limitations [23-25], despite the fact that the ELT is inherently asymmetric [26]. A number of variations of the ELT have also been developed to alleviate those shortcomings to some level [27], although, they do not reduce the die area and change the manufacturing process.

To overcome those disadvantages in the ELT, the new dummy gate-assisted (DGA) n-MOSFET layout was proposed [28]. The experimental results confirmed that this innovative structure for MOSFET is a radiation-tolerant device, even when a voltage of 0 V is applied to the dummies gates and the dummies Metal-layers [23]. Unfortunately, the ELT and the DGA layout increase the total die area of the IC in relation to the IC implemented with the standard layout. The MOSFET manufactured with hexagonal gate shape (Diamond) is an alternative layout to those mentioned above to increase the electrical performance and to maximize the device radiation hardness [29].

In order to improve the device matching, integration factor, reduce die area, increase the breakdown voltage (BV_{DS}) and Electrostatic Discharge (ESD) it was designed the Wave nMOSFET (WnM) [30] and some previous works of the Wave layout style for MOSFETs demonstrated that this innovative layout is able to enhance the analog and digital electrical performance of the planar power MOSFETs [31-32].

The WnM owns three important effects: The high Longitudinal Electrical Field (LEF) that is responsible for increasing the drain current in the device channel [30-32]; the lower Series Resistance (SR) - These two electrical characteristics mentioned occur due to its gate geometric shape and because of the drain and source areas (internal or external drain bias configurations) [30-32]; the third one is related to the special behavior of the Bird's Beak Regions (BBR) of the WnM.

In that context, this work focuses on an experimental comparative analysis of the X-ray radiation effects (TID effects) between the Wave and the standard layouts focusing on the analog CMOS ICs applications.

II. LAYOUT DETAILS

Figure 1 presents the layout of the WnM. It is possible to observe the gate, the drain and source for the superior and inferior semicircles, the longitudinal electrical field ($\overrightarrow{\varepsilon_{//}}$) in the channel, and the bird's beak region.
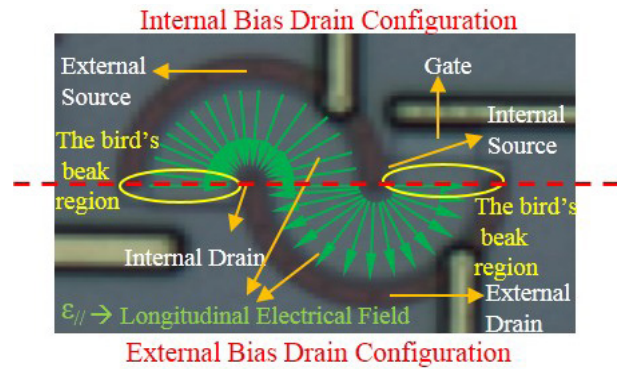
Figure 1. The WnM layout details. The superior and inferior semicircles where the gate, the drain and source can be observed as well as the longitudinal electrical field ($\overrightarrow{\varepsilon_{//}}$) and the bird's beak region.

The WnM comes from the Circular Annular Gate MOSFET (CAGM) [30] that is an asymmetric device (the internal region area, A_{INT}, is different of the external region area, A_{EXT}), by cutting it in the middle, shifting the semicircles and connecting them to compose a "S" shape in order to change the CAGM in a symmetrical device. The Wave layout style can be implemented by using any planar IC CMOS manufacturing processes used to implement the CAGM.

The CAGM can be biased in two different ways, because its internal region can be biased either as drain (internal drain bias configuration, IDBC) or as source (external drain bias configuration, EDBC) [30], which results in two different electrical behaviors, mainly due to the drain (R_D) and source (R_S) series resistances are different, where R_D is higher than R_S, because A_{INT} is smaller than A_{EXT} [30]. However, the MOSFET implemented with Wave layout style, as observed in the Figure 1, operates in the same time with the superior semicircle in the IDBC and the inferior semicircle in the EDBC [30]. Observe that, the Longitudinal Electrical Field (LEF) varies in the channel length (L) [30-32] and it is higher in the drain region of the superior semicircle, because the drain region area of the superior semicircle (A_{D_IDBC}) is smaller than the inferior semicircle area (A_{D_EDBC}) [30-32]. The higher LEF in the drain region of the superior semicircle is responsible to generate a higher I_{DS} than the one found in the inferior semicircle. Besides that, it was demonstrated that the WnM I_{DS} is higher than that found in the standard one (CnM), considering the same gate area (A_G) and bias conditions [30-32].

Considering that the superior semicircle of the Wave MOSFET is in the Internal Drain Bias Configuration (IDBC), the inferior semicircle is in the External Drain Bias Configuration (EDBC). Then, the WnM has a different electrical behavior and the bird's beak region of the WnM behaves in a different way as well. In other words,

the superior semicircle in IDBC and in the inferior semicircle in EDBC have different longitudinal electric field and distinctive drain/source areas, and then the LEF influence in the drain/source area and in the BBR present different behavior for the TID effects. The resultant of the WnM I_{DS} and the parasitic transistors influence are different when compared with the CnM, it should be analyzed and compared in order to understand the TID effects in the devices.

III. EXPERIMENTAL DETAILS

The devices were exposed to 10 keV X-ray irradiation using a Shimadzu XRD-7000 and they were not biased during the irradiation procedure. This initial study is crucial for us to obtain the parameters of the radiation procedure for future works with biased devices, such as the beam energy, beam electric current, dose rate, the exposition time of the device to calculate the cumulated total dose, distance between the beam and the devices under test, etc. [33].

As the first experiment, the irradiations were conducted to a cumulative dose up to 1.5 Mrad (from 500 krad to 1.5 Mrad with 500 krad steps) at a dose rate of 400 rad/s in unbiased devices. Although, the biasing was not used on the irradiations, and it is not the worst-case condition for these devices [34-35], it is understood that this experiment with unbiased devices reveals long term damage generated in the oxide and on bulk silicon [35] This situation, as for instance, describes the real situation of electronics that are not used during a space mission (spare parts) that can present malfunction or the loss of its functionality after TID effects.

Initially, all devices were electrically characterized (Pre-Radiation conditions) with the Keithley 4200 (drain current, I_{DS}, as a function of the gate voltage, V_{GS}, and of the drain voltage, V_{DS}). After that, the devices under test (DUT) were irradiated with X-ray, all at the same time, because they are in the same chip and positioned one beside the other. After that, the electrical characteristics curves of the devices were measured again and compared to the electrical characteristics curves of the devices in Pre-Radiation conditions, until we observe that they became different of the Pre-Radiation conditions. This procedure was repeated several times to identify the first X-ray radiation dose to produce damage in the devices (in this case 500 krad). Additionally, in order to observe the permanent damage in the devices, we performed the electrical characterization of them and compared with the last measurements performed in the irradiated devices in a daily basis. This procedure was done during one week, and then we observed that the electrical characteristics curves do not vary anymore to confirm the transistor transient effects do not exist, i.e., only the permanent damages were con-

sidered in the devices. This same procedure was done to the others X-ray irradiations procedure up to the last one (1.5 Mrad).

The radiation affects electronic components in different ways. Mainly, the effects can be divided into two categories: Single Event Effects (SEE) caused by individual energetic particles and cumulative effects where the device is degraded over time with the total absorbed dose of radiation (Total Ionizing Dose) [33-34], which is the focus of this work. Ionization effect is nothing more than a process of adding or removing electrons (or other charged particles) of atoms. This effect is linked to intensity and exposure time. With radiation, the electrons in the valence band of the material can gain enough energy to move to the conduction band, and then generate current whether an electric field in the irradiated material is applied. Because the mobility of the holes is smaller than the electrons, positive charges may be trapped in $SiO2$ or Si/SiO_2 interface causing degradation of the MOSFETs [33-34].

For this work, the devices were manufactured by using the 0.35 µm AMI (On-Semiconductor) Bulk CMOS ICs manufacturing process, via MOSIS Educational Program (MEP) [34]. The 0.35 µm of the AMI (On-Semiconductor) is performed by using its 0.5 µm C5/F Bulk CMOS ICs manufacturing process, the gate oxide thickness is 14,2 nm and the oxide isolation is LOCOS [36].

Table I presents the dimensions of the Conventional nMOSFET (CnM) and the Wave nMOSFET (WnM) used to perform this work. These devices are in the same die and are next (side by side) to each other.

Table I. The CnM and WnM dimensional characteristics.

Device	Conventional nMOSFET		Wave nMOSFET			
L (µm)	W (µm)	W/L	R1 (µm)	R2 (µm)	W (µm)	W/L
2.3	24.5	10.65	2.7	5.01	23.45	10.19

The relation between the geometric factors (f_g) of the Conventional, Circular Gate and Wave MOSFETs is given by the equation 1 [30].

$$fg = \left(\frac{W}{L}\right)_{conventional} = \left[\frac{2\pi}{\ln\left(\frac{R2}{R1}\right)}\right]_{circular} = \left[\frac{2\pi}{\ln\left(1+\frac{L}{R1}\right)}\right]_{circular} = \left[\frac{2\pi}{\ln\left(1+\frac{L}{R1}\right)}\right]_{wave} \quad [1]$$

In equation 1, R1 and R2 are the radiuses that define the beginning and the ending of the channel region of the transistor structure [30].

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

Table II presents the threshold voltage (V_{TH}) behaviors of the DUTs, after each X-ray exposure, considering Pre-Radiation (indicated by Pre-Rad), transient (immediately after the radiation procedure, indicated by Trans) and Post Rad (after seven days, indicated by Perm) values. The V_{TH} were determined by using the second derivative of the drain current (I_{DS}) as a function of gate to source voltage (V_{GS}), considering drain to source bias (V_{DS}) of 10 mV [37].

From Table II, observe that before the X-ray radiation procedure, the CnM and WnM V_{TH} present the same values (0.68 V).

Considering the transient experimental results, we notice that the CnM is more sensitive to the TID effect and present a V_{TH} variation of 49.2 % from the first to the second radiation dose (from Trans 1 to Trans 2) and 10.2 % from the second to the third dose (from Trans 2 to Trans 3), while the WnM V_{TH} variations for these doses are 4.6% and 5.9%, respectively. In addition to that, the CnM V_{TH} varied about 22.7% for a TID of 1.5 Mrad, while the WnM V_{TH} almost does not change (less than 2%). Therefore, the WnM can be considered as an alternative device to be used in CMOS ICs applications to operate in radiation, due to the Wave layout style characteristics for implementing MOSFETs. The increase of the V_{TH} from Pre-Radiation to the Permanent condition is related to the radiation-induced positive charges through the Si/SiO$_2$ interface, and V_{TH} reduction is associated with the increase of the radiation-induced positive charges inside the SiO$_2$ [1].

The Longitudinal Electrical Field (LEF) of the superior semicircle of the WnM, which is operating as Internal Drain Bias Configuration (IDBC), is higher than the one observed in the conventional counterpart. Knowing that the LEF in the WnM drain region is higher, when this device region is submitted to the ionizing radiation, the TID effect tends to be intensified and promotes a higher induction of the positive charges in its BBR during the irradiation procedure, however its drain area is smaller than the one found in the homologous CnM, which tends to reduce the TID effect in this WnM region. There is a compromise between the LEF and the

drain region dimension that can promote or reduce the TID influence in the device, due to the ionizing radiation exposure.

Besides that, the LEF of the inferior semicircle of the WnM, which operates as external drain bias configuration (EDBC), is smaller than the one found in the equivalent CnM, because the WnM drain area is bigger than the one found in the CnM counterpart, and therefore it shows to be less affected by the ionizing radiation, even though it presents a bigger drain area.
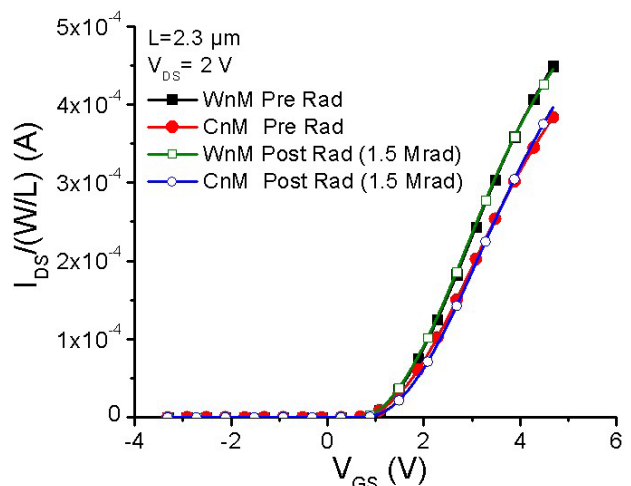
Thus, as a result of this experimental work, we notice that the WnM is less affected by the X-ray ionizing radiation in comparison to the one measured in the homologous CnM.

Figure 2 presents the experimental curves of the WnM and CnM (L=2.3 µm) I_{DS}/(W/L) as a function of the source-gate voltage (V_{GS}) for V_{DS} equal to 2 V.

In the Fig. 2, it can be observed that before TID (Pre Rad) the WnM IDS/(W/L) is 20% higher than the one observed in the CnM counterpart for both operation regions (Triode and saturation regions) Additionally, the CnM I_{DS} variation is of 5%, on average, while the WnM I_{DS} variation is not affected. This is due to the WnM innovative layout and its effects associated, which makes WnM more efficient in this electrical parameter, and with no variation after TID effects.

Figure 3 presents the experimental curves of the WnM and CnM (L=2.3 µm) Log [I_{DS}/(W/L)] as a function of the source-gate voltage (V_{GS}) for V_{DS} equal to 2 V.

From Fig. 3, before the TID of 1.5 Mrad, the devices´ Subthreshold Slopes (S) present the same values (90 mV/decade). But, after the ionizing radiation, we observe that the WnM S (94 mV/decade) present a smaller S variation (4%) in relation to the one measured in the CnM counterpart (29%), which is changing its S value to 116 mV/decade. This can be explained due to the differ-

Table II. CnM and WnM V_{TH} (V) behavior as a function of the TID (Mrad).

Device	Condition	Pre-Rad	Trans 1	Perm 1	Trans 2	Perm 2	Trans 3	Perm 3
	Dose (Mrad)	0	0.5	0.5	1	1	1.5	1.5
CnM V_{TH} (V)		**0.68**	0.59	0.94	0.88	0.88	0.79	0.82
WnM V_{TH} (V)		**0.68**	0.65	0.68	0.68	0.68	0.64	0.64

Figure 2. The I_{DS}/(W/L) as function of V_{GS} with V_{DS}= 2 V of the WnM and CnM for L=2.3µm.
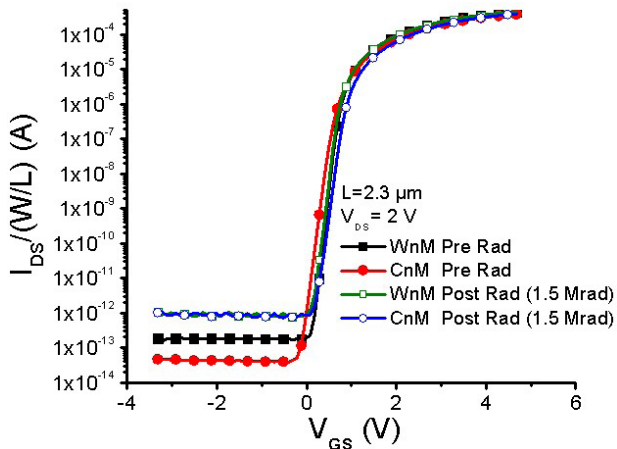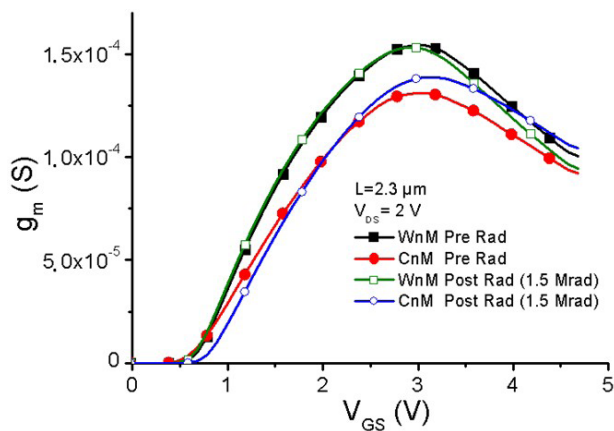
Figure 3. The Log [I_{DS}/(W/L)] as function of V_{GS} with V_{DS}= 2 V of the WnM and CnM for L=2.3μm.

entiate constructive features of the WnM BBRs, which are less affected by the ionizing radiation regarding the BBRs areas and the intensity of the longitudinal electric field present in these regions.

These results show the same trends observed in the V_{TH} variation. Since after TID of 1.5 Mrad the V_{TH} of the CnM increased, a degradation is expected for the S and the curve moves towards to the right, this is due to the positive radiation-induced charges through the Si/SiO$_2$ interface [1]. On the other hand, the S of the WnM is similar, even though there is a slightly decrease of the V_{TH} and the curve moves slightly to the left, this due to the increase of the positive radiation-induced charges inside the SiO$_2$ [1].

Figure 4 presents the experimental curves of the WnM and CnM (L=2.3 μm) g_m (W/L) as a function of the V_{GS} for V_{DS}= 2 V.

In the Fig. 4 observe that WnM g_m for V_{GS} equal to 3 V is 18% higher than the one verified in the CnM

counterpart before TID. Additionally, WnM has less variation (~2%) after the TID, while the CnM has 6% of variation. WnM has a very high Longitudinal Electrical Field and it needs less gate voltage V_G to obtain more drain current (20% more efficiency), it gives to the WnM better control to the drain current by increasing or decreasing the V_G. Besides that, due to WnM LEF effect and BBR, the WnM behaves with higher performance than the CnM for the radiation application (less variation after TID), even that is observed a little more degradation of the WnM g_m for high V_G values due to its high electrical field.

Figure 5 presents the experimental curves of the WnM and CnM (L=2.3 μm) I_{DS}/(W/L) as a function of the drain-gate voltage (V_{DS}) for V_{GS} equal to 2 V.

In the Fig. 5 note that the I_{DS} WnM is 25% higher than the one found in the equivalent CnM for Pre-Radiation. After the TID, the CnM presented 16% of variation, while the WnM showed only 2%. This result is very important to understand the electrical behavior of WnM compared to CnM, in addition to the higher performance of the WnM I_{DS}/(W/L) in Triode region (I_{DS}_tri), this better performance is observed throughout the Saturation region, it means a higher I_{DS}_sat for the WnM when compared to the CnM. Before radiation, the known effects of the Wave layout style prevail over the CnM, its high electric field in the internal drain region and the least equivalent series resistance put the WnM ahead as there is a greater drain current in Triode and Saturation regions compared with the conventional. In addition to that, for the Permanent condition (TID 1.5 Mrad) the WnM practically does not change its behavior, an extraordinary result, because when compared to its equivalent, it turns out 16% of change, this is explained by the WnM's lower sensitivity of the traps created in the gate, drain, source and BBR, where par-

Figure 4. The g_m as function of the V_{GS} with V_{DS}= 2 V of the WnM and CnM for L=2.3μm.
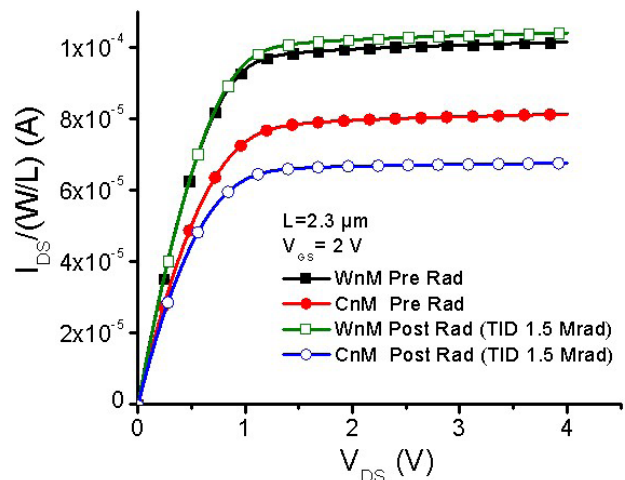
Figure 5. The I_{DS}/(W/L) as function of V_{DS} with V_{GS}= 2 V of the WnM and CnM for L=2.3μm.

asitic transistors created in the BBR have less influence on its electrical performance. These experimental results shown collaborate with the explanation discussed before about the different electrical behavior of the longitudinal electric field and the BBR. Therefore, it is noted that the resulting influence of the traps and the parasitic transistors created after radiation in the WnM are smaller than the CnM. It is possible to say with these experimental results that the WnM varied 14% less compared to its equivalent, this makes the Wave MOSFET an alternative for analog integrated circuits for radiation application.

Figure 6 presents the experimental curves of the WnM and CnM (L=2.3 μm) A_{V0} as a function of the I_{DS}/(W/L) for V_{DS} equal to 2 V.

In Fig. 6 we can observe that the WnM A_{V0} in function of I_{DS}/(W/L) shows better performance in every inversion mode before TID of 1.5Mrad.

For the weak inversion the WnM is 8 % (6dB) greater than the CnM, for the moderate and strong inversions, 6% (4dB) and 10% (3dB), respectively, for a Pre-Radiation condition. This means that WnM has a higher voltage gain in analog integrated circuits.

By comparing the Pre-Radiation with Permanent condition the CnM presented 4% (3 dB) of variation in weak inversion for I_{DS}/(W/L) of 1×10^{-9} (A), 7% (5 dB) of variation in moderate inversion for I_{DS}/(W/L) of 3×10^{-8} (A), and 10% (4 dB) in strong inversion for an I_{DS}/(W/L) of 1×10^{-4} (A). On the other hand, the WnM maintains similar performance with minimum variation after radiation exposure in every inversion mode, except for the results in the beginning of the weak inversion where there was a 5% drop or 4 dB. Therefore, for analog circuits implemented for radiation application such as a CMOS with low power - low voltage, when the moderate inversion region is generally used due to a good compromise
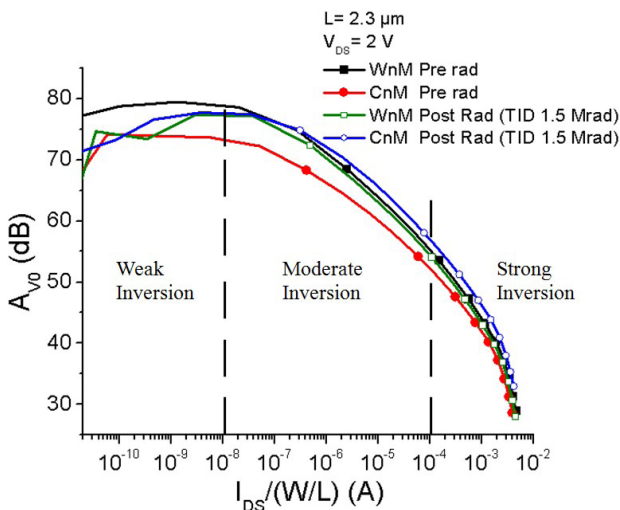
between A_{V0} and f_T, the WnM is a very attractive option. In addition to that, in the strong inversion the WnM could maintain a high frequency response in the circuit, since no change was observed after the radiation process. There is degradation in the weak inversion, however the degradation is similar between CnM and WnM. Those conclusions indicate that for a differential pair of an Operational Transconductance Amplifier (OTA), for example, the Wave MOSFET should have better results in terms of A_{V0} when compared to the CnM. The CnM increase of the A_{V0} after radiation occurs due to the parasitic MOSFETs in the BBRs of the CnM are activated and consequently its transconductance (g_m) tends to be increased. This does not occur in the WnM due to its special constructive feature of its BBRs, which maintain the parasitic MOSFETs in these regions practically deactivated.

Figure 7 presents experimental results of the WnM and CnM (L=2.3 μm) f_T as a function of I_{DS}/(W/L) for V_{DS}= 2 V. The Load Capacitance (C_L) used for f_T values is 10 pF.

Fig. 7 shows that WnM f_T is 23% higher than the CnM, considering an I_{DS}/(W/L) equal to 250 μA. Moreover, the WnM has a similar behavior (less than 2% of variation) after TID, while the CnM varied 8%. TID effects can be mitigated by design strategies (HBD, Hardening-By-Design), where the traps that causes impact in the device operation and the parasitic transistors effects in the bird's beak regions are reduced in this case. The WnM enhances the design of the analog ICs when higher f_T is required and this better behavior is not degraded after TID. For instance, in an OTA, this characteristic is important and the Wave MOSFET can be an alternative for the output stage of an OTA as well.
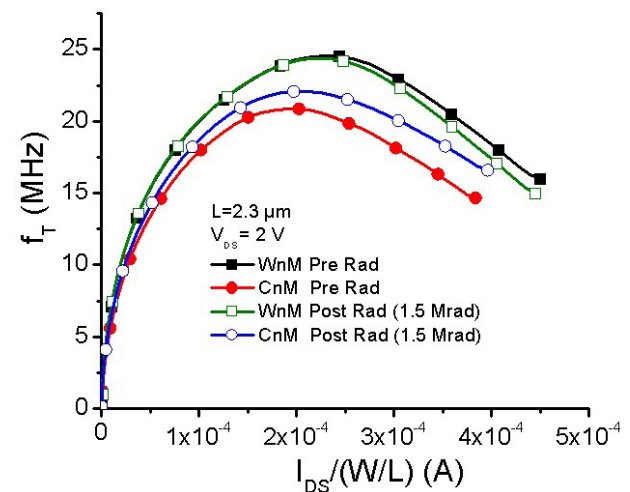

Figure 6. The A_{V0} as function of the I_{DS}/(W/L) with V_{DS}= 2 V of the WnM and CnM for L=2.3μm.

Figure 7. The f_T as function of I_{DS}/(W/L) with V_{DS}=4V of the WnM and CnM for L=2.3μm.

V. CONCLUSION

Besides the Wave layout style is able to improve the integration and devices matching (without generating any extra cost to the IC CMOS manufacturing process) it enhances the radiation tolerance, considering the experimental results in terms of the threshold voltage, the I_{DS}/(W/L) as a function of V_{GS}, g_m, I_{DS}/(W/L) as a function of V_{DS}, A_{V0} and f_T after TID effects (1.5 Mrad), with same aspect ratio and bias conditions. This can be mainly justified due to the electrical behavior of the longitudinal electrical field in the drain/source area and the Bird's Beak regions of the Wave layout style for MOSFET that reduces the radiation impacts. Therefore, this innovative layout structure can be considered as an alternative device to be used in analog IC operating for radiation application (medical and space applications), with a favorable compromise between A_{V0} and f_T.

ACKNOWLEDGEMENT

REFERENCES

[1] H. Barnaby, "Total-Ionizing-Dose effects in modern CMOS technologies," IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3103- 3120, 2006.

[2] International Technology Roadmap for Semiconductors website. Available: http://public.itrs.net/.

[3] G. K. Celler and S. Cristoloveanu, "Frontiers of silicon on insulator," J. Appl. Phys., vol. 93, no. 3, pp. 4955, 2003.

[4] J.P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C.Claeys, "Silicon on insulator "gate all around" device," in Proc. IEDM Tech. Dig., pp. 595, 1990.

[5] M. Vinet, T. Poiroux, J. Widiez, J. Lolivier, B. Previtali, C. Vizioz, B.Guillaumot, Y. Le Tiec, P. Besson, B. Biasse, F. Allain, M. Cassé, D. Lafond, J. M. Hartmann, Y. Morand, J. Chiaroni, and S. Deleonibus, "Bonded planar double-metal-gate NMOS transistors down to 10 nm," IEEE Electron Device Letters, vol. 26, no. 5, pp. 317, 2005.

[6] G. E. Moore, "Lithography and the Future of Moore's Law", Copyright 1995 IEEE. Reprinted with permission. Proc. SPIE Vol. 2437, pp. 2–17, IEEE Solid-State Circuits Society Newsletter, vol. 11, no. 5, pp. 37- 42, Sep. 2006.

[7] C.A. Mack, "Keynote: Moore's Law 3.0," Microelectronics and Electron Devices (WMED) Workshop, Boise, ID, 2013.

[8] T. J. Sanders, "CMOS hardness assurance through process controls and optimized design procedures," IEEE Trans. Nucl. Sci., vol. NS-24, pp.2051–2055, Dec. 1977.

[9] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," IEEE Trans. Nucl. Sci., vol. NS-45, pp. 2584–2592, Dec. 1998.

[10] N. Nowlin, K. Bailey, T. Turfler, and D. Alexander, "A total-dose hardening-by-design approach for high-speed mixed-signal CMOS integrated circuits," Int. J. High-Speed Electron. Syst., vol. 14, no. 2, pp. 367–378, 2004.

[11] V. Ferlet-Cavrois, S. Quoizola, O. Musseau, O. Flament, J. L. Leray,J. L. Pelloie, C. Raynaud, and O. Faynot, "Total dose induced latch in short channel NMOS/SOI transistors," IEEE Trans. Nucl. Sci., vol. 45,no. 6, pt. 1, pp. 2458–2466, Dec. 1998.

[12] F. E. Mamouni, S. K. Dixit, R. D. Schrimpf, P. C. Adell, I. S. Esqueda, M. L. McLain, H. J. Barnaby, S. Cristoloveanu, and W. Xiong, "Gate length and drain-bias dependence of band-to-band tunneling-induced drain leakage in irradiated fully depleted SOI devices," IEEE Trans.Nucl. Sci., vol. 55, no. 6, pt. 1, pp. 3259–3264, 2008.

[13] Y.-K. Choi, T.-J. King, and C. Hu, "Nanoscale CMOS spacer FinFET for the terabit era," IEEE Electr. Device Lett., vol. 23, no. 1, pp.25–27, Jan. 2002.

[14] F. Andrieu, O.Weber, C. Fenouillet-Béranger, P. Perreau, J. Mazurier,T. Benoist, O. Rozeau, T. Poiroux,M. Vinet, L. Grenouillet, J.-P. Noel, N. Posseme, S. Barnola, F.Martin, C. Lapeyre, M. Cassé, X. Garros, M.-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brevard, C. Tabone, P. Gaud, S. Barraud, T. Ernst, and S. Deleonibus, "Planar fully depleted SOI technology: A powerful architecture for the 20 nm node and beyond," in IEDM Tech. Dig., Dec. 2010, pp. 3.2.1–3.2.4.

[15] C. Lee, T. Arifin, K. Shimizu, and T. Hiramoto, "Threshold voltage dependence of threshold voltage variability in intrinsic channel silicon-on-insulator metal-oxide-semiconductor field-effect transistors with ultrathin buried oxide," Jpn. J. Appl. Phys., vol. 49, p. 04DC01-1, 2010.

[16] N. N. Mahatme, E. X. Zhang, R. A. Reed, B. L. Bhuva, R. D. Schrimpf, D. M. Fleetwood, D. Linten, E. Simoen, A. Griffoni, M. Aoulaiche, M. Jurczak, and G. Groeseneken, "Impact of Back-Gate Bias and Device Geometry on the Total Ionizing Dose Response of 1-Transistor Floating Body RAMs," IEEE Trans. Nucl. Sci., vol. 59, no. 6, pp. 2966–2973, December, 2012.

[17] M. Gaillardin, M. Martinez, P. Paillet, F. Andrieu,S. Girard, M. Raine, C. Marcandella, O. Duhamel, N. Richard, and O. Faynot, "Impact of SOI Substrate on the Radiation Response of Ultra Thin Transistors Down to the 20 nm Node", IEEE Trans. Nucl. Sci., vol. 60, no. 4, pp. 2583–2589, August, 2013.

[18] F. Faccio and G. Cervelli, "Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors," IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2413–2420, 2005.

[19] D. R. Alexander, "Design issues for radiation tolerant microcircuits for space," presented at the 1996 NSREC Conf., Indian Wells, CA, Jul.1996.

[20] R. C. Lacoe, "Improving integrated circuit performance through the application of hardness-by-design methodology," IEEE Trans. Nucl. Sci., vol. 55, no. 4, pp. 1903–1925, Aug. 2008.

[21] M. Campbell, G. Anelli, M. Burns, E. Cantatore, L. Casagrande, M. Delmastro, R. Dinapoli, F. Faccio, E. Heijne, P. Jarron, M. Luptak, A.Marchioro, P. Martinengo, D. Minervini, M. Morel, E. Pernigotti, I.Ropotar, W. Snoeys, and K. Wyllie, "A pixel readout chip for 10–30 MRad in standard 0.25 μm CMOS," IEEE Trans. Nucl. Sci., vol. 46, no. 3, pp. 156–160, Jun. 1999.

[22] R. C. Lacoe, J. V. Osborn, R.Koga, S. Brown, and D. C. Mayer, "Application of hardness-by-design methodology to radiation-tolerant ASIC technologies," IEEE Trans. Nucl. Sci. vol. 47, no. 6, pp. 2334–2341, Dec., 2000.

[23] M. S. Lee and H. C. Lee, "Dummy Gate-Assisted n-MOSFET Layout for a Radiation-Tolerant Integrated ," IEEE Trans. Nucl. Sci., vol. 60, no. 4, pp. 3084–3091, August. 2013.

[24] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Hejine, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: Practical design aspects," IEEE Trans. Nucl. Sci., vol. 46, no. 6, pp. 1690–1696, Dec.1999.

[25] A. Giraldo, A. Paccagnella, and A. Minzoni, "Aspect ratio calculation in n-channel MOSFET's with a gate-enclosed layout," Solid State Electron., vol. 44, pp. 981–989, Jun. 2000.

[26] F. Faccio, "Design hardening methodologies for ASICs," in Radiation Effects on Embedded Systems, R. Velazco, P. Fouillat, and R. Reis, Eds. New York: Springer-Verlag, 2007, pp. 143–160.

[27] N. Nowlin, K. Bailey, T. Turfler, and D. Alexander, "A total-dose hardening-by-design approach for high-speed mixed-signal CMOS integrated circuits," Int. J. High-Speed Electron. Syst., vol. 14, no. 2, pp. 367–378, 2004.

[28] M. S. Lee and H. C. Lee, "Dummy gate-assisted n-MOSFET layout for total ionizing dose mitigation (presented conference poster)," in Proc. Nuclear and Space Radiation Effects Conf., Las Vegas, NV, USA, Jul. 2011.

[29] S. P. Gimenez, "Diamond MOSFET: An innovative layout to improve performance of ICs", Solid-State Electronics, v.54, p.1690-1696, 2010

[30] S. P. Gimenez, "The Wave SOI MOSFET: A New Accuracy Transistor Layout to Improve Drain Current and Reduce Die Area for Current Drivers Applications," 215th ECS Meeting, ECS Trans., v. 19. pp. 153-158, San Francisco, 2009.

[31] A. L. da Silva, "Electrical Behavior Study of the Wave SOI nMosfet and Conventional Counterpart," M.S thesis - FEI, São Bernardo do Campo, 2010.

[32] R. Navarenho de Souza, and S. P. Gimenez, "Experimental Comparative Study Between the Wave Layout Style and its Conventional Counterpart for Implementation of Analog Integrated Circuits," ECS Trans., v.49, pp. 519-526, 2012.

[33] J. R. Schwank, M. R. Shaneyfelt, and P. E. Dodd, "Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Radiation Environments, Physical Mechanisms, and Foundations for Hardness Assurance," SANDIA NAT. LAB. DOC., Albuquerque, New Mexico, 2008.

[34] P. C. Adell, L. Z. Scheick, "Radiation Effects in Power Systems: A Review", IEEE Trans. Nucl. Scienc. vol. 60, no. 3, pp. 1929–1952, Jun. 2013.

[35] E. Simoen, M. Gaillardin, P. Paillet, R. A. Reed, and R. D. Schrimpf, M. L. Alles, F. El-Mamouni, D.M. Fleetwood, A. Griffoni, C. Claeys, "Radiation Effects in Advanced Multiple Gate and Silicon-on-Insulator Transistors", IEEE Trans. Nucl. Sci., vol. 60, no. 3, pp. 1970–1991, Jun. 2013.

[36] The MOSIS Service, http://www.mosis.com, 2010.

[37] A. Terao, D. Flandre; E. Lora-Tamayo, and F. Van de Wiele, "Measurement of threshold voltages of thin-film accumulation-mode PMOS/SOI transistors", IEEE Electron Device Letters, vol. 12, pp. 682 - 684, 1991.