The Influence of Back Gate Bias on the OCTO SOI MOSFET's Response to X-ray Radiation

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ABSTRACT

This work investigates the X-ray irradiation impact on the performance of an on-conventional transistor called OCTO SOI MOSFET that adopts an octagonal gate shape instead of a rectangular. The electrical behaviors of both devices were studied through an experimental comparative analysis of the total ionizing dose influence. In addition, the back-gate bias technique was applied in these devices to reestablish its threshold voltages and drain currents conditions that were degraded due the trapping of positive charges in the buried oxide. As the main finding of this work, after the irradiation procedure, we notice that the OCTO device is capable to reestablish its pre-rad electrical behavior with a smaller back gate bias than the one observed in the standard one counterpart. This is mainly because the parasitic transistors in the bird's beak region are practically deactivated due the particular octagonal gate geometry.

Index Terms: Octagonal layout, TID effects, back gate bias, bird's beak region.

I. INTRODUCTION

The Silicon-On-Insulator (SOI) Complementary Metal-Oxide-Semiconductor (CMOS) technology have been showing several benefits in radiation environment when compared to the standard (Bulk) CMOS one, mainly due its smaller active silicon area and the buried oxide layer (BOX), which isolates the silicon film of the substrate [1]. However, the fully depleted (FD) SOI devices, which have a large buried oxide thickness than the one found in the Bulk CMOS technology, present smaller radiation robustness for the total ionizing dose (TID) due to the TID induces positive charges to be trapped in the BOX [2,3].The TID effects become more noticeable as the SOI devices are further downscaled and the gate oxide thickness is further thinned [4]. In this context, there is a strong interest to improve the integrated circuits (ICs) radiation robustness by adopting the standard (Bulk) CMOS technology in radiation environment [5]. Several efforts have been performed to mitigate the radiation effects in ICs, as for instance, changing the electrical characteristics of the MOSFET substrate [6-10] or implementing undoped silicon film (gate region) with multiple gates (MuGFET, FinFET, Gate-all-Around FET) [11-13]. The use of the ultra-thin buried oxide (UT-BOX) planar Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), considering sub-20 nm node, also is used as alternative device to reduce the short channel effect (SCE) [14] and enable a low-power multi-V_{TH} operation controlled by the back-gate bias [15], focusing on the space and medical ICs applications in order to compensate the TID effects on the digital and analog parameters of the MOSFETs.

The Hardening by design (HBD) is a technique that adopts layout strategies to be used in analog and digital ICs to improve the intrinsic radiation tolerance and the reliability of ICs [16], as for instance, the enclosed layout transistor (ELT) [17] and the dummy gate-assisted (DGA) n-MOSFET [18].The Diamond (hexagonal gate shape) layout style for implementing SOI MOSFETs (DSM) can be considered as an example of HBD, because it combines two important features: the radiation robustness and the high electrical performance [19, 20]. This innovative planar SOI MOSFET was carefully invented to use the "Corner Effect" (CE) in the longitudinal direction of the transistor channel, named "Longitudinal Corner Effect" (LCE) to potentiate the resultant longitudinal (parallel) electric field along of the channel ($\overrightarrow{\varepsilon_{\parallel}}$) and consequently improve its electrical performance. The use of this innovative approach can be translated by a simple change in the gate geometry from rectangular to hexagonal, without causing any extra cost to planar CMOS manufacturing

processes [19]. The DSM presents better performance than standard MOSFETs, becoming interesting for analog switches and gate drivers applications [19]. The OCTO SOI MOSFET (OSM) (Fig. 1) is an evolution of DSM that presents octagonal gate geometry. It was specially designed to improve the breakdown voltage (BV_{DS}) and electrostatic discharge (ESD) in comparison to the DSM counterpart [19, 21]. Besides that, both the DSM and OSM have the bird beak regions smaller than those found in the conventional SOI MOSFETs (CSMs) counterparts, regarding the same aspect ratio (W/L, where W and L are respectively the channel width and length) and therefore it tends to be more tolerant to the radiation effects in comparison to the CSMs [20, 21].

Figure 1 presents a photograph of an OSM.

In Fig. 1, b and B are respectively the shorter and longer dimensions of the channel length (L), B' is the height of the triangular part of the hexagonal gate geometry, c is the cut-factor, α is the angle formed by the triangle part edges of the hexagonal geometry of the Diamond, t_{ox}, t_{Si} and t_{BOX} are the gate oxide, silicon film and buried oxide thicknesses, respectively. The OSM effective channel length ($L_{eff-OSM}$), in first approximation, is given by (b+2B)/3 [19, 21].

Therefore, focusing on the space and medical ICs applications, this paper aims to investigate the TID effects due to the X-rays irradiation and the use of the back-gate bias to reestablish the pre-radiation electrical behavior of the n-channel SOI MOSFETs designed with an octagonal gate shape and in the standard (rectangular gate shape) one counterpart.
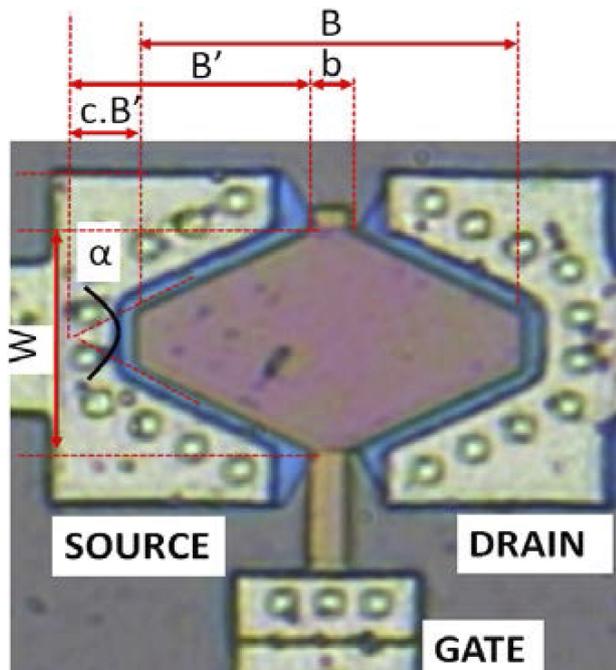
II. DEVICE CHARACTERISTICS

The studied devices are n-channel FD SOI MOSFET manufactured in the WINFAB clean rooms of the Université catholique de Louvain (UCL), Belgium. The CMOS technological parameters of these devices are: t_{ox}, t_{Si} and t_{BOX} equal to 30 nm, 80 nm, 390 nm, respectively, and the channel and drain/source doping concentrations equal to 6.10^{16} cm^{-3} and 1.10^{20} cm^{-3}, respectively. In addition, the process isolation is half shallow trench isolation (STI), half local oxidation of silicon (LOCOS), i.e. we first etch half the Si film and next finish by oxidation as in LOCOS. The nominal supply voltage of this CMOS technology is equal to 5V. Table I presents the devices dimensional characteristics used in this work.

Specifically talking about Diamond and OCTO layouts styles, they present three new effects: I- the LCE, responsible for increasing the longitudinal electric field (LEF): two and three vectors components to the Diamond and OCTO SOI MOSFETs, respectively, along the devices channel lengths [19]; II- the **PA**rallel Connection of **M**OSFET with **D**ifferent Channel **L**engths **E**ffect (PAMDLE) [22, 23] and an important effect to enhance the MOSFET radiation tolerance, named **DE**activator of the **PA**rasitic **M**OSFET in the **B**ird's **B**eaks **R**egions **E**ffect (DEPAMBBRE), due to the special characteristics of its bird's beak, due to the resultant LEF lines in the SOI MOSFETs BBRs are not parallel in its edges, in fact they are curved (Fig. 2), and consequently the parasitic transistors present in these regions are deactivated when submitted to the radiation environment [24]. This tends to prevent to increase in the I_{LEAK} and the shifting of V_{TH} in these devices, which enhances the radiation hardness [24, 25].

Figure 1. A photograph of a fabricated device.

Table I. The OSM and CSM dimensions

Dev.	Cut "c"	α	W	L	W/L	b	B
	[%]	[°]	[µm]	[µm]	---	[µm]	[µm]
CSM	100	180	30	27.5	1.09	---	---
OSM	25	53.1	30	35	0.86	5	50
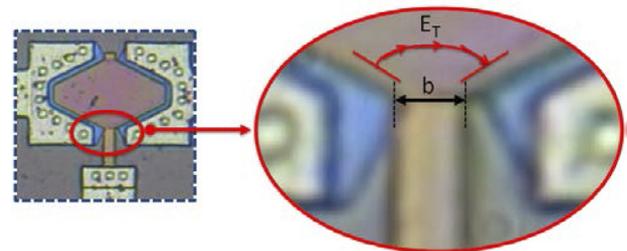
Figure 2. The longitudinal electric field lines of the Bird´s beak regions of the OSM structure are curves and therefore the parasitic MOSFETs in these regions are practically deactivated (DEPAMBBRE effect).

A. Studies performed using the OCTO layout for MOSFET

Previous works have already demonstrated the advantages of the octagonal layout style for MOSFETs in terms of the drain current (I_{DS}), saturation I_{DS} (I_{DS_SAT}), transconductance (g_m), maximum transconductance (g_{m-MAX}), g_m/I_{DS} ratio, Early voltage (V_{EA}), intrinsic voltage gain (A_V), unit voltage gain frequency (f_T) and on-state drain/source series resistance (R_{ON}) in relation to the conventional ones [20]. Besides that, a recent work demonstrated that the OSM presents higher radiation robustness in terms of the V_{TH}, SS and the remarkable results found for the leakage current (I_{LEAK}), in comparison to the standard one [24, 25], considering the same devices gate areas (A_G) and unbiased devices technique [26, 27, 28] during the X-rays irradiation procedure.

III. X-RAY RADIATION PROCEDURE

Studied devices were exposed to the X-ray radiation by using Shimadzu XRD-7000 at an effective energy of 10 keV at a dose rate of 23.5 krad/min (392 rad/s). The devices were irradiated unbiased [26, 27, 28] with a total cumulative dose of 600 krad, from 500 krad to 600 krad, with steps of 50 krad. Besides that, all MOSFETs were placed on the same chip and irradiated at the same time. Initially, we measured the devices without any radiation exposure. Secondly, we performed the measurement immediately after the radiation procedure, getting the first transitory results. To find the permanent damage, we continue measuring them every 24 hours during seven days, until we got the permanent result, in which the electrical characteristics remained the same. The devices were measured at room temperature in natural conditions (no annealing process was performed) using a Keithley 4200 Semiconductor Characterization System.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

The followed parameters and figures of merit were analyzed in order to compare the influence of X-ray radiation effects (TID) between the OCTO and standard SOI MOSFET: V_{TH}, the ratio between on-state drain current (I_{ON}) over the off-state drain current (I_{OFF}) and the I_{DS} x V_{DS}.

A. Threshold Voltage

The V_{TH} behaviors of the studied devices are summarized on Table II, considering the pre-radiation (pre-rad) values (values without TID effects) and the influence of each dose described here as a permanent values (perm), which consider the measurements performed after 7 days of waiting at room-temperature, without any bias applied in the devices. The V_{TH} is determined by using the second

Table II. The OSM and CSM V_{TH}

Dev.	Condition	Pre-rad	Perm	Perm	Perm
	Dose (krad)	0	500	550	600
CSM-	V_{TH} (V)	0.265	-0.87	-0.95	-1.03
OSM-	V_{TH} (V)	0.260	-0.73	-0.73	-0.79

derivative of I_{DS} as a function of V_{GS} curve [29], considering V_{DS} equals 10mV.

Analyzing the V_{TH} values reported on Table II, we observe that the CSM and OSM V_{TH} variations are respectively of 1.3V and 1.0V, considering the TID of 600 krad, i.e., they are very much affected by the X-ray radiation due to thick-coupled BOX [5, 10]. Additionally, increasing the TID, the V_{TH} is further reduced. This can be justified due to the electrostatic coupling of the X-rays radiation-induced positive charges in the BOX [5, 10]. Regarding the V_{TH}, the OSM demonstrates to be more tolerant (19%) to the X-ray radiation in comparison to the CSM counterpart. The main reason is due to the OSM bird beak regions have smaller dimensions than those found in the CSM counterpart, leading to less induced positive charges by the X-rays radiation in the S_iO_2 and S_i interfaces of the parasitic transistors of the OSM BBRs. Therefore, regarding the influence of ionizing irradiation effects in V_{TH}, we can conclude that OSM can considered a good alternative device to be used in analog ICs applications operating in radiation environment.

B. Back-gate Biasing to reestablish the devices pre-radiation electrical behaviors after radiation procedure

In order to minimize the degrading effects of the X-ray radiation over the V_{TH}, we can use the back-gate bias (V_{BG}) technique to reestablish the original V_{TH} value (pre-radiation) of the devices. Table III presents the V_{TH} behavior as a function of the V_{BG} after irradiation procedure.

Analyzing the V_{TH} values summarized on Table III, we deduce that to repair the pre-radiation OSM and CSM V_{TH} values, were necessary -10V and -13V of V_{BG} respectively. In other words, by using OCTO layout style, due to the lower V_{TH} shift with radiation, we need to apply smaller V_{BG} bias values to reestablish the pre-rad V_{TH} and therefore smaller power suppliers are required, when we use the OSM in space and medical ICs applications in radiation environment.

Table III. The OSM and CSM V_{TH} behaviors as a function of V_{BG}, considering 600 krad of TID

Dev.		V_{BG}(V)					
		0	-3	-6	-9	-12	-15
CSM-	V_{TH} (V)	-1.000	-0.584	-0.253	-0.003	0.205	0.447
OSM-	V_{TH} (V)	-0.795	-0.357	-0.112	0.117	0.340	0.557

C. On state drain current over the off-state drain current

Fig. 3 illustrates the CSM and OSM pre-rad and post-rad (600 krad) Log (I_{DS}) as a function of V_{GS}, considering different V_{BG} values.

Note that after radiation, the OSM leakage current (I_{LEAK}) is significantly reduced by approximately one decade and practically achieves the CSM I_{LEAK} levels, due to the DEPAMBBRE in the OSM structure.

Figure 4 presents the I_{DS}/(W/L) as a function of V_{GS} considering the OSM and its corresponding CSM counterpart after X-rays radiation procedure of 600 krad.

By analyzing Fig. 4, regarding the V_{BG} equal to -15 V used to reestablish the pre-rad electrical behavior of the devices and V_{GS} equal to 3V, the OSM I_{ON}/I_{OFF} ratio is about two times higher than the one observed in the CSM homologous, because the OSM I_{ON} remains higher than the one observed in the CSM counterpart, due to LCE and PAMDLE effects keep active in the OSM structure after a X-ray radiation of 600 krad. Furthermore, the I_{LEAK} of both devices are practically the same after ionizing irradiation procedure of 600 krad of X-rays.

Figure 4. The CSM and OSM I_{DS} as a function of V_{GS}, for V_{DS}=4V, considering V_{BG}=-15V after 600 krad.

D. Drain current vs drain voltage

The I_{DS} as a function of V_{DS} of both devices also are analyzed as a function of the back gate bias and are illustrated in Fig. 5.

(a)

(b)

Figure 3. The CSM (a) and OSM (b) I_{DS} as a function of V_{GS}, for V_{DS}=4V, considering different V_{BG} values after 600 krad.

(a)

(b)
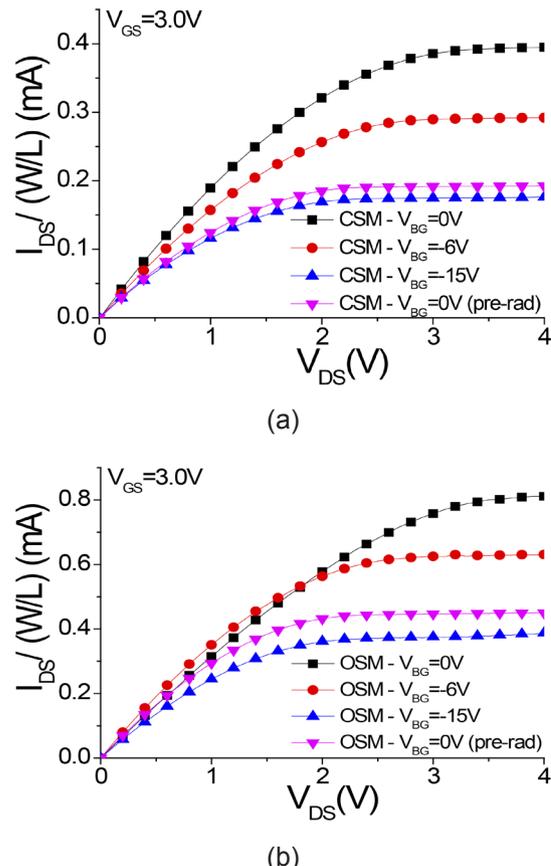
Figure 5. The CSM (a) and OSM (b) I_{DS} as a function of V_{DS}, for V_{GS}=3V, considering different V_{BG} values after 600 krad.

From Fig. 5, we can observe that after X-ray ionizing radiation of 600 krad, the I_{DS} increase in both devices, because the V_{TH} reduction as a consequence of the electrostatic coupling of the X-ray radiation-induced positive charges in the BOX [5, 10]. However, decreasing the V_{BG} bias from 0 to -15V, the pre rad values of the devices can be reestablished. In this case, the OSM value can be reestablished with a V_{BG} equal to -10 V, while for the CSM counterpart was reestablished with a V_{BG} equals -13 V., i.e. with a higher value of the power supplier. Besides that, comparing the pre-rad with the post-rad value, considering TID=600 krad and V_{BG}=0V, we observe that the CSM and OSM I_{DS} vary respectively by 105% and 80% and therefore the OCTO SOI MOSFET present a higher radiation tolerance (25%) than the one found in the CSM counterpart, considering a V_{GS} equal to 3V. This result can be justified due the DEPAMBBRE effect present in the OSM structure. Furthermore, the LCE and PAMDLE effects are kept actives when submitted to the radiative environments and under the influence of the back-gate bias.

V. CONCLUSION

This paper performed an experimental comparative analysis of the TID effects in SOI MOSFETs implemented with octagonal gate and standard layout styles. The OCTO SOI MOSFET demonstrates to be capable to present a higher TID tolerance and to maintain active the LCE and PAMDLE effects after the X-ray radiation exposure, taking into account the I_{ON}/I_{OFF} ratio and drain current in both operation regions (Triode and Saturation). As a remarkable result of this study, the OCTO layout style needs a smaller back-gate bias than the one observed in the CSM (standard device) to reestablish its pre-rad conditions of its parameters and figures of merit (V_{TH} and I_{DS}), which were analyzed by this work. These findings indicate that the Octagonal layout style for MOSFETs can be considered an alternative device to be used in space and medical ICs applications operating in radiation environment, without causes any extra cost for the current planar CMOS ICs manufacturing processes.

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