

Gate-Oxide Voltage Overstress Treatment in Charge Pump Circuits for Standard CMOS Technologies

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ABSTRACT

Charge pump circuits operating at voltage levels above that of the power supply usually suffer from gate-oxide voltage overstress. Such reliability problem has become a concern especially as the gate-oxide thickness is scaled down. Devising charge pump circuits that avoid such a problem is far simpler for CMOS triple-well technologies than for standard technologies, nevertheless fabrication costs are higher. Two approaches are usually applied to eliminate gate-oxide overstress in charge pumps designed for standard CMOS technologies, the first is multiple phase control, and the second is dual phase control with doubled voltage swing. The latter has been shown to produce more power efficient circuits, however solutions using such approach still present gate-oxide overstress in some transistors. In this work, it is shown that a slight change in some of the circuit connections is able to ultimately overcome the problem. Moreover, experimental results have shown that such circuit topology can reach a voltage multiplication efficiency of about 98 %.

Index Terms: charge pump, voltage overstress, low power, reliability

I. INTRODUCTION

Charge pump circuits are devised for a variety of applications including energy harvesting, RFID power supply, data recording of flash and EEPROM memories, hard reset operation for CMOS imagers, applications in systems embedding MEMS devices, and phase-locked loops. Whether it uses a low voltage power supply or a regular V_{DD} power supply, the main goal of these circuits is to deliver a voltage output higher than that of the power supply.

Owing to its simplicity the Dickson charge pump [1] is the main topology applied to applications where only very low voltage power supplies are available, such as in energy harvesting [2]. However, in applications where the regular V_{DD} power supply can be employed, the Dickson topology presents poor voltage multiplication efficiency compared with other topologies devised for the same purpose. This happens because the body effect increases the threshold voltage of the NMOS transistors of the circuit. Moreover, when the voltage difference between consecutive stages reaches $2V_{DD}$ the gate-oxide of some of its MOS transistors are subject to gate-oxide voltage overstress

[3]-[8]. The gate-oxide of a MOS transistor is said to be overstressed when the voltage difference between the gate and any other terminal is higher than that of the power supply V_{DD} .

Gate-oxide voltage overstress greatly reduces MOS devices' lifetime [9]. Therefore, it has become a concern for charge pump circuits. The problem is especially worse for new technologies, as the gate-oxide thickness is scaled down [10]. In the literature, it is found a number of designs, for standard CMOS technology, clamming to eliminate the problem [11]-[15]. However, as it will be shown, solutions which require four or six phases signal control to operate [10]-[12] consume more power than those requiring only dual phase control. Using CMOS triple-well technology is quite easy to design charge pumps without such problem [9], [14]-[15], nevertheless fabrication costs are increased. The solutions presented in [14]-[15] employ dual phase control, are devised for standard CMOS technologies, and claim to overcome gate-oxide voltage overstress. Notwithstanding, as will also be shown, it does not completely eliminate the problem.

The weakness of the solutions [14]-[15] was pointed out in [16], where an alternative solution was

proposed. The circuit solution proposed in [16] really overcomes gate-oxide voltage overstress, notwithstanding it is done at the cost of reduced voltage multiplication efficiency. Such problem will be explained in the next section.

In order to truly overcome overstress while keeping a high voltage multiplication efficiency, slight changes in the connections of the circuits presented in [14] are proposed herein.

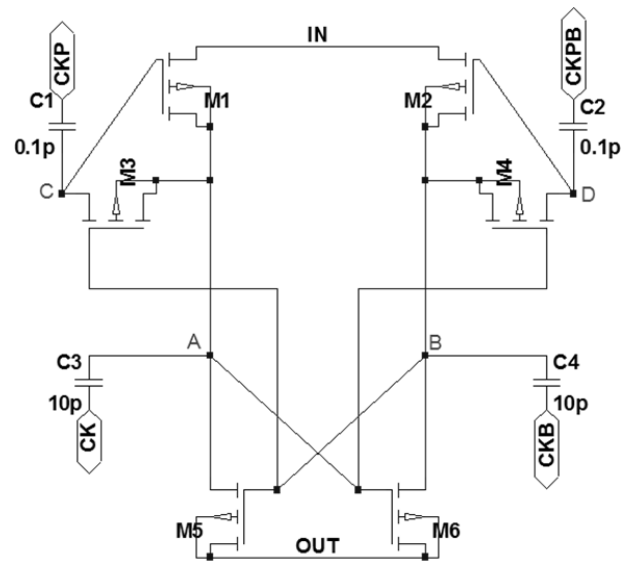
The charge pump circuits with the proposed changes to overcome overstress together with simulation results will be presented in the next section. Then experimental results showing the circuit performance will be presented in section III, followed by drawn conclusion in section IV.

II. OVERSTRESS TREATMENT

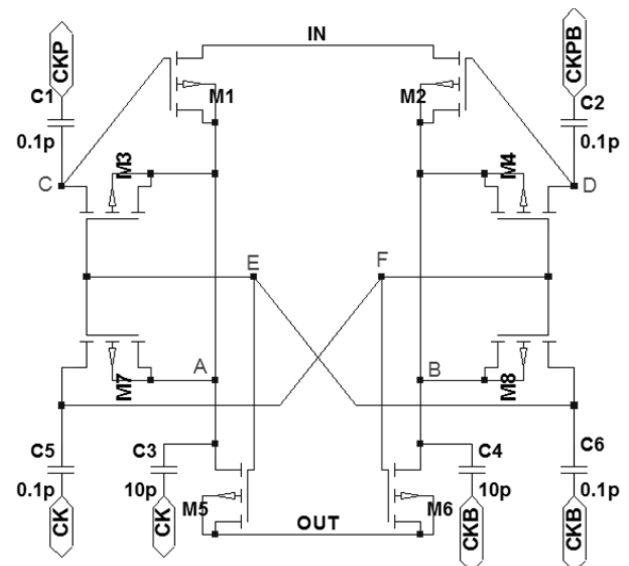
The two charge pump circuits proposed in [14], claiming to overcome gate-oxide voltage overstress, are presented in fig. 1(a) and (b) respectively. In addition to its main function, the circuit presented in fig. 1(b) features reduced on-resistance of its output transistors M5 and M6 as explained in [14], what makes it a faster than the circuit in fig. 1(a). More on this feature will be discussed with the experimental results. However, a basic analysis of the operation of these circuits shows that the transistors M3 and M4 of both circuits still present the overstress problem.

These circuits are driven by four different control signals CK, CKB, CKP and CKPB which scheme are shown in fig. 2. The control signals are applied to nodes indicated by the same labels in the circuits of fig. 1(a) and (b). The signals CKP and CKPB are respectively in phase with CK and CKB, and in counter phase with each other. The rise and fall times of these control signals ought to be as short as possible to avoid charge leakage. In this scheme the signals CK and CKB, as well as the signals CKP and CKPB must cross at 50 % of the swing between the low and high levels respectively. Moreover, the control signals CKP and CKPB have double voltage swing, which are generated by a dedicated circuit presented in [14].

The problem appears when the gate-oxide is subject to a voltage higher than V_{DD} . In the circuit of the fig. 1(a) when CKP is in low level and CKB is in high level, the voltage difference between nodes B and A will be V_{DD} and the voltage difference between nodes C and A will be $-V_{DD}$, therefore $V_{GD, M3}$ that is the voltage difference between nodes B and C reaches $2V_{DD}$. When the phase turns the voltage difference between nodes A and B will be V_{DD} and the voltage difference between nodes D and B will be $-V_{DD}$, therefore $V_{GD, M4}$ that is the voltage difference between nodes A and D reaches $2V_{DD}$.



(a)



(b)

Figure 1. (a) Charge pump circuit proposed in [14]; and (b) Charge pump circuit proposed in [14] with reduced on-resistance of transistors M5 and M6.

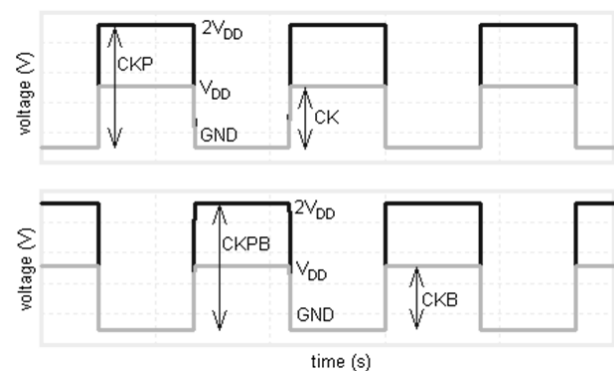


Figure 2. Control signal scheme for the circuits in fig. 1(a) and 1(b).

The same problem appears in the circuit of the fig. 1(b), when CKP is in low level and CKB is in high level, the voltage difference between nodes E and A will be V_{DD} and the voltage difference between nodes C and A will be $-V_{DD}$, therefore $V_{GD,M3}$ that is the voltage difference between nodes E and C reaches $2V_{DD}$. When the phase turns the voltage difference between nodes F and B will be V_{DD} and the voltage difference between nodes D and B will be $-V_{DD}$, therefore $V_{GD,M4}$ that is the voltage difference between nodes F and D reaches $2V_{DD}$. Under these conditions, the transistors M3 and M4 of both circuits will be subject to gate-oxide overstress.

In order to overcome gate-oxide voltage overstress the solution presented in [16] proposed a swing scheme for CKP and CKPB different from that in fig. 2. Basically it proposes that instead of swinging from GND to $2V_{DD}$, both signals swing from V_{DD} to $2V_{DD}$. Such approach really overcomes the overstress problem, however it increases the on-resistance of the input transistors M1 and M2 in both circuits. This effect reduces the voltage multiplication efficiency of the circuit, as will be shown in the simulation results.

The solution presented next shows that the problem can be promptly eliminated by a slight change in some specific connections of the circuits in fig. 1(a) and (b).

A. The Proposed Solution

To eliminate gate-oxide overstress in the circuits of fig. 1(a) and (b) this work proposes changing the gate connection of transistors M3 and M4 of both circuits as follows: in the first circuit the gate terminals of transistors M3 and M4 are disconnected from the nodes A and B, respectively, and both reconnected to the node IN, resulting in the circuit shown in fig. 3(a). The same approach is applied to the second circuit where the gate terminals of transistors M3 and M4 are disconnected from the nodes E and F, respectively, and both reconnected to the node IN, resulting in the circuit shown in fig. 3(b).

The circuits with the new proposed connections make use of the same voltage doubler circuit employed in [14] to produce the signals CKP and CKPB. It is necessary to point out that the circuit solution in fig. 3(a) presents the same circuit structure presented in [11]. Nevertheless, the operation of the circuit structure presented in [11] requires a four-phase control signal, whereas the present solution requires only two-phase control signal to operate.

In order to assert the ability of the proposed circuits to eliminate gate-oxide overstress, where the former solutions failed, the following analysis is performed: in the circuit of the fig. 3(a) when CKP is in low level and CKB is in high level, $V_{GD,M3}$ that is

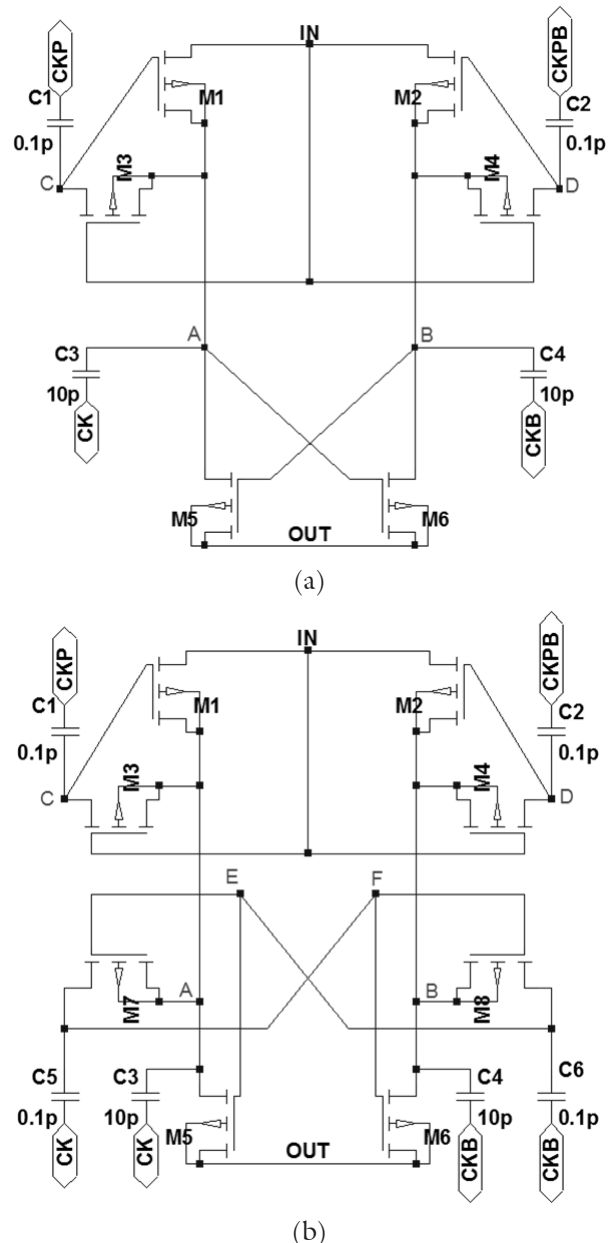


Figure 3. (a) Charge pump circuit with the proposed gate connections for the transistors M3 and M4; and (b) Charge pump circuit with reduced on-resistance of transistors M5 and M6, and with the proposed gate-connections for the transistors M3 and M4.

the voltage difference between nodes IN and C reaches only V_{DD} , when the phase turns $V_{GD,M4}$ that is the voltage difference between nodes IN and D reaches only V_{DD} and thus the problem is indeed overcome. The same steps can be applied to verify that the problem is also overcome with the circuit of fig. 3(b).

The only difference between the circuits with the proposed connections and those presented in [14] is the ability to overcome overstress. The operation of the circuits in fig. 3(a) and 3(b) is exactly the same as that of those in fig. 1(a) and 1(b). Hence the proposed circuits inherit some interesting features of the circuits

presented in [14] and [15] as efficient voltage multiplication and improved power efficiency. The performance of the proposed solutions is asserted by simulation and experimental results.

B. Simulation Results

Purposefully to assert the ability of the proposed circuits to eliminate overstress, as well as to compare their performance against each other, and also against the former solution presented in [14], BSIM3v3 simulations were performed with the four charge pump circuits shown in figs. 1 and 3 and also with that presented in [16]. The five circuits were designed for a standard 4-metal 2-poly CMOS 0.35 μ m technology. All the input and output transistors M1, M2, M5, and M6 of the five charge pump circuits have the same dimensions $W = 1.40 \mu\text{m}$ and $L = 0.35 \mu\text{m}$. All other auxiliary transistors of these circuits have dimensions of $W = 0.50 \mu\text{m}$ and $L = 0.35 \mu\text{m}$. In the circuits of fig. 1(a) and 3(a), the capacitance of C1 and C2 is 0.1 pF and the capacitance of C3 and C4 is 10 pF, and in the circuits of figs. 1(b) and 3(b) the capacitance of C5 and C6 is 0.1 pF.

The charge pump circuit employed in [16] is similar to that of fig. 1(a), however it implements body-bias scheme in the input transistor M1 and M2 as the solution proposed in [17]. The schematic diagram of the charge pump circuit of the solution [16] is presented in fig. 4. The dimensions of the four body-bias transistors M_{b1} , M_{b2} , M_{b3} and M_{b4} are $W = 0.50 \mu\text{m}$ and $L = 0.35 \mu\text{m}$.

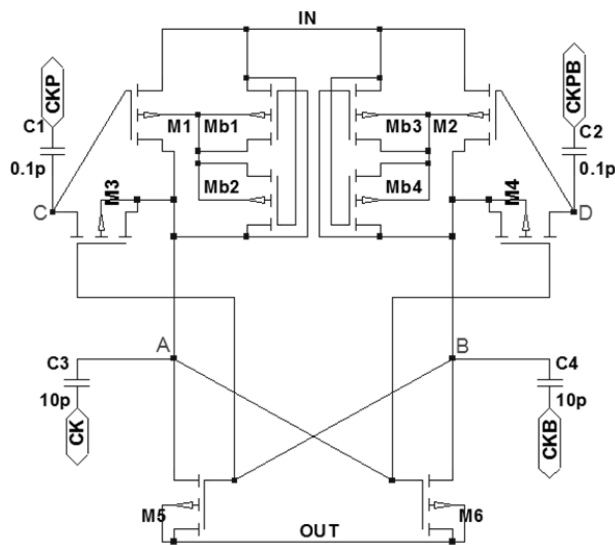


Figure 4. Charge pump circuit proposed in [16] similar to that of fig. 1(a), employing body-bias in the input transistors M1 and M2 as that proposed in [17].

Each of the five circuits is simulated with the four-stage charge pump scheme shown in fig. 5. The following test setup is applied: V_{DD} is 3.3 V, the output capacitance C_{out} is 100 pF, and the control signal scheme shown in fig. 2 is generated from a sole signal CK with 1 MHz, duty cycle of 50 %, high voltage level of 3.3 V, low voltage level equals GND, and rise and fall times of 1ns. The control signal CKB was generated by the inverter shown in fig. 6(a) with (W/L) dimensions of (8.0 μm / 0.35 μm) for the PMOS transistor and (4.0 μm / 0.35 μm) for the NMOS transistor. It is important to point out that ideally the minimal CK voltage swing for this circuit to operate properly is the threshold voltage of the PMOS transistors. Experimental verifications have shown that the minimal CK voltage swing might be above the PMOS threshold level.

The signals CKP and CKPB were generated by the circuit shown in fig. 6(b), which is the same circuit presented in [14], where the transistors M1, M2, M4 and M6 have dimensions $W = 0.50 \mu\text{m}$ and $L = 0.35 \mu\text{m}$, the transistors M3 and M5 have also dimensions $W = 0.50 \mu\text{m}$ and $L = 0.35 \mu\text{m}$, the capacitance of C1 and C2 is 1.0 pF.

The terminals CKP and CKPB of the circuit in fig. 4 are driven by the signals generated in the nodes CKP-X and CKPB-X of fig. 6(b). This procedure is exactly the solution proposed in [16].

The plot of nodes A and C of the second stage of the charge pumps of fig. 1(a) and (b) are shown in

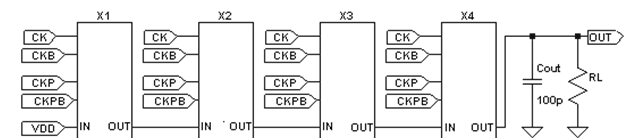


Figure 5. Four-stage test bench schematic

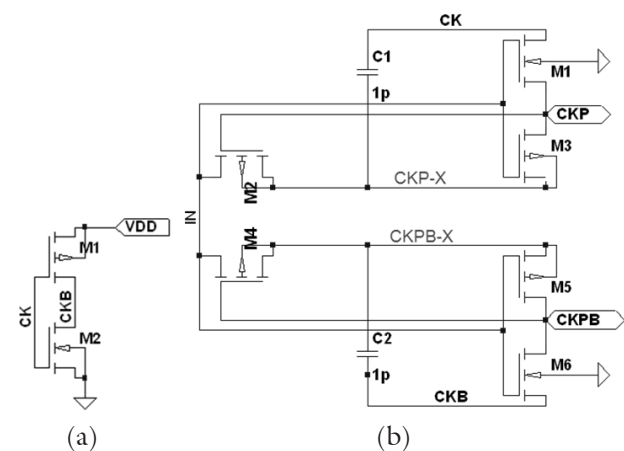


Figure 6. (a) Inverter; and (b) voltage doubler circuit.

fig. 7(a) and (b), respectively. In both circuits when the signal of node C is in high level the voltage difference between nodes A and C reaches just V_{DD} , but when it is in low level the voltage difference between nodes A and C reaches $2V_{DD}$. The overstress happens only during half period in each transistor M3 and M4, notwithstanding it shall accelerate circuit aging, reducing its lifetime [9]. During signal switching, overstress due to transient pulses can be found all over the circuit, notwithstanding pulses with long duration are more harmful to the oxide of MOS transistors than those of short duration [21].

The plot of nodes A and C of the second stage of the charge pumps of fig. 3(a) and (b) are shown in fig. 8(a) and 8(b). In both circuits when the signal

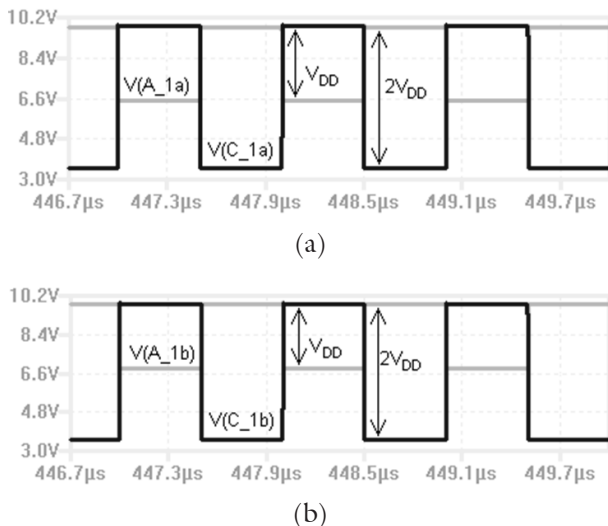


Figure 7. a) Plot of nodes A and C of the second stage of the first circuit of [14]; and (b) of the second circuit of [14].

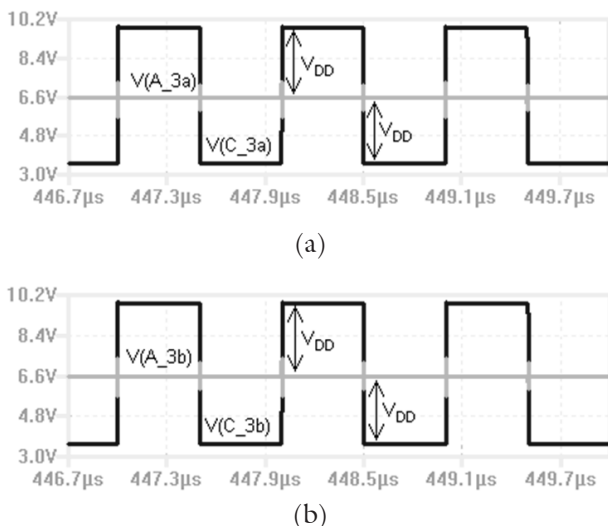


Figure 8. (a) Plot of nodes A and C of the second stage of the circuit with the proposed connections in fig. 3(a); (b) and of the circuit with the proposed connections in fig. 3(b)

of node C is in either high or low level the voltage difference between nodes A and C reaches just V_{DD} . Therefore, as expected the transistors M3 and M4 of these circuits are free from gate-oxide overstress.

According to [9], it is also expected that the proposed circuits shall have longer lifetime than those of the former solutions, nevertheless only careful and time consuming characterization can assert such expectation.

Besides overcoming the overstress problem, simulation results show no significant difference between the performances of the four charge pump circuits presented in fig. 1 and fig. 3. However, as the output reaches the highest voltage level, the performance of the charge pump of the solution proposed in [16] is jeopardized by the increasing of the on-resistance of the input transistors M1 and M2 of the circuit in fig. 4.

The increasing of the on-resistance of M1 and M2 in fig. 4 happens because as the output reaches the highest voltage level, during charge phase of C3 and C4, $V_{GS, M1}$ and $V_{GS, M2}$ become lower than V_{TH} . This problem is reduced when the output current load increases, in this case the output voltage of the circuit in fig. 4 reaches the level of the output of the circuits in fig. 1 and fig. 3. Such behavior is shown by the simulation results presented in fig. 9.

The voltage output of each of the four-stage charge pump circuits without current load are shown in fig. 9(a), and with output current load produced by resistances of 1000 K Ω and 200 K Ω are shown in figs. 9(b) and 9(c) respectively.

The ideal output voltage level of each stage is the voltage level of its input node IN plus the total swing voltage level of the signal CK. In this case the total swing voltage level of the signal CK is V_{DD} , and the input voltage level of node IN of the first stage is also V_{DD} . Therefore, each four-stage charge pump would ideally, without current load, deliver an output of 16.5 V that is $5V_{DD}$. The factor 5 is the circuit ideal voltage multiplication value.

The four-stage charge pumps circuits using the topologies of fig. 1 and fig. 3, under the described simulation conditions, presented voltage multiplication efficiency of about 99.4 % of its ideal level. On the other hand, the circuit using the solution proposed in [16] presented a voltage multiplication efficiency of about 83.4 %.

The rise time is defined as the space of time required by the output of the circuit to go from 10 % to 90 % of the final output voltage level. Under the described simulation conditions, the four-stage charge pumps built with the circuits of fig. 1 and fig. 3 present a rise time of about 59 μ s. However, experimental results show that these circuits present a much longer rise time, as it will be shown in the next section.

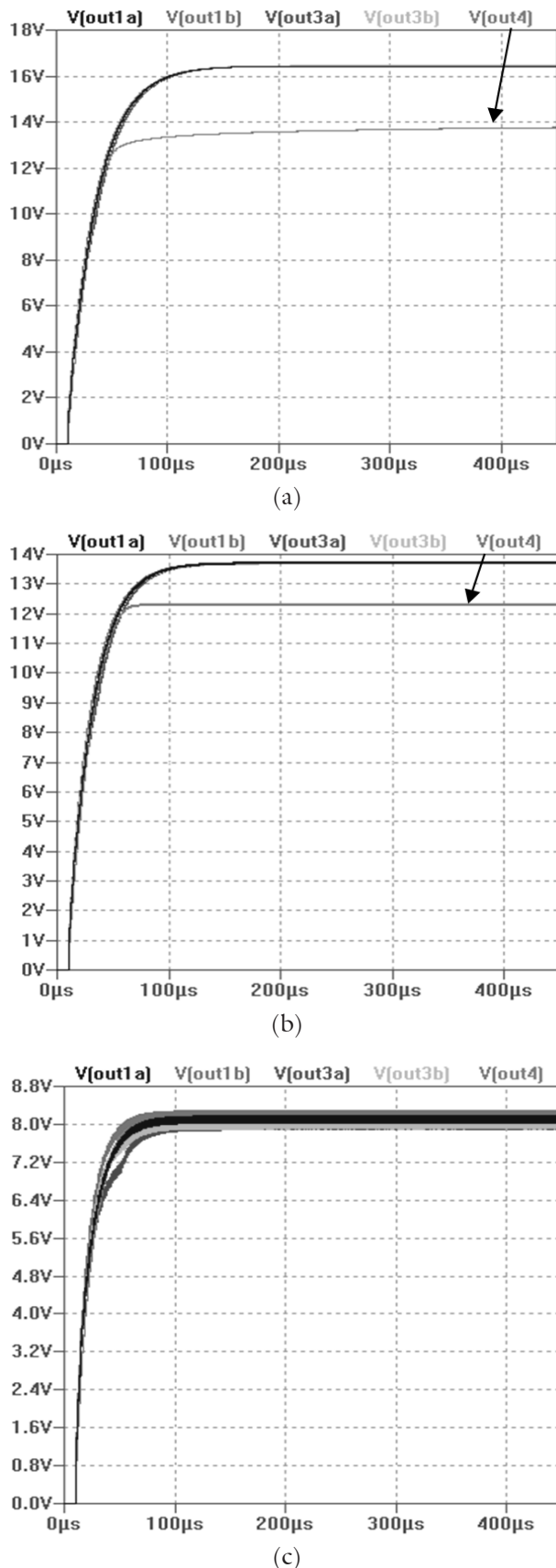


Figure 9. Fig.9 Four-stage voltage output simulations for the five charge pump circuit (a) without load; (b) with a 1000 K Ω output resistance; and (c) with a 200 K Ω output resistance

Under current load condition, as shown in figs. 9(b) and 9(c), the output voltage of the circuits in fig. 1 and fig. 3 is reduced from 16.4 V to 13.7 V and 8.0 V respectively. On the other hand, the output voltage of the circuit in fig. 4 is reduced from 13.76 V to 12.3 V and 8.0 V respectively. Below 12 V the problem presented by the solution [16] is reduced and the five charge pump circuits assume almost the same output level.

The use of the dual phase control signal to drive the proposed circuits, instead of the four-phase scheme proposed in [11], and the six-phase scheme proposed [12], confers them lower power consumption, as discussed in [15]. For instance, without output current load, the simulated power consumption of the four-stage circuits of fig. 1 and fig. 3 together with the power consumption of the circuit that generates the control signal is lower than 6.5 μW . Whereas those circuits requiring multiple-phase control signal [11] and [12] present power consumption higher 23.5 μW and 26.5 μW respectively.

To keep the voltage multiplication efficiency as high as possible under higher output current load conditions, one can either increase the frequency of the signal CK or increase the pump capacitance C3 and C4 of either charge pump circuits.

III. Experimental Results

The experimental results herein presented were acquired from the characterization of two four-stage charge pump circuits using the topologies presented in fig. 1(a) and 1(b) respectively. As shown in the previous section, the only difference between these topologies and those in fig. 3(a) and 3(b) is the ability to overcome gate-oxide overstress, all other characteristics of these circuits are similar.

The layout of the two four-stage charge pump circuits using the topology shown in fig. 1(a) and fig. 1(b), together with the voltage doubler circuit of fig. 6(b), are presented in figs. 10(a) and 10(b) respectively. These circuits were designed and fabricated in the AMS standard 4-metal 2-poly 0.35 μm CMOS technology. The dimensions of the transistors and capacitors of the circuits are the same employed to perform the simulations. The micrograph of the two fabricated four-stage charge pumps is shown in fig. 11.

The characterization of the two charge pumps were performed using the following equipment and setup: as the power supply, an MPC 3003D with a VDD level of 3.2 V was employed; the CK signal was generated with an HP 8130A, using a frequency of 1 MHz with rise and fall times of 1 ns; the transient captures were made with an scope TDS 460A; and the steady state voltage levels were measured with an HP 3458A.

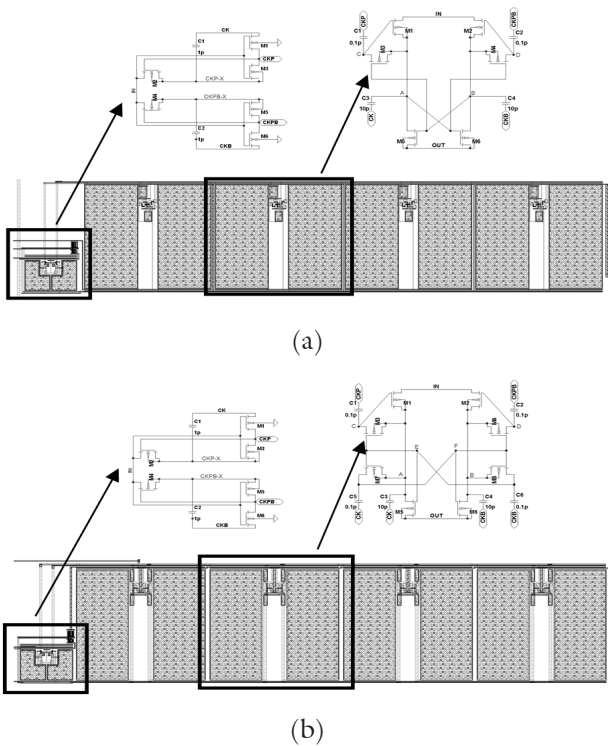


Figure 10. (a) Layout of the four-stage charge pump circuit using the topology presented in fig. 1(a) with the voltage doubler circuit of fig. 6(b), both structures are indicated by the arrows; (b) Layout of the four-stage charge pump circuit using the topology presented in fig. 1(b) with the voltage doubler circuit of fig. 6(b), both structures are indicated by the arrows

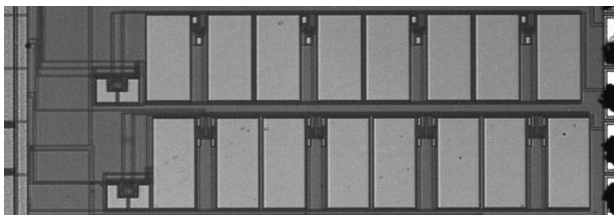


Figure 11. Micrograph of the two fabricated four-stage charge pump circuits

The measured rise time and the highest output voltage of both circuits when there is no output load are presented on the plots in fig. 12(a) and fig. 12(b).

Owing to the scheme described in [14] to reduce on-resistance of the output transistors M5 and M6 of the charge pump presented in fig. 1(b), the four-stage charge pump in fig. 10(b) presents a rise time of about 29 % shorter than that of the charge pump in fig. 10(a). This effect is perceived when the results of fig. 12(a) and 12(b) are compared. The reduced on-resistance effect of the charge pump in fig. 1(b) was hardly noticed in the simulations. Notwithstanding this effect was clear with the experimental results as predicted in [14].

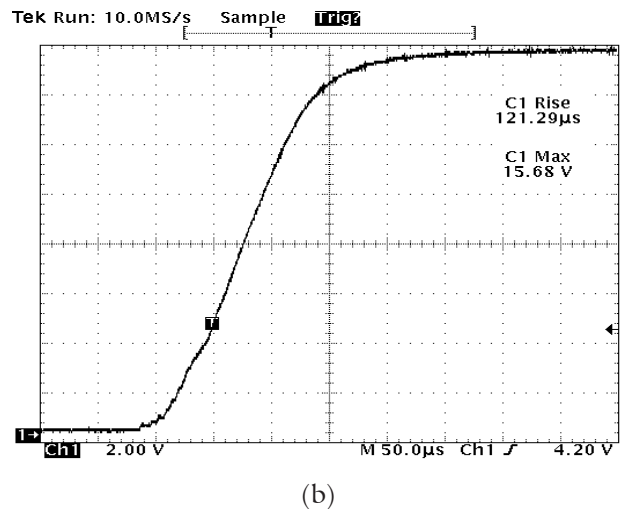
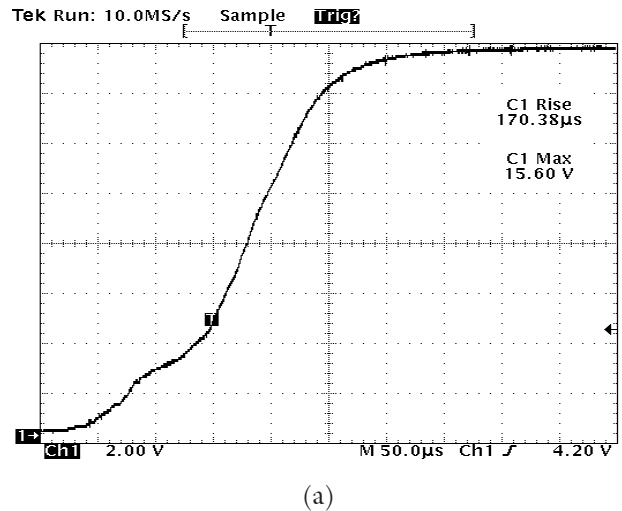


Figure 12. (a) Measured rise time and highest output voltage of the circuit of fig. 10(a); (b) Measured rise time and highest output voltage of the circuit of fig. 10(b)

When both circuits are without output load, the highest output voltage yielded by both circuits is almost the same, as predicted by the simulation results. In this configuration, with $V_{DD} = 3.2$ V, the voltage multiplication efficiency of both circuits is 97.5 % and 98 % respectively. This is less than 2 % smaller than the voltage multiplication efficiency predicted by the simulations.

The output voltage of both circuits when they are under output current load is presented in fig. 13. These results show that as the current load increases, the output voltage is reduced. When the output voltage falls below about 9.5 V, which for this frequency of operation is reached with an output current load of about 20 μ A, the voltage output falls straightly to the ground level. This seems to be a kind of latch-up effect due to a quite large current flowing into the body of the PMOS transistor, as predicted in [17].

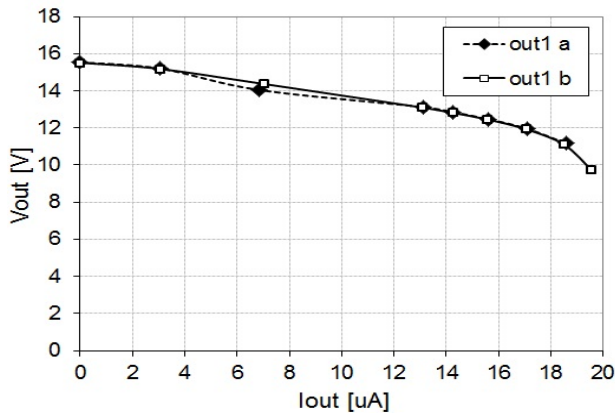


Figure 13. Output voltage vs current load of the circuits in fig. 10.

IV. CONCLUSIONS

In this work it was proposed a slight change for some connections of two double-path charge pump circuits so that they would be free from gate-oxide overstress. The proposed solution is applied to circuits which require only two-phase control signal scheme to operate. The circuits show voltage multiplication efficiency compliant to those presented in the literature. The relevancy of the proposed solution lies in the ability to overcome gate-oxide overstress, and therefore restraining precocious circuit failure due to accelerated aging process that reduces the circuit lifetime. The circuits employed in this work present improved power efficiency in relation to previous topologies which require multiple-phase control signal. Experimental results asserted the high multiplication efficiency of the circuits, and also the rise time improvement in one of the topologies employed in this work. Moreover, the proposed charge pump circuits are general solutions for any CMOS technology.

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