A 2-Transistor Sub-1V Low Power Temperature Compensated CMOS Voltage Reference: Design and Application

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ABSTRACT

This paper presents the design and application of a CMOS sub-1V voltage reference using a 2-transistor Self-Cascode MOSFET (SCM) structure able to get low power consumption, temperature compensation, and small area. An efficient design procedure applied to this simple topology relying on NMOS transistors with different threshold voltages allows attaining large immunity against bias current and supply voltage variations. The two transistors can operate in weak, moderate, or strong inversion making the design flexible in terms of area and power consumption. Implemented in a > 0.18μm standard CMOS technology, the circuit provides a 400mV voltage reference with a variation of ±0.18% from -20°C to 75°C (or less than 15ppm/°C), operates from 3.6V down to 800mV while biased with a 5nA resistor-less PTAT current source that varies ±30% over PVT, and consumes less than 20nA with an area of 0.01mm^2. The same concept was used to create a temperature compensated voltage drop with regard to a monitored power supply voltage but using a 2-PMOS SCM structure with transistors of different threshold voltages. These two circuits were adopted as part of a Power Management (PM) system for RFID tag applications. The PM includes a LDO voltage regulator and a low voltage detector that require both the voltage reference and the low voltage monitor. The LDO regulated output voltage and the trip-point of the voltage detector vary +/-5.5% and +/-3.3%, respectively, over temperature, without trimming.

Index Terms: Low power, low voltage, temperature compensated voltage reference, CMOS integrated circuit design, LDO voltage regulator, low voltage detector.

I. INTRODUCTION

Robust low-power voltage references are crucial to properly bias analog circuits with a well-defined, very stable signal over process, temperature, and power supply variations. Aligned with current technologies trends, these circuits should be small in area and able to operate with low voltage and low power constraints, especially for portable and RFID applications. Furthermore, efficiency, simplicity, easy-to-design analog circuit structures compatible with VLSI technologies are highly desirable [1-2]. In this scenario, new circuit approaches such as the one described here are highly desirable.

Methodologies for CMOS analog design based on the concept of inversion level have been shown to provide a very solid alternative for high performance in very low power and low voltage circuits [3-4-5]. Such design techniques, that adopts the current as the main design variable, has been widely employed to develop voltage and current references as well as temperature detection circuits as described in [6-7].

This paper presents the design of a new sub-1V, low power, low voltage, temperature compensated (i.e., ZTAT) voltage reference using the technology-independent inversion level methodology described in [6-8]. The simple circuit relies on a Self-Cascode MOSFET (SCM) structure implemented using 2 NMOS transistors with different threshold voltages, devices that nowadays are usually available in many standard CMOS processes. These two transistors can operate in weak, moderate, or strong inversion saturation making the design flexible in terms of area and power consumption. Implemented in a 0.18μm standard CMOS process, the circuit provides a 400mV voltage reference with a variation of less than 15ppm/°C from -20°C to 75°C (or ±0.18%), operating from 3.6V down to 800mV.

The same idea was used to create a temperature compensated voltage drop with regard to a monitored power supply voltage but using a 2-PMOS SCM structure with transistors of different threshold voltages.

These two circuits were adopted as part of a Power Management (PM) system that includes a 5nA

resistor-less PTAT current source, a series LDO voltage regulator and a low voltage detector. This PM system is the analog front end (AFE) core of a low frequency (LF) RFID tag [9].

This paper is organized as follows: in Section II, the Advanced Compact Model (ACM) and the concept of inversion level are summarized. The design procedure for the temperature compensated voltage reference using an NMOS SCM structure is presented in Section III. Section IV describes the circuit application in the PM system, addressing its main features. Experimental results are reported in Section V. Finally, our conclusions are summarized in Section VI.

II. THE ACM MODEL

The ACM model, a current-mode MOSFET model that applies the concept of inversion level [3-4], provides continuous analytical functions for the transistor current from weak to strong inversion. According to the ACM model, the drain

current can be split into the forward (I_F) and reverse (I_R) currents:

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{1}$$

where:

$$I_S = I_{SQ}(W/L) = I_{SQ}(S) \tag{2}$$

$$I_{SQ} = \mu C'_{ox}\, n \frac{\phi_t^{\,2}}{2} \tag{3}$$

I_F (I_R) depends on the gate and source (drain) voltages. In forward saturation $I_F >> I_R$, so $I_D \approx I_F = I_S \cdot i_f$. Note I_S is the normalization current, I_{SQ} is the sheet specific current, i_f (or i_r) is the forward (or reverse) inversion level, and μ, C_{ox}, n, ϕ_t, and S are, respectively, the mobility, gate oxide capacitance per area, slope factor, thermal voltage and transistor aspect ratio (W/L).

In the ACM model, the relation between current and voltage is given by [3-4]:

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right) \tag{4}$$

where:

$$V_P \cong \frac{V_{GB} - V_{T0}}{n} \tag{5}$$

is the pinch-off voltage related to V_{GB}, the gate-to-bulk voltage, and V_{TO}, the zero bias threshold voltage.

III. THE ZTAT VOLTAGE REFERENCE USING A TRANSISTOR SCM WITH DIFFERENT THRESHOLD VOLTAGES

The association of M1 and M2 transistors in Figure 1, which is called here the Self-Cascode MOSFET (SCM) structure, is the core of the ZTAT voltage reference. As will be seen next, the SCM can perform as a ZTAT reference voltage for any inversion level providing the threshold voltage of M1 (V_{TH1}) is larger than that of M2 (V_{TH2}), and driving both transistors to operate in saturation.

The voltage reference $V_{ref} = V_X$ can be easily found assuming M2 is working in weak inversion. In this case $V_{GB1} = V_{GB2} = V_{GB}$, and V_X voltages are giving respectively by (see Figure 1):

$$V_{GB} \approx V_X + V_{TH2} \tag{6}$$

$$V_X = V_{DS1} = V_{SB2} - V_{SB1} \tag{7}$$

In (7), V_{SBi} is the source-to-bulk voltage of transistor i.

Using (4)-(7), V_X reduces to:

$$V_X = \zeta V_{TH1} - \gamma V_{TH2} + k\phi_t \tag{8}$$

where the parameters ζ, γ, β, and C are defined as:

$$\zeta = \frac{1}{(1-\beta)n_1} \tag{9}$$

$$\gamma = \frac{1-\beta n_2}{(1-\beta)n_2} \tag{10}$$

$$\beta = \frac{n_1 - n_2}{n_1 n_2} \tag{11}$$

$$k = \left[\sqrt{i_{f1}+1} - \sqrt{\alpha i_{f1}+1} + \ln\left(\frac{\sqrt{i_{f1}+1}-1}{\sqrt{\alpha i_{f1}+1}-1}\right)\right] \tag{12}$$

Note that, in (12), parameter α is the ratio between the forward inversion levels of transistors M1 and M2 given by:

$$\alpha = \frac{i_{f2}}{i_{f1}} = \frac{I_{SQ1}S_1}{I_{SQ2}S_2}\left(\frac{N}{N+1}\right) \tag{13}$$

with factor N defined by the gain of a PMOS current mirror, as illustrated in Figure 1.

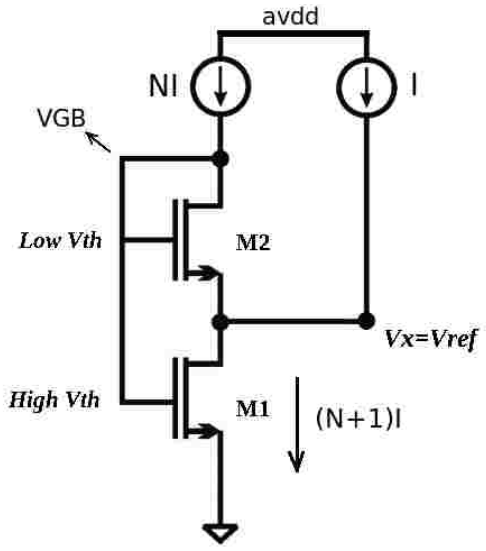

Figure 1. The SCM structure build with saturated NMOS transistors of different threshold voltages ($V_{TH1} > V_{TH2}$).

Eq. (8) shows V_X depends on the threshold voltage difference of transistors M1 and M2, as well as on the thermal voltage ϕ_t. It is well known that the MOS threshold voltage has a CTAT (Complementary-to-Absolute Temperature) behavior whereas the thermal voltage is PTAT (Proportional-to-Absolute Temperature). So, assuming that $V_{TH1} > V_{TH2}$, the 2-T SCM voltage reference in Figure 1 can be designed to have the PTAT and CTAT components cancelling each other in temperature.

After finding the voltage reference temperature dependence ($\partial V_X/\partial T$) and neglecting the variation with temperature of the slope factors n_1 and n_2 (i.e., $\partial\zeta/\partial T = 0$, $\partial\gamma/\partial T = 0$, and $\partial\beta/\partial T = 0$), one can find the parameter k that allows to compensate V_X over the temperature range ($\partial V_X/\partial T = 0$):

$$k = \frac{\gamma \frac{\partial V_{TH2}}{\partial T} - \zeta \frac{\partial V_{TH1}}{\partial T}}{\frac{\partial \phi_t}{\partial T}} \tag{14}$$

For a given fabrication process, (14) indicates the factor C that adjust the PTAT portion of (8) to counterbalance the CTAT components associated to the NMOS threshold voltages, to get a temperature compensated voltage reference.

Note that typically in a standard CMOS process, $\partial V_{THi}/\partial T$ ranges from -0.6mV/°C to -2.2mV/°C while $\partial\phi_t/\partial T$ equals to +85 μV/°C. Figure 2 is a plot of parameter k vs. i_{f1} for several values of α as in (13). The black line is the k value to get compensation in temperature. Using the k value obtained from (14) and choosing a given α, one can find the inversion factor i_{f1}. Then, from (13) it is possible to calculate i_{f2} and, finally, S_1 and S_2. It is important to mention that points above the k value will result in a PTAT voltage reference, whereas points below it will yield a CTAT one.

Although (8) has been derived assuming M_2 in weak inversion, the results still can be considered a good start point for the design methodology. Small adjustments using CAD tools are then necessary when

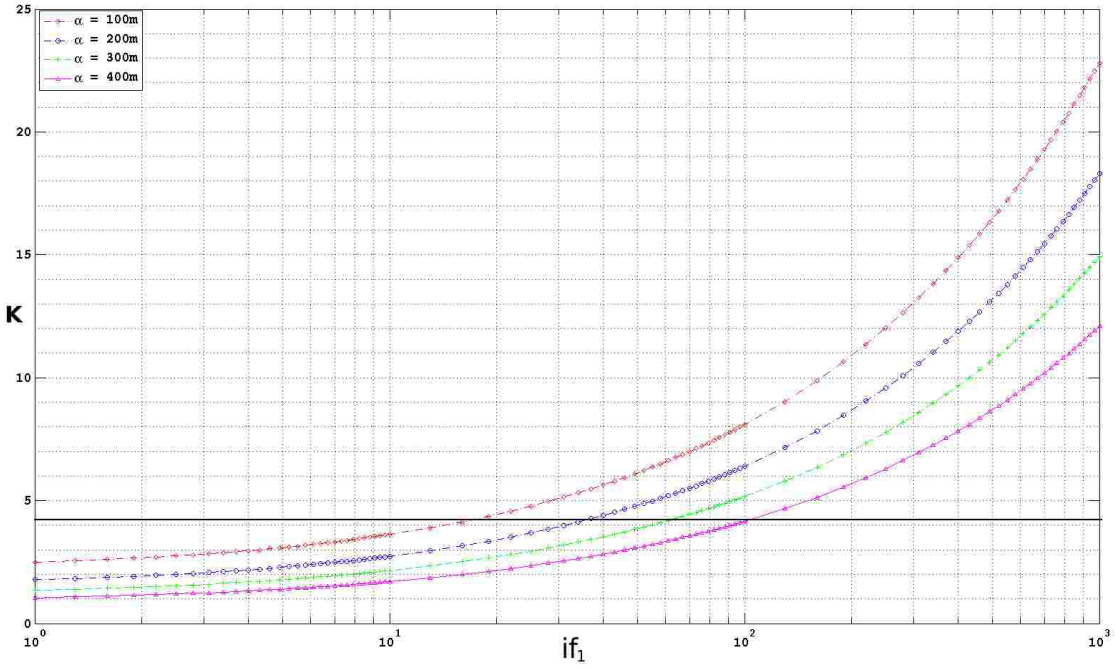

Figure 2. Parameter k versus inversion factor if1 for several values of α.

biasing the upper MOSFET (M_2) in moderate or strong inversion.

Note that (8) can result in a negative V_x (V_{DS1}), depending on V_{THi}, n_i, $\partial V_{THi}/\partial T$. However, parameter k, from (12), can be adjusted to result in a positive V_x ($\alpha > 1$ *or* $0 < \alpha < 1$).

IV. APPLYING THE ZTAT VOLTAGE REFERENCE CIRCUIT IN A PM SYSTEM FOR RFID TAGS

The proposed voltage reference was applied in a power management (PM) system suitable for RFID tag applications [9]. The PM system is composed by the ZTAT voltage reference, a resistor-less current reference, a series LDO voltage regulator and a low voltage detector. The complete system is depicted in Figure 3.

The series low-dropout (LDO) voltage regulator scales down the input voltage (usually from rectifier/clamp stage) and provides a fixed supply for the system. The block is composed by an operational amplifier which uses a special compensation scheme [9], a PMOS output stage and a resistor ladder.

The voltage detector block is based on a low voltage, low power CMOS comparator which compares the output voltage of two SCM structures. One is the ZTAT voltage reference (ground referenced) and the second is a 2-T PMOS SCM structure with transistors of different threshold that generates a temperature compensated voltage drop with regard to the regulated output voltage (AVDD).

The design equations for the PMOS 2-T SCM are the same as for the ZTAT voltage reference but design parameters (threshold voltages, threshold voltages variation with temperature, and so on) were carefully chosen and estimated to get a low voltage trip-point in accordance with system requirements. By design, the low voltage trip-point was set to be 0.9V.

All blocks are supplied by a low power 5nA resistor–less PTAT current source circuit. The current reference [6] uses two SCM structures, each one composed by two NMOS devices with the same threshold voltage. Note that each SCM is biased in different inversion levels (weak and moderate).

This approach combines the use of SCM structures with the ZTAT voltage reference to achieve a fully CMOS architecture (without resistor, bipolar transistors or any special device) with low voltage, low power and reduced area.

V. EXPERIMENTAL RESULTS

We now present measurement results of a test chip where the PM system was implemented. All blocks were designed and processed in a standard 0.18μm CMOS process technology that provides MOS devices with different threshold voltages.

A. ZTAT voltage reference

The ZTAT voltage reference was measured directly on wafer using a semi-automatic probe station with thermal chamber and a B1500 parameter analyzer. First, the best combination for the PMOS current mirrors was experimentally determined (bias currents I and NI in Figure 1). A nested sweep for I and NI was done over temperature (at -20ºC, 0ºC, 25ºC, and 75ºC temperature points) from 10nA to 200nA with a 5nA step. The optimum combination found was I = 45nA and NI = 15nA.

Figure 4 illustrates the 400mV ZTAT voltage reference variation over temperature for such combination of bias currents. Note the circuit provides an average voltage reference of 405mV with a variation of ±0.18% or 14.63ppm/ºC, from -20ºC to 75ºC. Figure 5 shows the 2-T SCM voltage reference for 9 parts across the wafer and at 3 different temperature points (-20ºC, 25ºC and +75ºC). The 2-T SCM voltage reference varies from 382mV to 405mV across the wafer.

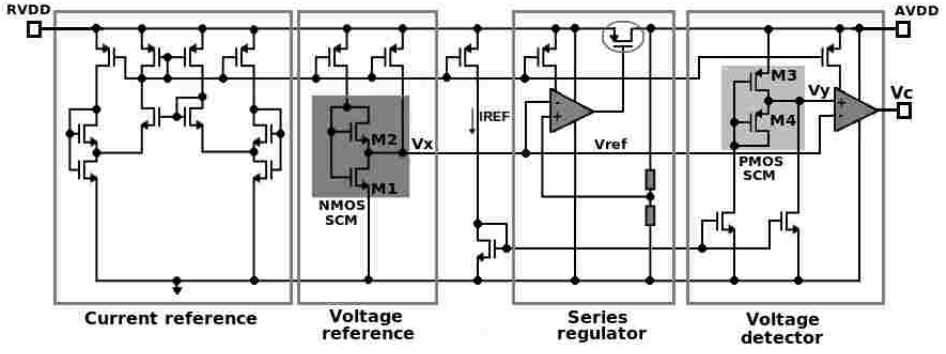

Figure 3. PM system suitable for RFID tags.

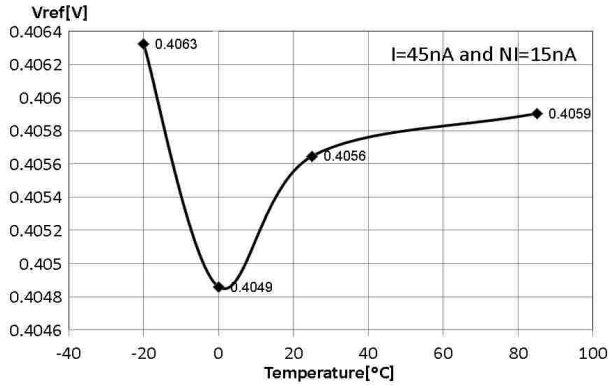

Figure 4. Voltage reference for the optimum PMOS bias currents combination.

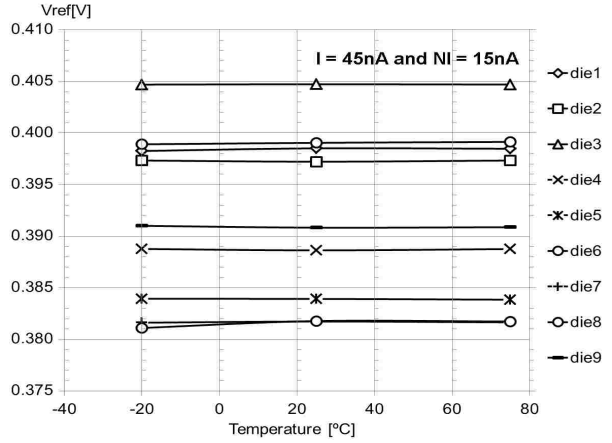

Figure 5. Voltage reference for 9 different samples across the wafer.

Table 1 shows the performance comparison of the 2-T SCM voltage reference against recently published voltage references in the literature. The comparison is done in terms of some design parameters. The thermal coefficient (TC [ppm/ºC]) of the present work is comparable to the state-of-the-art in the sub-1V voltage references arena. However, the big advantages of the present work are the circuit area and the fine control of the inversion level (IC Control) of the two transistors in the SCM. Due to the bias current scheme, a precise inversion coefficient level of the transistors in the SCM is achieved and a reduced area can be obtained as shown in Table 1.

Table 1. Performance comparison of voltage references.

Parameter	[10]	[11]	[12]	[13]	This work
V_{ref} [mV]	175	518	650	630	400
TC [ppm/ºC]	16.9	33	37	17	14.63
MinV_{DD} [V]	0.5	2.1	0.85	0.95	0.8
Power [W]	2.22p	4.6u	5.1n	10u	48n
LS [%/V]	0.033	0.1	1.35	n/a	n/a
Area [mm²]	0.00135	0.1	n/a	1.09	0.01
Tech [um]	0.13	0.4	0.18	0.5	0.18
IC Control	no	no	no	no	yes

The minimum power supply of the 2-T SCM voltage reference is given by the voltage reference itself plus 100mV to maintain the PMOS current mirrors in saturation (see Figure 1). Despite not measured, the line sensitivity (LS) parameter is comparable to the state-of-the-art since the circuit allows for large variations of the bias current.

B. Current reference

The 5nA current source was measured in 10 dies from different wafer corners (typical, best, and worst) at -20ºC, 25ºC and 85ºC. Figure 6 depicts its PTAT behavior demonstrating it varies ±30% over the temperature range. The measured part-to-part variation of the current source was ±20%.

Figure 7 shows the 400mV ZTAT voltage reference variation over temperature when biased by the same 5nA current source. The voltage reference circuit provides an average voltage reference of 380mV with a variation of 136ppm/ºC, from -40ºC to 85ºC.

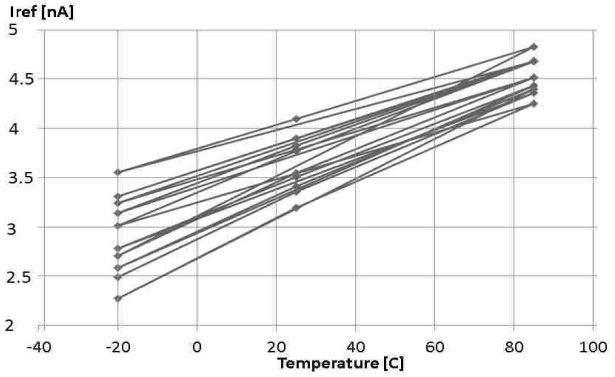

Figure 6. Resistor-less 5nA PTAT current source results over temperature.

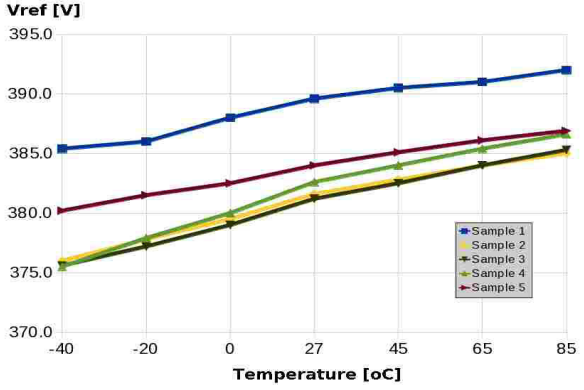

Figure 7. ZTAT voltage reference variation over temperature when biased by the same 5nA PTAT current source.

C. Voltage regulator

Figure 8 illustrates the regulated output voltage of the LDO regulator on 10 parts at -20ºC, 25ºC, and 85ºC, when varying the unregulated power supply voltage from 0V to 3.1V. The LDO employs the 400mV ZTAT voltage reference to generate a 1V regulated output voltage. Figure 8 validates the excellent behavior of the 400mV voltage reference over temperature despite the large variation of the current over both temperature and process (part-to-part disparity).

Note the overall regulated output voltage of the LDO is within ±5.5% including power supply, temperature, and process variation. Besides that, the extrapolated power consumption of the voltage reference circuit at hot (85ºC) was 20nA.

D. Voltage detector

Considering a supply sweep from 2 to 0V, the voltage detector circuitry was also tested. Experimental results indicate the low voltage detector trip-point (TP) is around 0.9V as expected by design.

The variation with temperature of the low voltage detector trip-point is shown in Fig. 9 for 3 samples from -40°C to +85°C. The average value is TP=0.9V and it varies around ±3.3% over temperature.

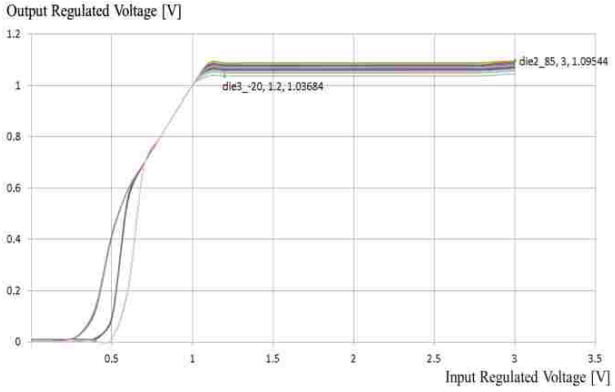

Figure 8. Regulated output voltage results.

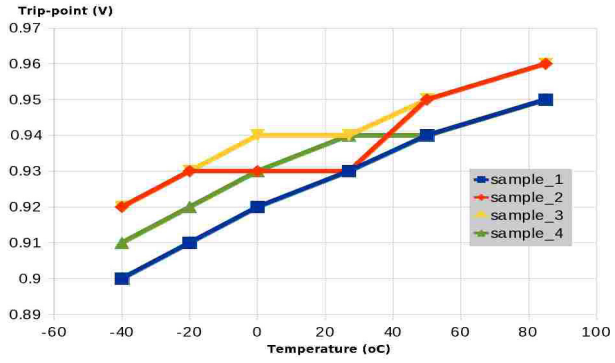

Figure 9. Voltage detector trip-point results over temperature.

VI. CONCLUSIONS

The design of a novel, simple sub-1V low power voltage reference using a 2-transistor SCM topology has been described. Design methodology based on ACM model using current as main design variable was detailed and successfully applied to develop a 400mV voltage reference. The same concept was used to create a temperature compensated voltage drop with regard to a monitored power supply voltage but using a 2-PMOS SCM structure with transistors of different threshold voltages.

These two circuits were adopted as part of a Power Management (PM) system for RFID tag applications. The PM includes a LDO voltage regulator and a low voltage detector that require both the voltage reference and the low voltage monitor. It combines the use of SCM structures with the ZTAT voltage reference to achieve a MOS architecture (without resistor, bipolar transistors or any special device) with very low power and reduced area. The complete PM system is functional with 1μA current consumption.

Experimental results were reported to validate design strategy and prove applicability of the principle to construct a sub-1V temperature compensated voltage reference and its related circuits. The voltage reference and voltage detector circuits and its design procedures have been already filed at the Brazilian Patent Office (INPI) [14-15].

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