Efficient IR Drop Analysis and Alleviation Methodologies Using Dual Threshold Voltages with Gate Resizing Techniques

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ABSTRACT

IR drop impacts circuit delay time and reliability. The IR drop comes from unexpected peak current (Ipeak) consumption. This paper proposes an efficient methodology with an in-house EDA tool named **IPR** to analyze and reduce the Ipeak. IPR adopts dual threshold voltages (Vth) and gate resizing technique; it also lowers the short, dynamic, and static leakage current consumption without degrading the system performance. IPR consists of two parts: Ipeak analysis and Ipeak alleviation processes. Nonlinear static/dynamic timing analysis techniques, in cooperation with dual Vth cell library, provides two kinds of accurate Ipeak calculation methods used in IPR. Using the incremental timing analysis, the Ipeak processing time can be accelerated. Demonstration of the ISCAS89 benchmark circuits shows that IPR can reduce Ipeak by 39%, power consumption by 14%, and delay time by 19%. In addition, it provides 334 times faster computation with 2% and 10% estimation errors of the Ipeak and power in gate-level, respectively, as compared to circuit level simulation results.

Index Terms: IR drop, Peak current, Low power design

I. INTRODUCTION

When the designed circuit consumes a maximum current over the power supplied, the power supply provides an insufficient current and brings about voltage drop (IR drop) to induce circuit performance degradation. IR drop is a well-known signal integrity issue in very deep submicron technology. The IR drop not only induces circuit delay but also reduces the circuit noise margins from lower supply voltages, which leads to reliability issues. The IR drop comes from unexpected peak current (Ipeak) consumption, which is higher than that of the original design's specifications. The Ipeak occurs in a very short period of time and brings about a large IR drop simultaneously. Fig. 1 shows that the Ipeak induces voltage drop levels under three types of resistance (R) of the power source.

The commonly used methodology to resolve the IR drop issue is to re-design power supplies (i.e. using wider power rails for large supplied currents) and to add the decoupling capacitance into the power source. These methods do not take the performance penalty issues into account.

There are some circuit-level EDA tools (e.g. VoltageStorm) that can help designers to identify a circuit's performance impacted by IR drop. The back-end design guide with long computation time issues results in poor management of the Ipeak in the early design stage. IR drop related issues are expected to worsen in future complex designs. Gate-level evaluation tech-

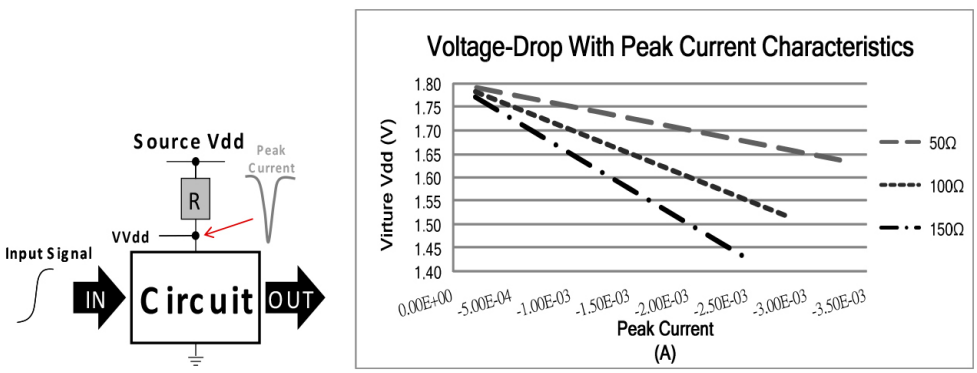

Figure 1. The Ipeak induced supply voltage drop to the circuit.

niques [4-9] have been proposed to resolve these problems, but a long computation time and insufficient accuracy are disadvantages of these proposed techniques.

Ipeak calculation should take the gate delay into consideration. In the traditional design methodology, the circuit performance analysis relies on the longest path delay time calculation by using static timing analysis (STA) or dynamic timing analysis (DTA). The IR drop may not induce circuit delay, due to the fact that not all gates in the circuit are affected by IR drop. The path delay will not increase if the consumed current of those transition gates on the path does not exceed the maximum supply current. Moreover, the circuit total delay does not increase if the gate increasing delay (due to lower voltage) is not located at the critical path. Hence, there is no need to repeat timing calculations of all paths by applying STA/DTA.

Traditional STA/DTA calculate the circuit delay by adding the delays of all gates based on a single threshold voltage source, which does not consider the different gate delays when there is a varying Vth.

From our simulation analysis, the Ipeak of a circuit occurs from the logic gates and flip-flop (FF) state transition at the same timing interval. Therefore, the Ipeak can be resolved by reducing the FF and logic gate transition current by separating the logic gates and FF transition intervals. Some researchers have proposed alleviation techniques to satisfy these optimization processes, but these techniques lead to circuit performance degradation problems.

The Ipeak of a logic gate and FF is dependent on two factors. The first factor is the input signal transition time. For the same output loading, an input signal with large transition time (slow signal transition) will bring about a lower Ipeak. The second factor is the large or small output loading with the same transition time of input signals. From these observations, threshold voltage adjusting with logic gate resizing techniques can be used to degrade the Ipeak.

The following equations show the MOS transistor drain-source current. By increasing the threshold voltage, the peak and average current values can be effectively reduced. Generic design techniques adopt the gate Vth adjusting technique for both regulating circuit performance and power consumption.

$$Ids = \frac{1}{2}\mu_n cox \frac{W}{L}(V_{in} - V_{th})^2 \quad \text{saturation region} \qquad (2)$$

$$Ids = \frac{1}{2}\mu_n cox \frac{W}{L}(2(V_I - V_{th})V_O - V_O^{\,2}) \quad \text{linear region} \qquad (3)$$

The low power design techniques can be used to degrade the Ipeak. Most generic low power techniques focus on reducing the dynamic and leakage power consumptions, but their usefulness is limited to Ipeak reduction, as the low power techniques attempt to shrink the current waveform dimensions. The Ipeak reduction technique reduces the highest current value.

The general power consumption can be divided into three parts, which are represented as follows:

$$P_{total} = C_L V_{DD}^2 f_{0->1} + t_{SC} V_{DD} I_{peak} f_{0->1} + V_{DD} I_{leakage} \quad (1)$$

The first part of C_L is the circuit output loading, where the V_{DD} is supply voltage, and $f_{0->1}$ is the circuit state transition frequency. The second part of t_{SC} refers to the short circuit current duration time and Ipeak is the short current value. The third part includes leakage current.

The paper proposes a methodology to reduce peak-current (Ipeak) and average power while minimizing delay and area. The main techniques used in the IPR framework include gate sizing and multiple-threshold voltage adjusting.

Using the gate size and multiple threshold voltage (Vth) techniques can effectively reduce the Ipeak. In terms of Vth, the higher Vth of the gate, the longer the delay time and the lower Ipeak. The lower Vth of the gate, the shorter delay time and the higher the Ipeak. In terms of gate size side, the small the gate size, the longer the delay time and the lower the Ipeak. The larger size of the gate, the shorter the delay time and the higher the Ipeak.

In the proposed IPR technique, Fig. 2 shows how the gate resizing and the multi-threshold technique can effectively reduce the circuit transition peak current. Most Ipeaks are generated from the gates that are located close to the circuit's fanin or the flip-flops in the circuit transition. By using IPR to adjust the gate size and Vth, Ipeak reduction with lower power consumption and smaller area can all be obtained.

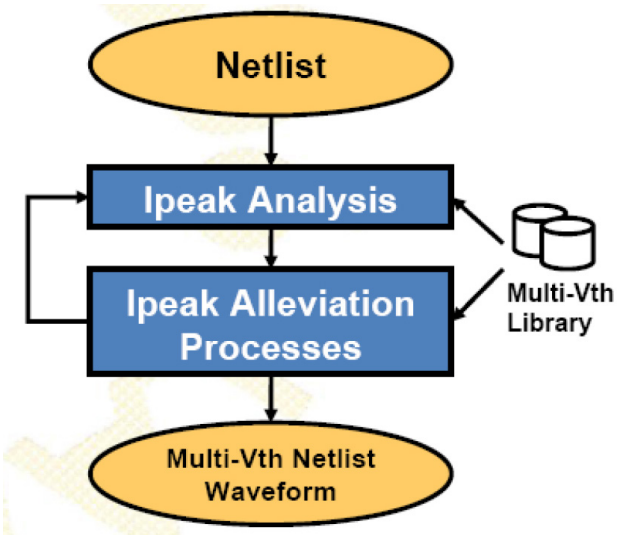

Figure 2. The proposed IPR technique.

In our proposed Ipeak reduction technique, both the FF and logic gate Vth are simultaneously adjusted to reduce the Ipeak. In comparison with CLUSTVAR, the IPR alleviation method emphasizes the FF issue, and can effectively degrade both the Ipeak and power consumption. The IPR alleviation process can also reduce the average power consumption without increasing the circuit delay time and area penalty.

The proposed incremental STA/DTA technique focuses on the necessary paths to avoid re-computing the delay times of all of the paths. NLSTA/NLDTA (nonlinear STA/nonlinear DTA) uses the table lookup method to estimate the gate delay time, which is pattern dependent. Due to the fact that the NLSTA/NLDTA technique adopts the real circuit transition times, the estimation results are more accurate than those using STA/DTA. Compared to the commercial circuit-level SPICE simulation tool (***Nanosim***), IPR provides quick and accurate Ipeak estimations. The IPR gate-level estimation and alleviation process help to resolve the voltage drop problem during the early design stage.

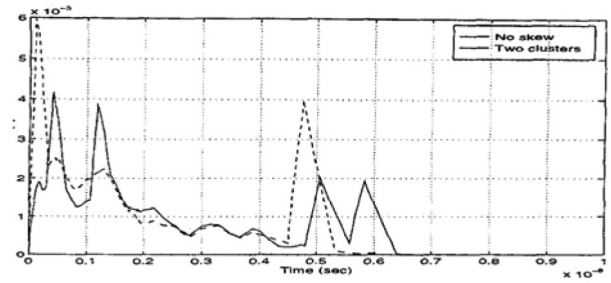

Figure 3. The proposed peak current reduction waveform in [1].

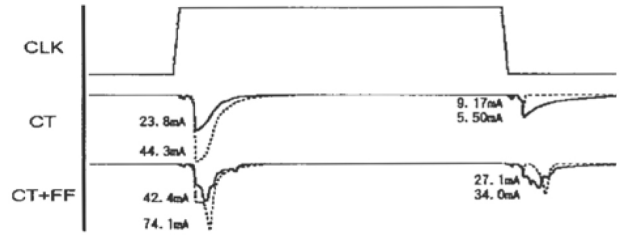

Figure 4. The proposed peak current waveform in [2].

II. LITERATURE REVIEW OF IPEAK REDUCTION TECHNIQUES

An algorithm [1] was proposed that determines the clock arrival time at each flip-flop in order to minimize the current peaks while respecting timing constraints. Benchmark circuits show that current peaks can be reduced by more than a factor of two without penalty on cycle time and average power dissipation.

[2] proposed an opposite-phase scheme for peak current reduction. The basic idea is to divide the clock buffers at each level of the clock tree into two sets: half the clock buffers operate at the same phase as the clock source, while the other half operate at the opposite phase to the clock source. Consequently, this technique can reduce the peak current of the clock tree by nearly 50%, with the current waveforms shown in Fig. 4.

[1-2] proposed an efficient Ipeak reduction technique that uses the useful clock skew to shift the Ipeak generation's location. This technique does not consider that the waveform dimension magnitude is nearly the same, which leads to the highest reduction in peak current, but not in power consumption.

From the literature, CLUSTVAR (Cluster Inclined Supply and Threshold Voltage Scaling with Gate Resizing) [3] is an algorithmic platform for power optimization by using dual supply voltages, gate sizing, and dual threshold voltages. CLUSTVAR can find a circuit status with the lowest dynamic and leakage power consumption-on the premise that the circuit will not degrade performance or violate timing constraints. By demonstrating combinational circuits in the MCNC'85 benchmark suite, the savings of dynamic and leakage power are up to 42% and 67%, respectively.

The CLUSTVAR [3] contribution is for the lower power reduction, in CLUSTVAR, the algorithm is developed based on a maximal-weight independent set. However, the CLUSTVAR only considers the combinational circuit part.

In IPR the peak current reduction and the average power reduction into consideration, and considers using the multiple Vth for logic gate and Flip-Flop (FF). The high/low Vth FFs are used to replace the FFs, that uses the same Vth. As the proposed IPR method considers the impact of Flip-Flop (FF), and the low power efficiency will be better than the CLUSTVAR technique.

The CLUSTVAR technique [3] is STA based. Most conventional STA tools provide overly pessimistic results and are only suitable for general-application designs. The traditional STA computations would require that all the nodes in this circuit be recomputed due to the circuit delay time global impact as shown in Fig. 5. This is due to the facts that simplify STA calculation to reduce the gate-delay re-computation time.

A method is elucidated in [10], in which the combinational circuit simultaneous switching operations are minimized. The delay slack time among the paths and clustered paths have similar slack values. The proposed register-transfer level (RTL) method takes advantage of the logic-path timing slack to reschedule circuit activities and to minimize value within timing intervals.

[11] proposes spreading the clock-tree drivers switching activity while maintaining low clock skew at the clocked tree's sink-nodes. The clock-tree driv-

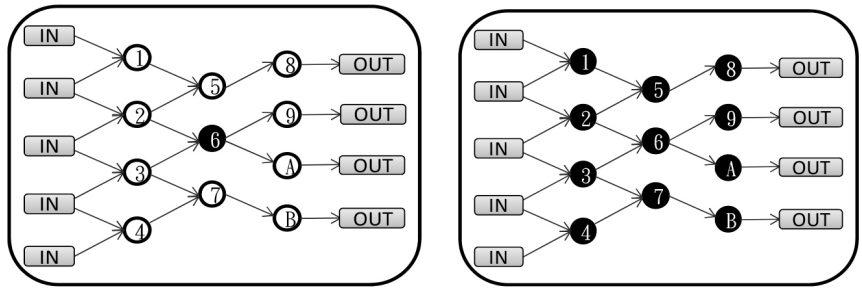

Figure 5. The conventional static gate-delay calculation technique.

er's switching characterization has been used for fast computation of peak currents. [10] employs a mix of high-threshold voltage and low-threshold voltage clock-drivers to minimize clock skew.

In [12], the objective is to reduce the number of glitches from the clock skew scheduling in a circuit, thus reducing dynamic power. The scheduling is formulated to an Integer linear programming problem, and the vector-independent clock skew schedule is derived to reduce glitches.

The studies [10-12] are related to the proposed IPR technique. However, the motivations are different among them. [10][12] contributions are for the power reduction, but not for the peaking current. In IPR, the major target is peak current reduction and the average power reduction has been taken into consideration

For the Ipeak reduction issue, IPR is different from the above research and has several advantages. The proposed IPR gate-level approaches after the circuit has finished the physically back-end synthesis stage, and the gate-level information to be extracted and calculated. This methodology will be more accurate if it is compared to being in the higher (RTL) design phase. Hence, the accuracy increased and computation time reduced targets are both achieved by IPR.

III. THE PROPOSED IPEAK CALCULATION PROCESS

The proposed IPR achieves the targets of Ipeak reduction, power savings, and less area penalty by exploiting the gate resizing and threshold voltage (Vth) adjusting techniques. It adopts a nonlinear dynamic timing analysis with incremental delay time calculation techniques to quickly and accurately reduce Ipeak.

1. Ipeak calculation

Most of the traditional IR-drop evaluation techniques are computed by STA. The STA calculates the path delay by summing all individual gate delays, a process named linear STA. Linear STA is a pattern independent of the worst-case estimation technique. Due to the fact that the STA technique provides an overly pessimistic evaluation of the circuit delay time, it is only suitable for a quick and rough Ipeak estimation.

As the Ipeak is input pattern and delay timing dependent, the linear Dynamic Time Analysis (DTA) technique is used for the pattern dependent delay time calculation, with estimation results close to the real

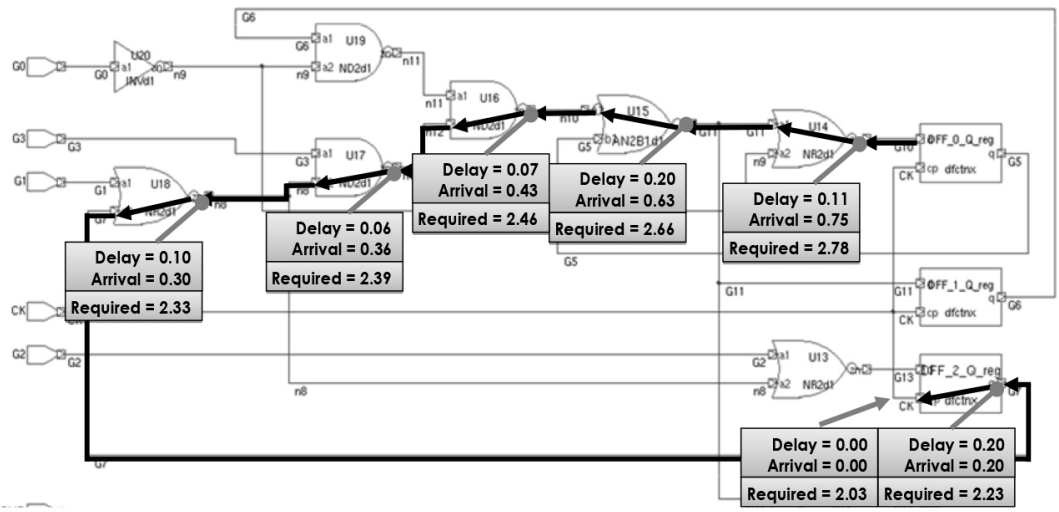

Figure 6. The slack time computation for sequential circuit delay.

ones. NLDTA (nonlinear DTA) achieves more accurate estimation than linear DTA-which has a long calculation time when compared to the STA, NLSTA, and DTA. The accurate Ipeak induced delay is a dynamic behavior, which is pattern dependent. The pessimistic estimation problem from traditional STA or DTA can be solved by using the proposed NLSTA and NLDTA, which are pattern dependent estimation techniques. The NLSTA and NLDTA delay time calculations are obtained from table look up.

NLDTA adopts the transition current of real applications, making it suitable for specific designs. The good Ipeak estimation test patterns (i.e. testbenches) of NLDTA can activate the largest number of gate switches (i.e. transitions) at the same time. Those patterns are the same as when triggering the circuit to generate the largest voltage drop. The NLDTA verification input patterns provided by the circuit designer might be less than those of NLSTA.

2. The incremental delay time calculation

IPR adopts the threshold voltage adjusting and gate resizing techniques to reduce the Ipeak. The gate delay and Ipeak need to be recomputed for accurate estimation when the threshold voltages of the FF and logic gates can be adjusted. However, it is complex to dynamically re-calculate the delay of the circuit by considering all FF and logic gates using dual threshold voltages, because the adjusted Vth results in different FF and logic gate delay times. Therefore, the former estimation on Ipeak should be re-calculated until all FFs/gates are processed. IPR dynamic timing analysis is also required for calculating the floating delay times under dual threshold voltages and resizing of FFs and logic gates. Dynamically re-calculating the circuit NLSTA/NLDTA is time consuming. The calculation time can be reduced by using the incremental methods.

Fig. 5 shows an example of re-computation of gate delays in the STA if the node-6 gate information is modified. Due to the global impact on the circuit delay, the delay information for all of the nodes in this circuit needs to be re-computed. If the incremental STA is adopted, the recomputed process is only needed for the connected gates in fanin and fanout cones of node-6, as shown in Fig. 7. The proposed IPR can quickly estimate the worst-case Ipeak of the circuits by incremental NLSTA/NLDTA.

In IPR, the dynamic nonlinear-STA model uses the table lookup technique to compute an accurate delay time. If used to modify the node-6 gate information, the following incremental STA, only the impacts for the fanin and fanout cones of this node are shown in Fig. 8.

IV. IPEAK ALLEVIATION PROCESS

IPR adopts that threshold voltage adjusting and gate resizing techniques can effectively reduce the Ipeak. In addition, the Ipeak, the average power and area penalty can be reduced by the proposed method. Moreover, the circuit delay time will not be increased if the proposed technique is adopted under positive delay slack time.

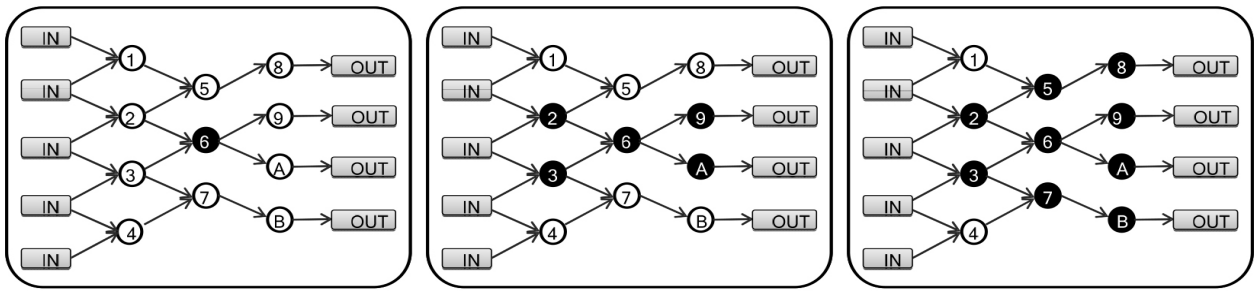

Figure 7. The incremental delay timing computation.

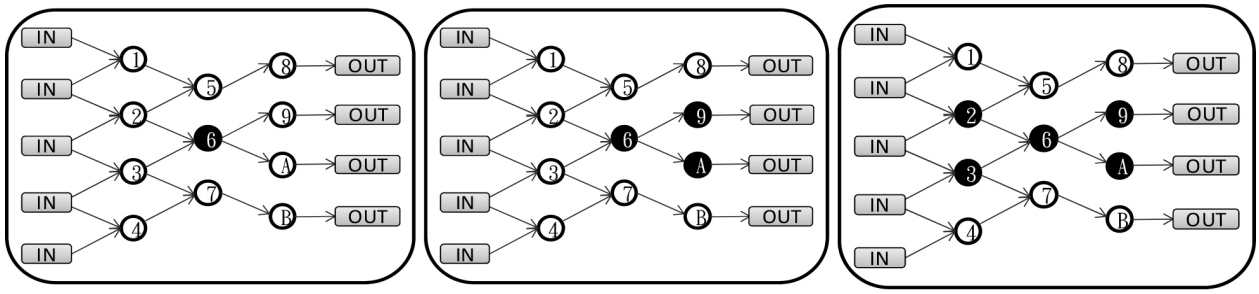

Figure 8. The proposed dynamic non-linear delay time calculation sequence.

The largest Ipeaks are generated from the FFs with prior stages of the logic gate transitions at the same time. High Vth FF/gate has a higher circuit delay time with a lower Ipeak than with a low Vth FF/gate. The proposed Vth adjusting technique has FFs and logic gates in non-critical paths with positive slack time replaced by high Vth FFs/gates, as shown in Fig. 9.

The gate resizing technique employs the greedy algorithm. First, we define the logic gate slack time as φ. The gate resizing process selects the gate with the largest φ and replaces this gate with a small driving gate. For the gate with the smallest φ, we resize it to a large driving gate. This process reduces the transition current, while maintaining the circuit performance.

The proposed IPR can quickly degrade the designed circuit's worst-case Ipeak. The first step is to define the circuit-level from a topological sort, and then to sort the circuit-level by Ipeak. The circuit-level data structure is mapped to a timing-based circuit tree topology. This tree topology makes path tracing easy. The longest circuit path delay can be easily found from the lowest gate of this circuit tree.

The process involves computation and sorting of all gates in each level by the cost (COST). After that, the FF, logic gate Vth adjusting, and gate resizing process are adopted according to the cost function of each gate. The cost function of each gate is defined as:

$$COST=(Peak_{before}-Peak_{after})/(Slack_{before}-Slack_{after}) \quad (4)$$

A large cost function means that the FF/gate contributes to a high Ipeak reduction, which first needs to be processed. The $Peak_{before}$ and $Peak_{after}$ refer to the Ipeak of this FF/gate before and after sizing. $Slack_{before}$ and $Slack_{after}$ refer to the slack times of this gate before and after sizing. The Ipeak reduction process is as follows:

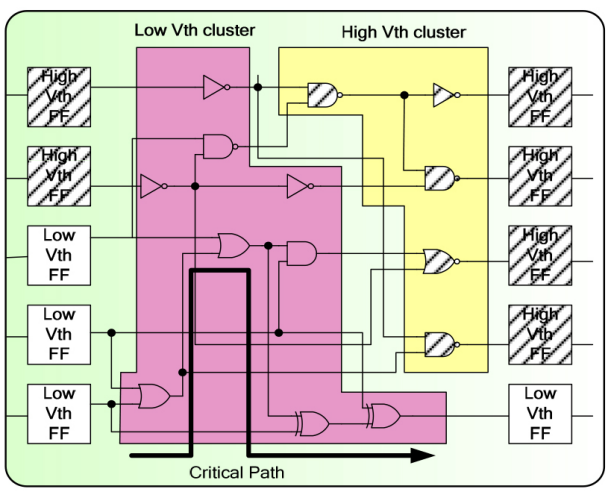

Figure 9. The Ipeak alleviation using dual threshold voltages.

1. *Divide the circuit into a level structure;*
2. *Compute the Ipeak (Ipeak) of each circuit-level;*
3. *For the circuit-level*
   {
   (1) Select the highest Ipeak circuit-level
   {
   a. *Compute the cost function of those FFs/gates in the circuit-level and sort the cost function by heap sort;*
   b. *Re-compute the COST of the FF/gate after the resizing and Vth adjusting process, and select gate with the highest COST;*
   c. *Assign the suitable sizing and Vth to this FF/gate.*
   }
   (2) Re-compute the circuit slack time using the incremental NLSTA/NLDTA technique;
   (3) Repeat (1) until all FFs/gates are processed in the same circuit-level.
   } *Repeat for the second highest circuit-level until all circuit-levels are processed.*

The threshold voltage aware cell delay is characterized from the CCU 0.18μm CMOS standard cell library, and calibrated using HSPICE simulation results. The intrinsic delay is characterized from the gate simulation without output load. The high and low threshold voltages of the gate are 0.4452004V and 0.269V for NMOS (-0.4379811V and -0.1277685V for PMOS), respectively.

V. THE PROPOSED IN-HOUSE IPR EDA TOOLS

Fig. 10 shows a conventional sequential circuit. We first divide the generic circuit into combinational and FF parts, and then repeat the calculation process for the separable combinational and FF circuit parts. Then, after the FF and combinational parts Ipeak alleviation process, the alleviation flow merges back to the original circuit.

Fig. 11 shows the framework of the proposed IPR EDA tool. The analysis mode is adopted to quickly calculate the path delay by applying the incremental timing analysis technique. Then, after the circuit-level with the largest Ipeak is located by sorting, the new Ipeak alleviation is processed by varying in Vth or logic gate resizes.

The Ipeak alleviation/analysis tool includes two major functions, as shown in Fig. 12, i.e. Ipeak analysis and Ipeak alleviation. This software package is written in *C, sis,* and *Perl*. This tool is also equipped with a common interface, compliant with commercial tools like Synopsys and Nanosim.

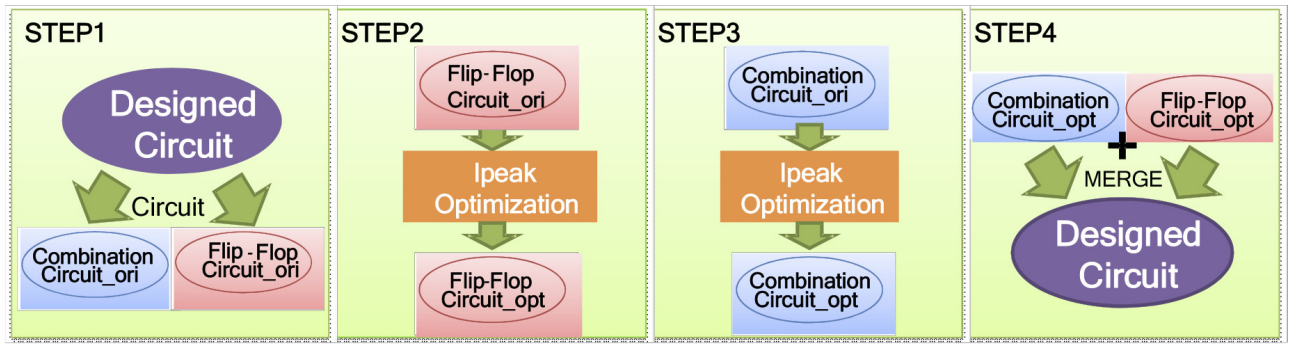

Figure 10. The sequential circuit processing flow in the proposed IPR.

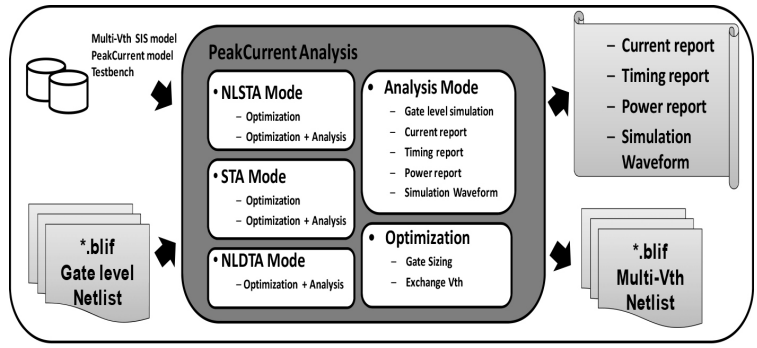

Figure 11. The proposed IPR tool framework.

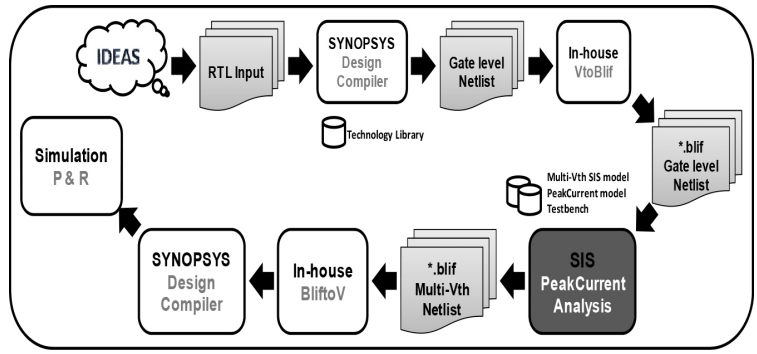

Figure 12. The proposed IPR alleviation/analysis flow.

The Ipeak analysis consists of the functions:

1. Gate level function simulation;
2. Consumption current report;
3. Circuit delay timing report;
4. Power consumption report;
5. Voltage/current waveforms.

The Ipeak alleviation includes the techniques:

1. Gate resizing;
2. Threshold voltage adjustment.

The contribution of the proposed IPR EDA tool is two-fold. First, it is a quick and accurate technique for Ipeak estimation technique. Second, it is able to reduce the peak and average current values of the circuits. The IPR helps designers to design circuits with low Ipeak and average currents in the early design phase.

The slack time lets the logic gates in the non-critical path to be replaced by a high-Vth gate, in our analysis the largest transition currents are closed to the circuit fanins or outputs of flip-flops. The high and low thresholds are 0.23V and 0.38V, respectively. The threshold voltage adjusting techniques introduced in Fig. 13, the gate resizing technique is as the similar manner.

Because the result of conventional static timing analysis technique is too pessimistic, the technique is not suitable for specific applications. The dynamic non-linear timing analysis technique is used to obtain the slack time. There are 2000 random test patterns used for the test circuit during the peak current evaluation stage. The nonlinear dynamic timing analysis technique obtains the desired peak current reduction, saving power and design area. Table 2 shows the comparisons of non-linear STA and DTA.

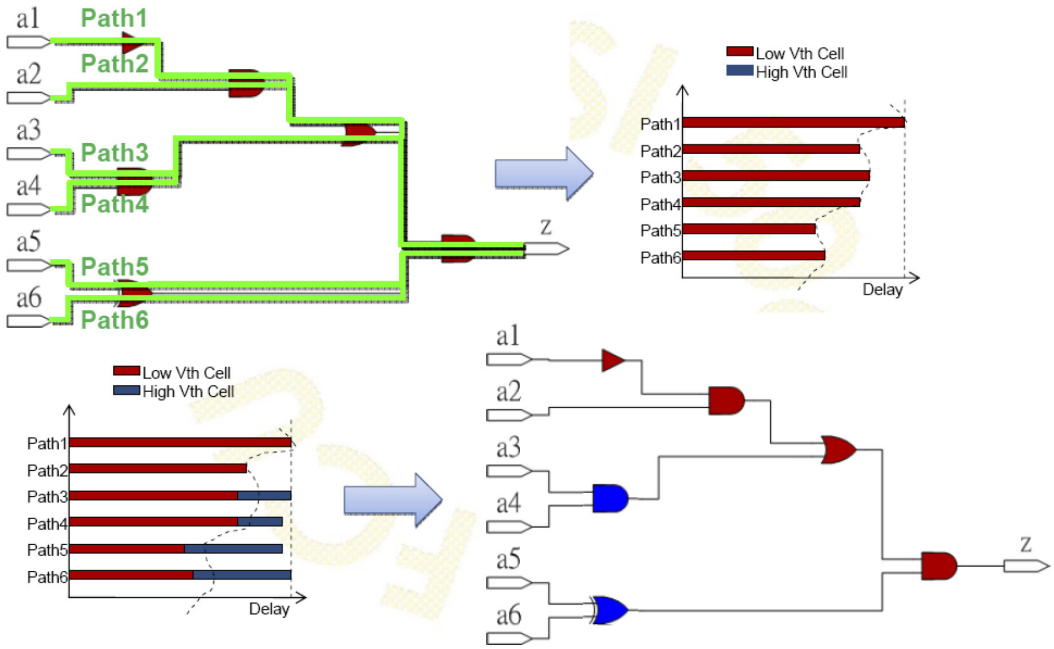

Figure 13. IPR replaces the original gate into high and low threshold voltage gate.

The proposed IPR technique uses the gate-sizing, multi-threshold technique. The cost function of gate-sizing and high/low-Vth gate selections is:

$$\textbf{Cost Function} = (\textbf{Peak}_{before} - \textbf{Peak}_{after}) / (\textbf{Slack}_{before} - \textbf{Slack}_{after})$$

$Peak_{before}$ and $Peak_{after}$ mean peak current of this gate before and after sizing, respectively. $Slack_{before}$ and $Slack_{after}$ mean slack time is nearly the same before and after sizing. The large cost functions mean gate contribute to more peak current reduction results, and thus it needs to be replaced first.

The follows greedy algorithm is adopted for gate-sizing and high/low-Vth gate selection process. The procedure of peak current reduction

1. Divide the circuit into level structure
2. Compute the peak current of each level
3. For the circuit

(1)Choose the highest level
{
{ (2) a. compute the cost function of those gates in this level by heap sort
b. Compute the cost of this gate under different sizing and threshold voltag es with a highest-cost gate and find a suitable threshold voltage.
}
(3) Recompute the circuit delay slack time using the incremental STA technique.
(4) Repeat (1) until the all gates to be pro cessed are at the same level.
}
(5) Repeat the second highest level until all levels are processed.

VI. EXPERIMENTAL RESULTS

There were 10 test circuits used to demonstrate the performance of the proposed IPR tools, including nine of the ISCAS89 benchmark circuits and one variable length decoder (VLD) circuit. Table 1 shows the original circuit simulation results by Nanosim. Two thousand random test patterns are used for testing the circuits, and the results were used as the basis in the comparison with the CLUSTVAR technique [3]. The negative values in Table 2 to Table 5 show that the values obtained from CLUSTVAR and the proposed NLSTA/NLDTA techniques of IPR are less than the basis of the original circuit (without any alleviation process) in Table 1.

Table 2 shows the comparisons of the peak current and power consumption between the proposed technique and the CLUSTVAR technique. Adopting the NLSTA and NLDTA results with a more than 35% reduction in the average Ipeak, there is a 7% and 8% reduction in power of the NLSTA and NLDTA techniques respectively, as compared to CLUSTVAR.

As the CLUSTVAR technique does not consider the delay time optimization which include FFs, the circuits' longest delay times increase if Vth and driving capability are adjusted only for logic gates. In Table 3, comparison with CLUSTVAR technique shows that there is a 1% and 19% delay time reduction for the NLSTA and NLDTA techniques, respectively. There are no significant differences in area comparisons among the CLUSTVAR, NLSTA, and NLDTA techniques.

Table 1. The original simulation results for the test circuits

Circuit Name	Original			
	Peak Current(mA)	Average Power(uW)	Max Delay(nS)	Core Area(pitch)
s27	- 1.263	13.479	1.190	205
S349	- 4.523	81.384	2.526	1554
s9234	- 33.694	543.176	3.464	15131
S5378	- 62.813	949.860	2.928	21377
S13207	- 133.398	2290.972	5.406	49785
S15850	- 100.447	2134.741	8.754	50271
VLD	- 37.116	665.922	11.561	47734
S38417	- 282.405	6517.099	5.199	149410
S38584	- 366.605	7667.985	5.323	146958
S35932	- 557.300	9681.069	2.983	159564

Table 2. The reduction of Ipeak and power consumption

Circuit Name	Peak Current			Average Power		
	Clustvar	NLSTA	NLDTA	Clustvar	NLSTA	NLDTA
s27	- 4.14%	- 30.15%	- 36.16%	- 4.33%	- 8.30%	- 9.67%
S349	- 2.92%	- 40.81%	- 38.72%	- 6.53%	- 12.63%	- 12.71%
s9234	- 2.83%	- 39.23%	- 38.53%	- 3.34%	- 11.81%	- 12.18%
S5378	- 12.61%	- 44.59%	- 44.54%	- 13.43%	- 20.08%	- 21.70%
S13207	- 2.54%	- 38.89%	- 39.00%	- 3.69%	- 12.58%	- 13.89%
S15850	- 1.40%	- 37.92%	- 37.89%	- 5.52%	- 13.78%	- 15.32%
VLD	- 1.68%	- 34.16%	- 38.64%	- 6.74%	- 16.81%	- 16.43%
S38417	- 1.78%	- 38.56%	- 38.76%	- 2.13%	- 11.28%	- 11.04%
S38584	- 3.68%	- 38.30%	- 38.28%	- 7.97%	- 15.18%	- 16.10%
S35932	- 4.23%	- 38.77%	- 39.48%	- 4.55%	- 11.85%	- 13.04%
Average	- 3.78%	- 38.14%	- 39.00%	- 5.82%	- 13.43%	- 14.21%

Table 3. The reduction in delay time and core area

Circuit Name	Delay Time			Core Area		
	Clustvar	NLSTA	NLDTA	Clustvar	NLSTA	NLDTA
s27	27.05%	- 5.29%	- 3.86%	0.00%	0.00%	0.00%
S349	46.40%	- 0.64%	- 1.84%	0.00%	0.00%	0.00%
s9234	67.01%	- 0.19%	- 0.19%	- 0.49%	- 0.22%	- 0.24%
S5378	37.05%	- 1.23%	- 5.05%	- 0.29%	- 0.29%	- 0.28%
S13207	39.19%	- 1.28%	- 52.43%	- 1.12%	- 0.53%	- 1.27%
S15850	30.35%	- 1.42%	- 31.78%	- 1.58%	- 0.27%	- 1.86%
VLD	17.71%	- 0.53%	- 67.97%	- 0.04%	- 0.04%	- 0.12%
S38417	40.63%	- 1.13%	- 27.58%	- 0.09%	- 0.09%	- 0.10%
S38584	31.92%	0.31%	- 2.48%	- 0.83%	- 0.83%	- 0.92%
S35932	52.89%	0.00%	0.00%	0.00%	0.00%	- 0.26%
Average	39.02%	- 1.14%	- 19.32%	- 0.44%	- 0.23%	- 0.50%

Table 4. The estimation accuracy of the proposed IPR as compared to that of Nanosim

Circuit Name	MAX Peak Current(mA)			Average Power(uW)		
	Nanosim	OUR	error %	Nanosim	OUR	error %
s27	- 1.263	- 1.260	- 0.20%	13.479	11.902	- 11.70%
S349	- 4.523	- 4.465	- 1.30%	81.384	72.421	- 11.01%
s9234	- 33.694	- 34.546	2.53%	543.176	494.048	- 9.04%
S5378	- 62.813	- 62.114	- 1.11%	949.860	862.956	- 9.15%
S13207	- 133.398	- 127.825	- 4.18%	2290.972	2101.525	- 8.27%
S15850	- 100.447	- 96.135	- 4.29%	2134.741	1966.001	- 7.90%
VLD	- 37.116	- 36.705	- 1.11%	665.922	605.615	- 9.06%
S38417	- 282.405	- 273.937	- 3.00%	6517.099	5897.327	- 9.51%
S38584	- 366.605	- 358.809	- 2.13%	7667.985	6864.462	- 10.48%
S35932	- 557.3	- 535.546	- 3.90%	9681.069	8667.232	- 10.47%
		Average error %	- 1.87%		Average error %	- 9.66%

Table 5. Execution times using Nanosim and the proposed IPR

Execution time(S)	Nanosim	OUR	X
s27	2268.12	8.20	276.60
S349	16789.01	59.98	279.91
s9234	173108.72	352.11	491.63
S5378	201476.46	720.84	279.50
S13207	681476.33	1601.11	425.63
S15850	558466.99	1396.23	399.98
VLD	222593.30	530.11	419.90
S38417	716073.10	4682.41	152.93
S38584	1566344.48	5796.95	270.20
S35932	2659931.09	7747.44	343.33
		Average	333.96

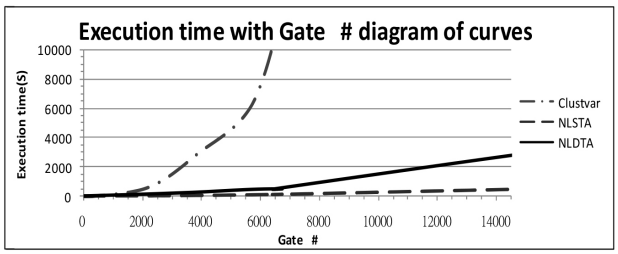

Figure 14. Comparison of the execution times of different techniques.

Table 4 shows the comparisons of the estimation results between the Nanosim and the proposed IPR EDA tools. The IPR provides good estimation with only 1.87% and 9.66% estimation errors in Ipeak and power consumption respectively, as compared to Nanosim.

From the viewpoint of execution times shown in Table 5, the proposed IPR is 334 times faster than Nanosim. The Nanosim simulation results are adopted as the golden values in the experiments.

Fig. 14 shows the comparisons of the execution times among the techniques of CLUSTVAR, NLSTA, and NLDTA with respect to circuits having different numbers of gates. Different from the CLUSTVAR technique based on the conventional STA algorithm, the proposed IPR uses the incremental NLSTA/NLDTA with less calculation time for large circuits.

VII DISCUSSIONS

A large peak-current (Ipeak) induced a voltage-drop and impacted the circuit delay time and reliability. This paper presents an Ipeak estimation technique and an Ipeak alleviation technique (based on gate resizing and Vth selection). There are several claims addressed in this paper.

(1) The input signal with a lower transition time (fast signal transition) has a lower Ipeak.

(2) The generic static timing analysis tool does not consider gate dual-delay for dual-Vth cells for the path delay time calculation.

(3) When calculating the Ipeak, the proposed IPR method partitions a circuit level by level and then sums the Ipeak at every level. However, due to the different delays of various gate types, gates of the same level do not necessarily switch at the same time. The proposed technique identifies the transition gate and takes the gate's timing and peak-current into the calculation.

(4) In general, using gate size and Vth change as a means of peak-current reduction is more easily evaluated than other competing constraints in low-power domain design objectives and might be fit for advanced design technology.

(5) The Ipeak is related to the timing of the gate's transitions. Accurate timing analysis can efficiently reduce Ipeak. The proposed incremental STA was used for quick and accurate estimates. Compared with the other gate level tools, the non-linear STA model provides more accurate results.

(6) Moreover, the dynamic nonlinear STA has good computation effort saving. The computation time comparisons is shown in the Fig. 15.

(7) There is a greater power reduction of the proposed IPR than CLUSTVAR [3]. Ipeak minimally contributes to lower power consumption. There is a 10% average power reduction if the Ipeak reduction is used. This means a benefit for the average power reduction by judging from reducing the Ipeak, only the Vth and gate resizing are used. The Ipeak reduction technique is a better method for designing a low-power circuit, as the lower Ipeak technique can be applied for the power reduction by decreasing the average current.

(8) In the proposed IPR technique, an algorithmic platform is used for peak-current (Ipeak) reduction by using gate-sizing and multiple-threshold voltage techniques. By using gate-sizing and dual-threshold voltage, both Ipeak and the dynamic power consumption are lowest. The operation can find the circuit that will not degrade in performance or violate time constraints. Moreover, when computing, the proposed IPR technique considers delay-time and Ipeak reduction at the same time, making use of IPR with different CMOS processes. By demonstrating on sequential circuits in the MCNC'85 benchmark suite, a 39% Ipeak reduction and a 14% power reduction can be achieved. IPR is up to 334 times faster at calculating reductions compared with conventional SPICE level tools. There is a ±2% margin of error for the proposed IPR tool.

VIII. CONCLUSION

The voltage drop induced by peak current not only results in circuit delay, but also reduces the circuit noise margin and brings about the issue of reliability. The proposed IPR uses dual threshold voltages with gate resizing to effectively degrade Ipeak, power consumption, delay time, and core area without extra overhead or circuit delay time. The proposed IPR provides the quick and accurate estimation of peak current and power consumption of a circuit, which helps designers to predict and improve the circuit voltage drop in an early design phase.

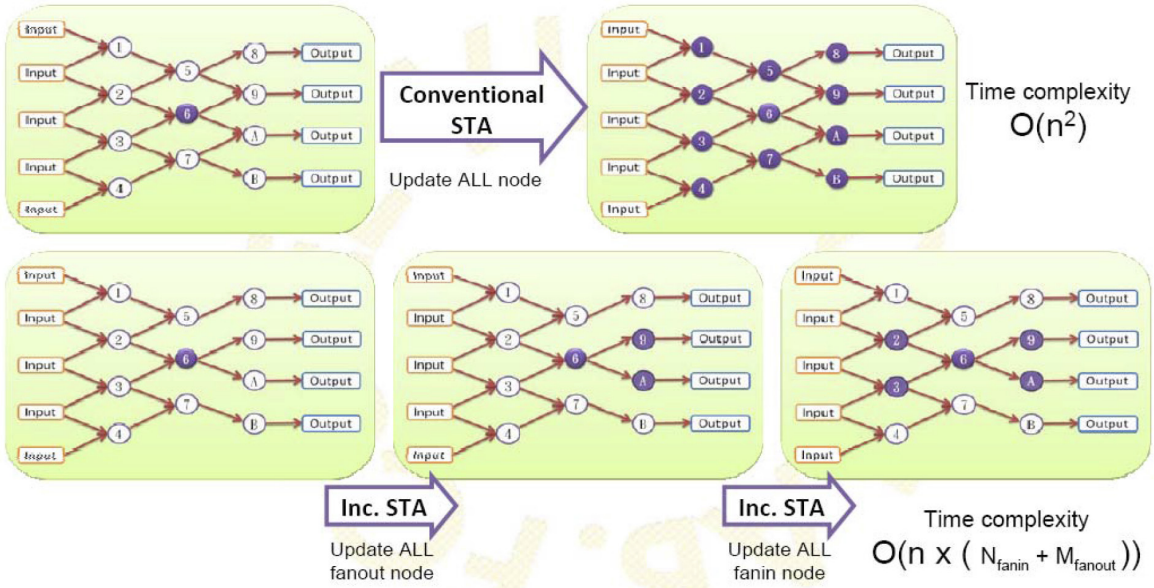

Figure 15. The timing calculation comparisons for proposed increment STA technique.

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