Negative high voltage DC-DC converter using a New Cross-coupled Structure

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ABSTRACT

In this paper, a negative high voltage DC-DC converter using a new cross-coupled charge pump structure has been proposed, which can solve the shoot-through current problem of the conventional charge pump by using a four clock phase scheme. Also, by switching the power supply to each stage based on the supply voltage, a variable voltage gain can be obtained. A complete analysis of the interaction between the power efficiency, area, and frequency have been presented. The proposed negative charge pump is designed to deliver $40\mu A$ with a wide supply range from 2.5V to 5.5V using $0.18\mu m$ high voltage LDMOS technology.

Index Terms: Charge pump, DC/DC converter, Switched-capacitor power converter, Voltage multiplier

I. INTRODUCTION

Charge pump circuits (also called switched capacitor DC-DC converters) are widely used to generate voltages beyond normal supply range or a negative voltage. Charge pumps have been widely used in the nonvolatile memories, such as EEPROM and Flash memories [1]-[5], Power IC, and switch capacitor systems. The output power in these applications is often in the mW range, but converter efficiency and area taken by the charge pump can be very important.

Among many approaches to the charge pump design, the switched capacitor circuits such as Dickson charge pump [6]-[8] are very popular, because they can be implemented on the same chip together with other components of an integrated system. The voltage gain of Dickson charge pump is a function of the number of stages. However the voltage drop across the diodes or diode-connected transistors is too lossy for high efficiency applications. Ref. [9] presented a static charge transfer switches technology to compensate the inherent transistor threshold voltage drops. Theoretically, the modified charge pump is more efficient than the conventional one, but a major drawback is an undesirable reverse charge leakage, which reduces the voltage pumping gain. An improved design proposed two years later claimed to be capable of solving the leaking problem by adding a pair of auxiliary transistors in each power stage [10]. However the impact of the body effect limits this topology to five power stages.

As the supply voltage decreases to the threshold voltage, the conventional Dickson charge pump does not function properly, since its conversion efficiency would be near zero. As the alternative to Dickson charge pump circuits, cross-coupled switched capacitor DC-DC converters are more appropriate for battery-driven portable applications [11]-[16]. Since the voltage gain for the cross coupled architecture is higher than that of a Dickson charge pump, the number of stages needed to reach a specific output voltage is reduced. This reduces the parasitic capacitances introduced in the circuit.

This paper describes a new charge pump that is able to generate a high negative voltage with a wide supply voltage range. The variable voltage gain is realized by switching the power supply to each power stage based on the supply voltage V_{DD}. A three stage topology implemented in $0.18\mu m$ high voltage LDMOS technology is demonstrated in section II. Section III describes detailed circuit design issues. Design considerations of the negative charge pumps are presented in section IV, where tradeoffs between power area and frequency are addressed. In section V, the performance of the negative charge pump is described, and finally conclusions are given in section VI.

II. ARCHITECTURE OF THE PROPOSED HIGH VOLTAGE NEGATIVE CHARGE PUMP

The basic operation of the conventional cross-coupled charge pump circuits is shown in Fig. 1. The non-overlapping complementary clock phases *Φ1* and *Φ2* are designed to avoid short-through current. V_A and V_B swing from V_{DD} to $-V_{DD}$ alternately to charge C_{L1} to $-V_{DD}$. By cascading three such structures, a voltage gain of -7X can be obtained. Since C_{L1} is charged in both phases, the operating frequency is 2 times of the Dickson charge pump.

However, in order to prevent shoot-through current of the inverters driving C_3 - C_6, a level shifter circuit is needed which consumes static power. Moreover, the non-overlapping clock phase *Φ1* and *Φ2* prevent shoot-through current for M1 and M2, but they also generate shoot-through current for M3 and M4. This happens in the *2nd* and *3rd* stages too. Finally, the conversion ratio of the conventional charge pump circuit is fixed as long as the circuit topology is decided, which results in a limited input voltage range.

An improved negative charge pump design based on cross-couple structure is shown in Fig. 2. The operation of the negative charge pump is as follows. Four clock signals have been used to avoid the shoot-through current. When *Φ1=1* and *Φ2=0*, V_A is pushed up to 0V while V_B is pulled down to $-V_{DD}$. At the same time, M3 is turned off and M4 is turned on. As a result,

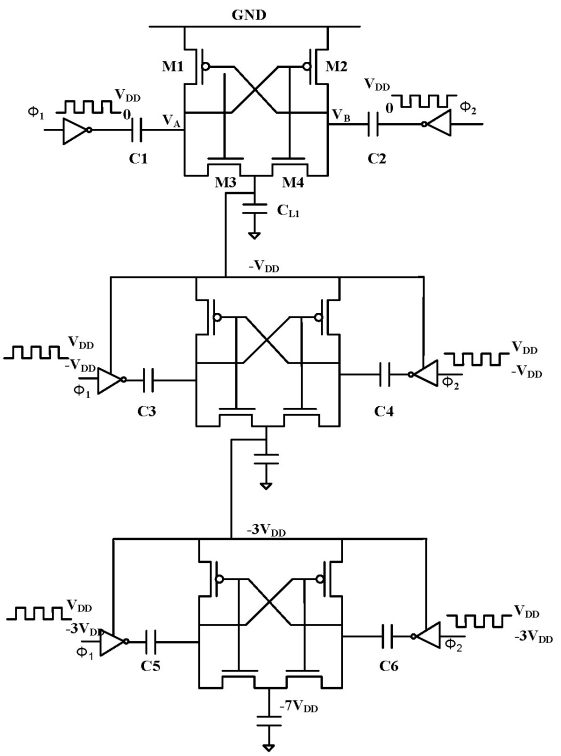


Figure 1. Conventional cross-coupled structures of negative charge pump circuits.

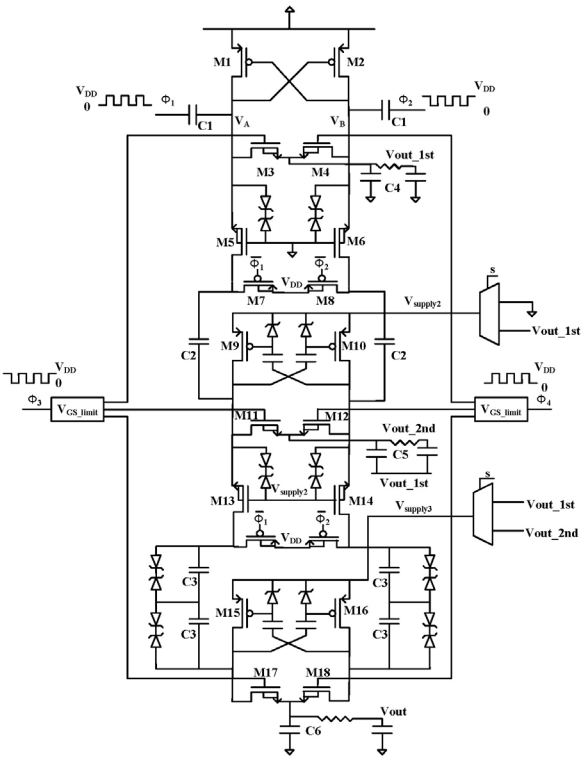


Figure 2. LDMOS drive circuit for V_{GS} breakdown protection.

the output voltage of the *1st* stage will be pulled down to $-V_{DD}$. The gate voltage of M5 and M6 is grounded, which makes sure they are turned on separately only when V_A or V_B is pulled down to $-V_{DD}$.

The top plate of C2 is pushed up to V_{DD} when *Φ1=1* and pulled down to $-V_{DD}$ when *Φ1=0*. The bottom plate of C2 is pushed up to $-V_{DD}$ and pulled down to $-3V_{DD}$ separately when the supply voltage of the second stage is Vout_1st. In this case, the voltage gain of the *2nd* stage is -3X. Finally, if $V_{supply3}=Vout\_2^{nd}$, this negative charge pump can provide a maximum voltage gain of -7X. By switching the supply voltage of the *2nd* and *3rd* stage, a variable conversion ratio can be realized.

For process consideration, since the MIM capacitor can tolerate up to 8V across the pates, the bottom plate of C5 is connected to Vout_1st and capacitor C3 is replaced by two capacitors in series. Although fringing capacitance can be used here, it provides lower power efficiency due to high parasitic capacitance. The only fringing capacitance that cannot be avoided is C6. By connecting the gate voltage of M13 and M14 to $V_{supply2}$ instead of *Φ3* and *Φ4*, a larger V_{GS} is allowed, which reduces the RC delay. The charge pump circuit operates at a high frequency level in order to increase their output power with in a reasonable size of total capacitance used for charge transfer. The operating frequency may be adjusted by compensating for changes in the power requirements and saving the energy delivered to the charge pump.

III. CIRCUIT DESIGN ISSUES

A. Clock Scheme

The non-overlapping clock phase *Φ1* and *Φ2* prevent shoot-through current from M1 and M2 as shown in Fig. 2. However, if these two clock phases are applied to the gate voltage of M3 and M4, the shoot-through current occurs when both of them are at high voltage. This results in higher ripple voltage and power consumption.

In order to avoid current flowing from C1 to the output while *Φ1* is high, M3 should be turned off. The clock phase *Φ3* and *Φ4* have been generated as shown in Fig. 3. The negative delay is realized by adding a buffer between the inverter and the clock generator. As a result, M3 or M4 will be turned on only during the time V_A or V_B is pulled down. Since C2 is charged and discharged by clock phases of *Φ1* or *Φ2*, the clock phases in the *2nd* stage are the same as that in the *1st* stage. There are two advantages here: First, the clock phases of M9 and M10 are still non-overlapping. Second, the clock phases of *Φ3* and *Φ4* can still be used to avoid shoot through current from V_{DD} to *Vout_2nd*. This applies to the *3rd* stage too. This means the four clock scheme is applicable to all the three stages in this charge pump circuit to avoid the shoot-through current. Since only six minimized logic gates are added, the extra power consumption is negligible.

B. LDMOS Drive Circuit

The process used in this design is 0.18μm high voltage LDMOS technology. The drain and source

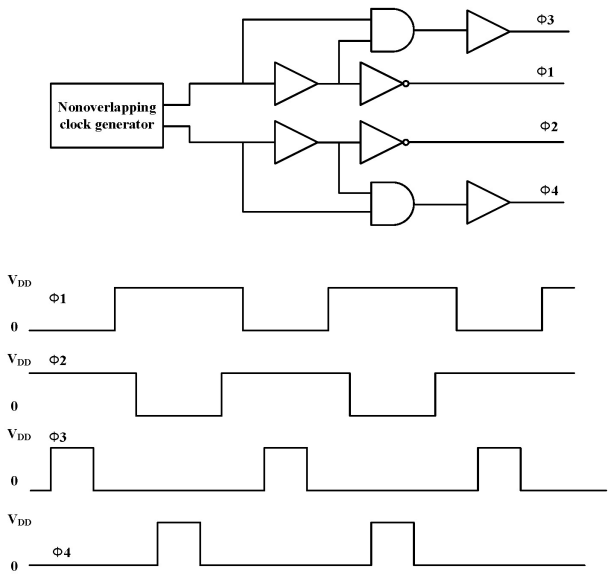


Figure 3. Four clock phase generator used to prevent shoot-through current.

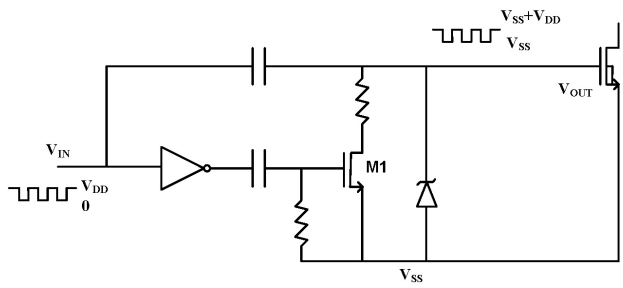


Figure 4. LDMOS drive circuit for V_{GS} breakdown protection.

breakdown voltage V_{DS} is as high as 24V. However, the gate and source breakdown voltage V_{GS} is limited to 5.5V. The V_{GS} breakdown protection circuit is designed using capacitive coupling technology as shown in Fig. 4. The input signal is a clock signal swings between V_{DD} and ground while the output voltage *Vout* swings between $V_{SS}+V_{DD}$ and V_{SS}. The transistor M1 is added to ensure that while $V_{SS}<V_{Breakdown}$ (schottky diode's reverse breakdown voltage), the lower dc level of V_{out} is still able to be pulled down to V_{SS}. In this case, the gate and source voltage is limited to V_{DD}, which is less than the breakdown voltage.

C. MIM Capacitor and Fringing Capacitor

The maximum voltage across the MIM capacitor is around 8V in the high voltage LDMOS technology. In this design, the voltage across the *2nd* output stage and in the *3rd* stage exceeds this voltage limit. One possible solution is to use the fringing capacitor to replace these MIM capacitors. However, the fringing capacitor has much larger parasitic capacitance than MIM capacitor, which reduces the power efficiency. Alternatively, the bottom plate of C5, capacitor at the *2nd* output stage in Fig. 2, is connected to *Vout_1st* instead of ground, which could limit the voltage across C5 within 8V. Moreover, the capacitor in the 3*rd* stage C3 is replaced by two capacitors in series, which reduces the voltage across by half. Although this will increase the area by 4 times, it still provides better power performance than using fringing capacitor, and the increased size of the area is acceptable since the capacitors in the *3rd* stage have the minimum value as will be explained in section IV. As a result, the only fringing capacitor used in this design is C6 at the *3rd* output stage.

D. Non-Regular Multiplexer

The multiplexer used in this design is to switch the power supply of the *2nd* and *3rd* stage to different voltage levels in order to provide a variable voltage gain based on the supply voltage V_{DD}. Since the input voltage level to the multiplexer is unknown and is based on V_{DD} as well as the voltage gain, the select signal of this

multiplexer has to be designed carefully. Otherwise, the pass transistors are not switched properly.

Figure 5 shows the circuit diagram of the non-regular multiplexer which consists of an NMOS select signal generator, PMOS select signal generator, and two pass transistors.

For the NMOS Select Signal Generator in Fig. 5(a), while the input voltage is high, transistor M3 is turned off and there is no current going through the current mirror. As a result, the current only flows through M4, and the output voltage V_{OUT} between the Zener diode and ground has a voltage level of V_{LOW} to V_{LOW}+5V.

On the other hand, while the input voltage is low, V_A is pulled down and almost of the current flows through M3 and M5. In this case, M4 works in the weak inversion region, and M6 is in the triode region. The voltage between the drain and source of M6 almost equals to 0 in order to meet a zero current condition. The output voltage level is now pulled down to V_{SS}.

Similarly, the output voltage of the PMOS Select Signal Generator in Fig. 5(b) swings between V_{High} and V_{High}-5V. The reverse breakdown voltage of the Zener diode is 5V.

The design of the non-regular multiplexer uses 0 and V_{DD} as the select signal and outputs a voltage level of V_{IN1} or V_{IN2}. As shown in Fig. 5(c), V_{IN2} is the *2nd* stage output voltage and V_{IN1} is the *1st* stage output voltage, so we have $V_{IN2}<V_{IN1}$. When select signal *S* is high, the output voltage of NMOS select signal generator is V_{IN2}+5V, which turns on the NMOS pass transistor and pulls *Vout* down to V_{IN2}. At the same time, the output voltage of PMOS Select Signal Generator is V_{IN1}, which turns off the PMOS pass transistor and prevents charging current flowing from V_{IN1} to *Vout*. On the other hand, while select signal *S* is low, the output voltage of NMOS select signal generator is V_{IN2}, which turns off the NMOS pass transistor and prevents charging current from *Vout* to V_{IN2}. The output voltage of PMOS Select Signal Generator is V_{IN1}-5V, which turns on the PMOS pass transistor and pushes *Vout* up to V_{IN1} without a threshold voltage drop, where the body of the MOSFETs has to be connected carefully in order to prevent forward biasing of the PN junction.

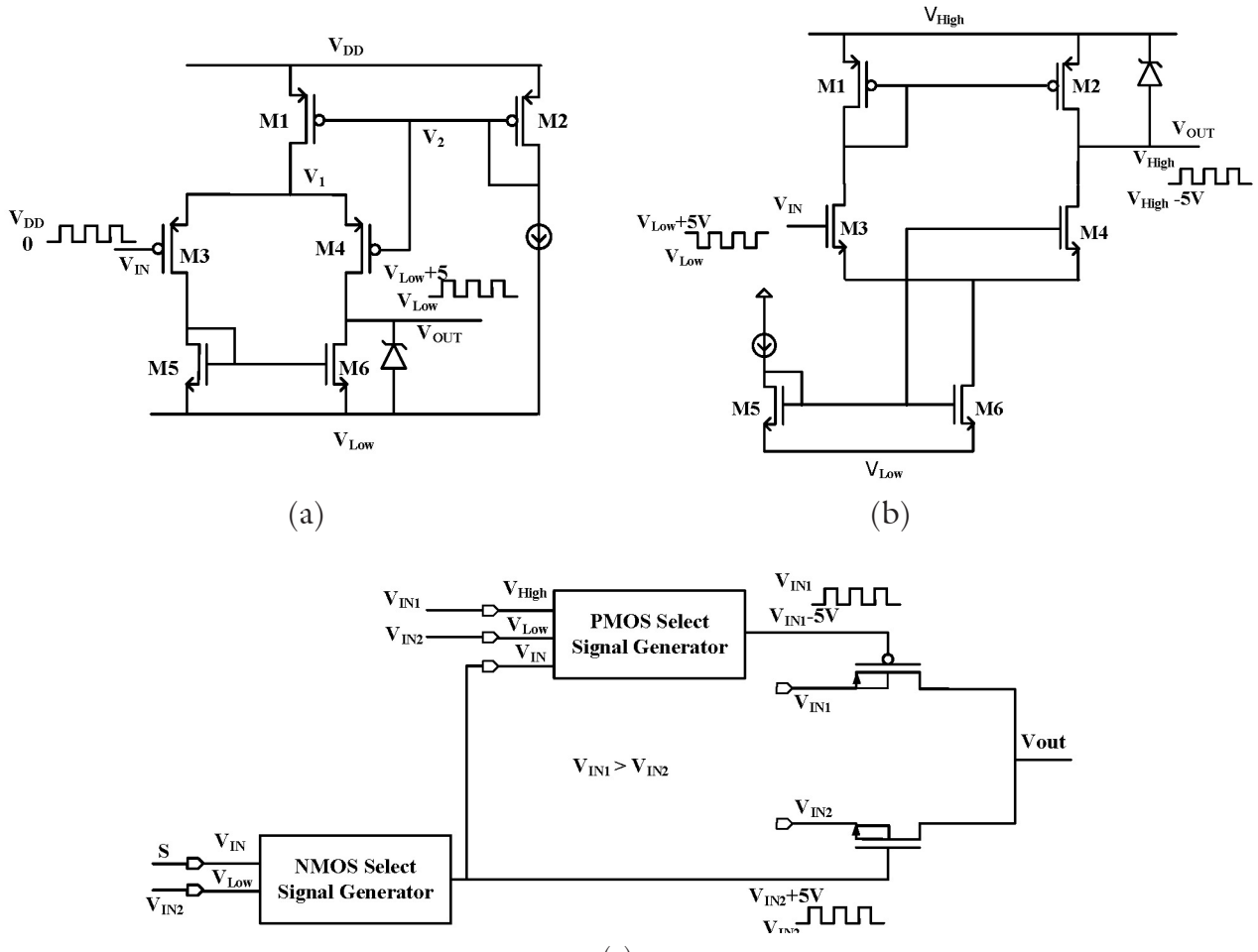


Figure 5. Non-regular Multiplexer circuit design: (a) Select signal generator for NMOS; (b) Select signal generator for PMOS; (c) Detailed circuit diagram of the Non-regular multiplexer.

IV. POWER, AREA AND FREQUENCY CONSIDERATIONS

The charge pump circuit analysis so far concentrates on the circuit operation only. It is required to have a minimum area and high power efficiency in modern IC technology to save the fabrication cost. In order to optimize the circuit performance, the interaction among the power, area, and frequency is analyzed. Figure 6 is the simplified diagram of the proposed negative charge pump circuit with the voltage gain of -7X. Each MOSFET has been replaced by a two-phase switch. For the cross-coupled structure, the charging and discharging status are switched every half period. For example, suppose the loading current is I_0, while the left half part of the circuit is being discharged by the load current, the right half part of the circuit is being charged from the power supply. In this case, the average current flowing through C_5 equals to I_0. Simultaneously, C_6 is being charged by the same amount of average current I_0 in order to restore the charge that has been discharged during the previous half period. At the 2^{nd} output stage, the equivalent load current is now $2I_0$, consisting of the discharging currents flowing through C_5 as well as the charging current flowing through C_6. Also, the average current flowing through the capacitors C_3 and C_4 in the 2^{nd} stage increases $2I_0$. Based on the same analysis, it is concluded that the equivalent loading current at the 1^{st} output stage is $4I_0$ and the current flowing through C_1 and C_2 is also $4I_0$. Given the analysis above, the output voltage of the proposed negative charge pump circuit with loading current I_0 can be calculated as follows:

$$V_{out\_3rd} = -7V_{DD} + 4I_0 t / C_1 + 2I_0 t / C_3 + I_0 t / C_5 \\ = -7V_{DD} + I_0 t(4/C_1 + 2/C_2 + 1/C_5) \quad (1)$$

For a given area, the lowest output voltage is obtained only when $C_1=2C_3=4C_5=4C$:

$$V_{out\_3rd\,min} = -7V_{DD} + \frac{3I_0}{Cf} \quad (2)$$

In order to analyze the power efficiency, the input and output power is also calculated. For the input power, there are three sources:

$$P_{in} = 4V_{DD}I_O + 2V_{DD}I_O + V_{DD}I_O = 7V_{DD}I_O \quad (3)$$

Given the output voltage V_{out_3rd} and load current I_{load}, the output power is:

$$P_{out} = <V_{out\_3rd}> * I_{load} = 7V_{DD}I_{load} - \frac{3I_0^2}{Cf} \quad (4)$$

Comparing Eqn. (3) and (4), the power is dissipated on the MOSFET transistors when the gate is switched on and off. The power efficiency can be calculated as follows:

$$PowerEfficiency = \frac{P_{out}}{P_{in}} = \frac{7V_{DD}I_0 - \frac{3I_0^2}{Cf}}{7V_{DD}I_0} = 1 - \frac{3I_0^2}{Cf} \quad (5)$$

Equation (5) shows that higher power efficiency can be obtained by increasing the operating frequency of the charge pump circuit. However, this is not quite correct since the analysis so far has neglected the parasitic capacitance. A more accurate calculation of power efficiency can be approximately expressed as:

$$PowerEfficiency = \frac{P_{out}}{P_{in}} \\ = \frac{7V_{DD}I_0 - \frac{3I_0^2}{Cf} - \frac{3\alpha I_0^2}{C_C f} - \frac{3\beta I_0^2}{C_{MOS} f}}{7V_{DD}I_0 + (E_{C\_C} + E_{C\_MOS})f} \\ = \frac{7V_{DD}I_0 f - 3(\frac{I_0^2}{C} + \frac{\alpha I_0^2}{C_c} + \frac{\beta I_0^2}{C_{MOS}})}{(E_{C\_C} + E_{C\_MOS})f^2 + 7V_{DD}I_0 f} \quad (6)$$

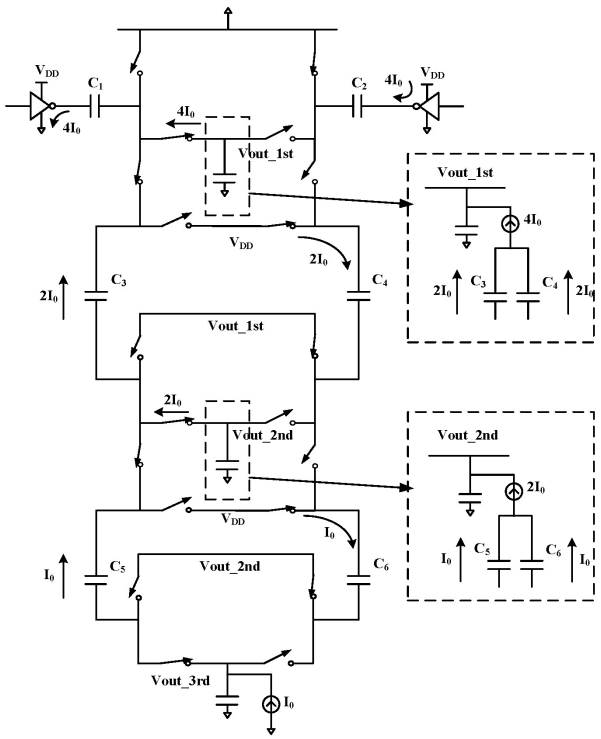
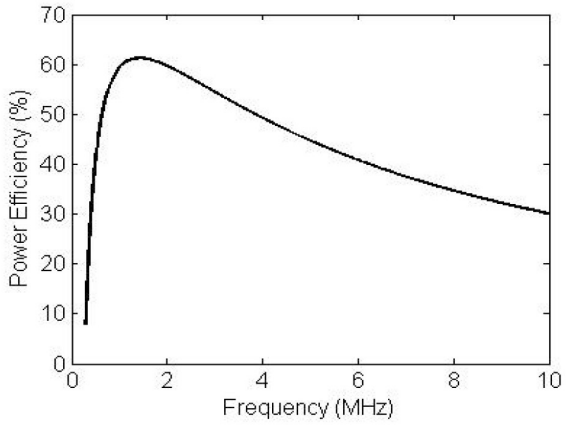


Figure 6. Simplified circuit topology for the analysis of power, area, and frequency interaction.

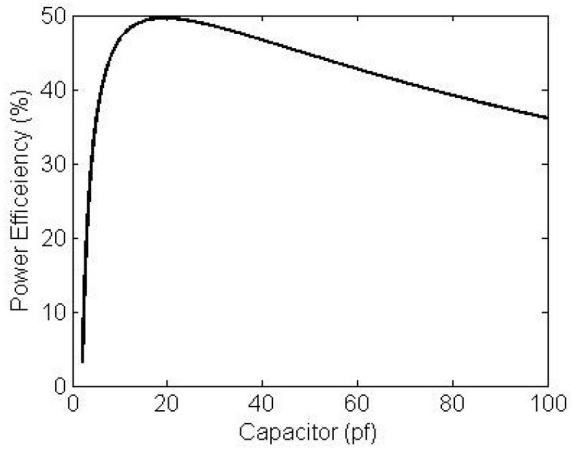
where C_C and C_{MOS} are the parasitic capacitance of MIM capacitors and transistors, respectively. Also $E_{C\text{-}C}$ and $E_{C\text{-}MOS}$ are the corresponding energy consumption due to the voltage switch which is constant within one period.

The value of αI_0 and βI_0 represents the equivalent current flowing through the parasitic capacitors and is determined by the type of technology used. In Eqn. (6), the input power is larger than $7V_{DD}I_0$ since the charging current has to be larger than I_0 in order to restore the additional charge dissipated on the parasitic capacitors. The load current flowing through the capacitors will reduce the output voltage and is a source of power consumption. However, the voltage switch on the parasitic capacitors only consumes power and has no effect on output the voltage.

Figure 7 shows the numerical simulation of power efficiency as a function of frequency and area. While the frequency increases, the power efficiency increases first and then decreases as shown in Fig. 7(a), which means, for a given area, there always exists an optimized switching frequency that could provide a maximum power efficiency. As shown in Fig. 7(b), when the area of capacitors increase to a certain value, the power efficiency starts to decrease since the parasitic capacitors from the MOS transistors dominates the power performance. The parameters of the charge pump circuit can be optimized by sweeping the frequency and area repeatedly until the maximum power efficiency is obtained.



(a)



(b)

Figure 7. Numerical simulation of power efficiency as a function of frequency and area: (a) Power efficiency vs. frequency @ $C=2C_C=2C_{MOS}=50pf$, V_{DD}=2.5V, $I_0=40\mu A$, and $\alpha=\beta=25\%$; (b) Power efficiency vs. area @ $V_{DD}=2.5V$, $I_0=40\mu A$, $Freq=5MHz$, and $\alpha=\beta=25\%$.

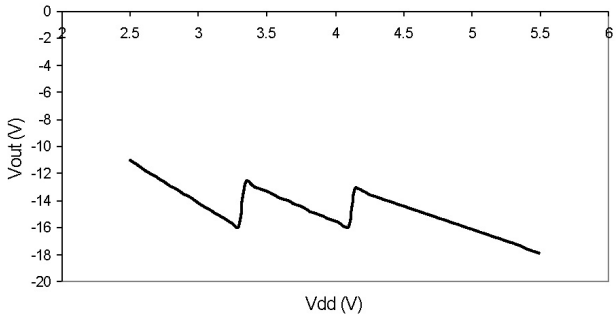
V. CIRCUIT SIMULATION AND OPTIMIZATION

As discussed in section III, the capacitors in the third stage should be replaced by two caps in series in order to avoid the use of fringing capacitors, which will increase the area by four times. Based on the analysis above, in order to have the maximum voltage gain, the capacitors from the stage should be resized as 4:2:1. As a result, the area cost of the two capacitors in series is acceptable since the last stage has the minimum capacitance. However, in order to reduce the parasitic capacitors, capacitors from the 1^{st} to the 3^{rd} are sized as 8:4:1 ratio.

In order to verify the effect of capacitance on the output voltage and power efficiency, the proposed charge pump is simulated at 1MHz with a current load of $40\mu A$ using 0.18μm high voltage LDMOS technology. The area discussed below is the overall area of the negative charge pump circuit which is proportional to the capacitance. As shown in Fig. 8(a), the output voltage is inversely proportional to the area and is not related to the parasitic capacitors expected in Eqn. (2). The interaction between the power efficiency and area in Fig. 8(b) meets well with the numerical simulation results in Fig. 7(b). Simulation of the charge pump in Fig. 8 shows an optimized area of $0.5\ mm^2$ by considering both output voltage and power efficiency.

Another important issue in charge pump operation is the operating frequency. Figure 9 shows the output voltage and efficiency as a function of operating frequency. The output voltage is inversely proportional to the switching frequency as shown in Fig. 9(a) as expected in Eqn. (2). The charge pump has a maximum efficiency of 50% at around 1MHz switching frequency as shown in Fig. 9(b), which meets well with Eqn. (6). Considering both output voltage and efficiency, the optimized frequency of 1MHz is selected.

Given the optimized parameters, the proposed charge pump circuit is simulated with $40\mu A$ load current at 1MHz operating frequency. Figure 10 shows the performance of the negative charge pump with the area of 0.5mm^2 and supply voltage range from



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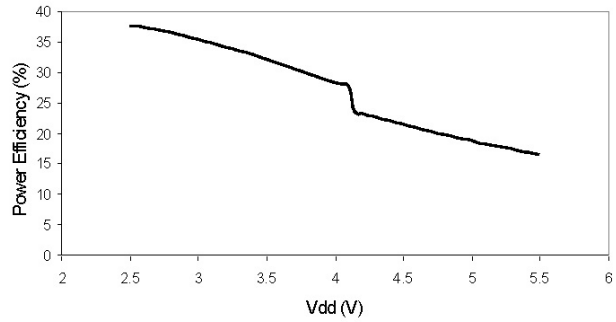
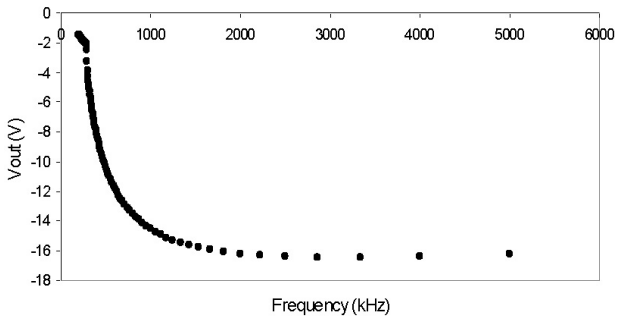


(b)

Figure 8. Output voltage and efficiency of the negative charge pump circuit as a function of supply voltage with *40 μA load current: (a) Output voltage vs. V_{DD} @ 0.25 mm² area; (b)* Efficiency vs. V_{DD} *@ 0.25 mm²* area.



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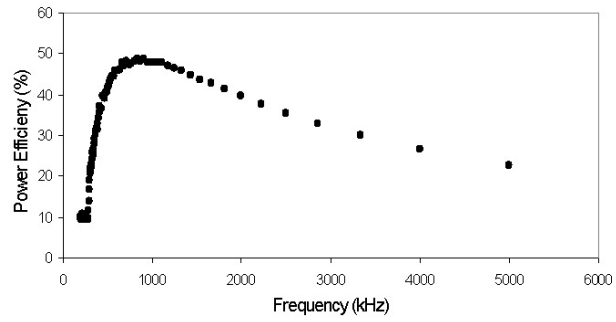
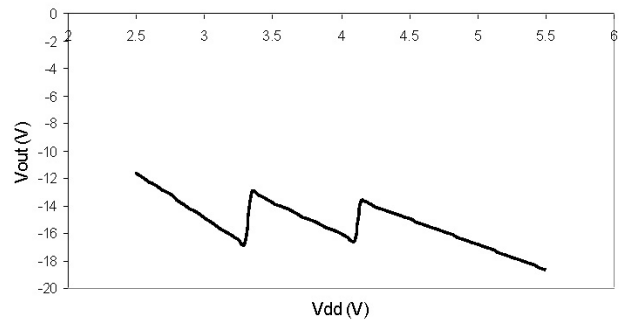
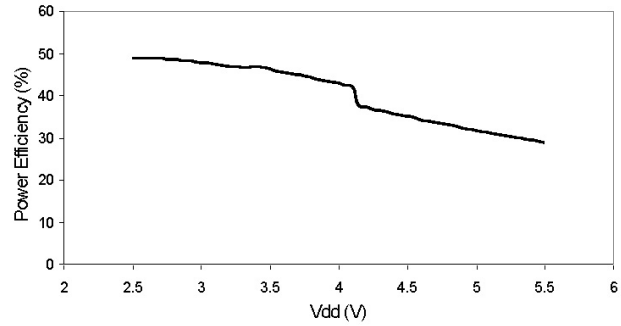


(b)

Figure 9. Output voltage and Efficiency as a function of operating frequency @ *0.5 mm²* area with *40μA* load current and *3V* power supply: (a) Output voltage vs. frequency; (b) Efficiency vs. frequency.



(a)



(b)

Figure 10. Output voltage and efficiency of the negative charge pump circuit as a function of supply voltage with *40 μA* load current: (a) Output voltage vs. V_{DD} @ 0.5 *mm²* area; (b) Efficiency vs. V_{DD} @ 0.5 *mm²* area.

2.5V to 5.5V. The output voltage is within *-15±3V* with variable voltage gains of -4X, -5X, and -7X separately. The power efficiency of the proposed negative charge pump circuit is from 30% to 50% which is lower than that of charge pumps using off-chip capacitors due to the high parasitic capacitance. In order to reduce the fabrication cost, the area is further reduced to 0.25 *mm²*. In this case, the output voltage is within *-14.5±3.5V* and the power efficiency is from 18% to 38% as shown in Fig. 8.

VI. CONCLUSION

In this paper, a negative charge pump circuit with variable voltage gains is designed and implemented using *0.18μm* high voltage LDMOS technology. The proposed charge pump circuit operates at 1MHz frequency with *40μA* current load with a wide power supply range from 2.5V to 5.5V. The clock overlapping issue is resolved by a four clock phase scheme. In order to have a fixed output voltage within *-15±3V*, the voltage gain of the charge pump circuit is variable from - 3X to -7X and is based on the supply voltage. Compared to the area size of *0.5 mm²*, power efficiency of the *0.25 mm²* designed is reduced by 10% at the same voltage gain for lower area cost. Measure re-

sults verified the functionality and performance of the proposed charge pumps. The results demonstrate the viability of the proposed design as a solution to the applications that require negative high voltage supply. This paper will be a good reference for programmable negative high voltage generator design.

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