A Novel Built-in Self Calibration Technique To Minimize Capacitor Mismatch for 12-bit 32MS/s SAR ADC

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ABSTRACT

This paper proposes a novel Built-in Self Calibration (BISC) technique for a 12-bit 32MS/s successive approximation register (SAR) analog-to-digital converter (ADC) using a single input to reduce the capacitor mismatch of the digital-to-analog converter (DAC) and to compensate the comparator input offset voltage. The proposed self-calibration scheme optimize the mismatch of the DAC by changing additional auxiliary capacitor array during calibration mode. In addition, in order to minimize the offset voltage of the comparator in the SAR ADC, a simplified voltage amplifier is proposed. The controller for the proposed algorithm operates as foreground operation to achieve low power consumption during operation. Compared to the converters that use the conventional procedure, INL and DNL are reduced by about 47% and 52%, respectively. The prototype was designed using 130nm single poly 6 metal standard CMOS technology. The ADC achieves a SNDR of 65.6 dB and consumes 4.62 mW. The ADC core occupies an active area of only 240μm× 298 μm using 1.2V supply and the sampling rate of 50 MS/s.

Index Terms: Built-in Self Calibration, SAR, Analog-to-Digital Converter

I. INTRODUCTION

Both digital and analog circuits test technology have been developed for nearly 40 years and have evolved into hardware and software based testing techniques. In early years, a test bench had to be designed and constructed for each circuit.

Later, automatic test equipment (ATE) has been used for a general test solution for most devices. During the use of the ATE, the complexity and density of the circuits increased dramatically while better quality and reliability were required by consumers and the market at the same time.

While the cost per chip has been decreased with advances in fabrication, the cost for test has not been decreased more than expected in the market. Especially, as analog circuits need a variety of target specification, built-in-self-test (BIST) methodology has been developed to reduce the total cost. Although the chip size is increased, the total cost can be reduced by using BIST as the cost for test can be reduced. Both external ATE machines used in the IC production stage and embedded test solutions such as BIST required for chip diagnosis and test are necessary in the design of modern electronic systems. The need to adopt or establish automated testing standards has been recognized as essential for higher yield and lower cost by most manufacturing companies. However, no such automatic process exists for mixed-signal circuits where the interface between digital and analog components is impossible to be directly accessed by the test circuit and equipment. Moreover, additional pin count is most likely required. This paper investigates a novel self-calibration approach for BIST in mixed-mode integrated circuits in SOCs.

The advancement in fabrication and design technology enables the integration of various digital and analog modules, and it has helped to bring single systems-on-chips (SOCs) [1][2]. Traditional circuit components developed as reusable cores are now integrated into one complex SOC. Most SOCs include a microprocessor, DSP processor, memory, RF components, analog block, and application specific CMOS logic units. In addition to digital units, analog and mixed-signal circuits are becoming essential parts of SOCs and wireless modems including transceiver also have been integrated into SOCs.

Analog and mixed-signal circuits have been widely used for multimedia, wireless communication, networking and control systems [3]. For example, the

emerging applications such as micro-electro-mechanical systems (MEMS) and application processor for mobile devices are integrated with electronic circuits in a single substrate and analog circuitry is essential to enable interaction between digital logic blocks and other blocks. It is expected that most future ICs will be mixed-signal circuits rather than pure digital logic or analog logic.

Figure 1 shows an example of a mixed-signal SOC. The most common analog circuits are analog to digital converters (ADCs) and digital to analog converters (DACs) to interface digital processors with the real world. It is also common that complex mixed-signal SOCs include more than one ADC and DAC. These data converters require anti-aliasing filters and reconstruction filters to remove aliasing noise [4]

Digitally assisted analog design [5][6] and integrated transceiver calibration [7][8] approaches are gaining popularity in ensuring efficient and reliable mixed-signal systems in nano-scale CMOS technologies. One design aspect is to equip analog blocks with performance-tuning features that allow the recovery from process variations and faults. Examples of such tuning mechanisms include input impedance matching, gain and center frequency tuning for low-noise amplifiers [8]-[10], second-order nonlinearity and mismatch correction for mixer [11]-[13] as well as linearity enhancements for baseband filters [14]. The other aspect related to digitally assisted design is the extraction of performance metrics on the chip to enable one-time or periodic calibrations. Many performance characteristics can be observed based on the output spectrum of a circuit under test (CUT) or a chain of analog blocks, which has led to on-chip spectrum analyzers that emulate conventional off-chip instrumentation [15][16].

In general, the analog BIST or BISC system consists of Device-Under-Test (DUT) whose output goes to ADC input directly or to ADC input through gain stage, FFT, and the control circuitry that connects

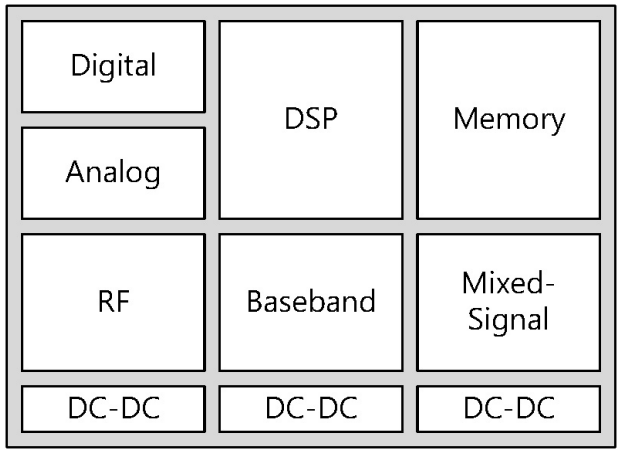

Figure 1. An example of a mixed-signal SOC.

the feed-back loop between the monotonic resistor or capacitor array and the output of FFT [17]. The BIST methodology in ref. [17] is one-chip solution that includes ADC in the chip to convert the output of DUT directly. Due to the inherent quantization error from ADC, the required ADC resolution to get suitable result is higher than 10 bit in ref. [17]. The required specification of ADC for BIST system in ref. [17] is 10-14 bit resolution and 30MHz sampling speed. It is evident that BIST or BISC system should be one-chip solution so that all of components such as ADC and FFT are integrated on the same die for cost reduction and test efficiency. In order to realize the integration, it makes more sense to use single-ended input ADC than differential input ADC for the on-chip BISC hardware implementation [18]. It is also well known that differential input ADC has several advantages compared to the single-ended input such as higher noise margin and doubled input range. However, in order to generate differential input from single-ended input, a balun is required for suitable input frequency range and this component is not only hard to be integrated but also has high cost, which is a big dilemma. It is usually not easy to design a high resolution ADC using single-ended input because of the inherent drawbacks of single-ended input such as noise issues. Especially, in SAR based ADC design case, there are several challenges that make it more difficult to accomplish high resolution using single-ended input due to the mismatch of capacitor array for charge-redistribution and offset voltage of the comparator.

In order to vanquish those problems, a novel calibration based mixed-signal mode circuit design technique is proposed for SAR ADCs, and the technique that uses an enhanced self-calibration approach to compensate the process variations method is proposed in this paper. In more detail, this paper presents a SAR based ADC design that uses a charge-redistribution DAC with a self-calibration feature in 130nm CMOS process to achieve a high resolution and low power consumption. The proposed ADC employs a novel self-calibration technique for the DAC to reduce the capacitor matching issue of the metal-insulator-metal(MIM) capacitors in nano-scale CMOS technologies and to obtain 12-bit resolution without dissipating extra power. The power consumption of the SAR control logic circuit is further reduced by highly optimizing the control logic using asynchronous circuits. The proposed controller measures the comparator offset due to mismatch of the capacitor array of the DAC during each bit conversion period and change the auxiliary capacitors for each DAC's capacitor to compensate any mismatch. The switch codes value for adjusted auxiliary capacitor arrays are saved once, and there is no additional power consumption during normal operation of ADC.

II. DEVICE MISMATCH ANALYSIS OF SAR ADC

A. DAC mismatch

The conversion linearity of the SAR ADC is subject to circuit component non-idealities. In case of charge redistribution SAR ADC, when matching is accurate, the SAR ADC performs an ideal binary search to convert the sampled analog input into an N-bit binary code. The resulting ADC transfer curve is shown as the dotted line in Fig. 2 for a 12-bit example. In this case, the conversion is free of any differential or integral nonlinearity [19].

The mismatch of capacitor is composed of global and local effects. The edge and the oxide effects of the capacitor are other two variables in different point of view. The relationship is given by the Eqn. (1).

$$\frac{\Delta C}{C} = \sqrt{K_{le}C^{-3/2} + K_{ge}C^{-1} + K_{lo}C^{-1} + K_{go}} \qquad (1)$$

where the K_{le} is the local edge effect factor, K_{ge} is the global edge effect factor, K_{lo} is the local oxide effect factor, and K_{go} is the global oxide effect [20].

When capacitor mismatch is present, the ADC transfer curve is highly distorted, especially when small capacitors are used for fast settling and to reduce power consumption. As a result, the decision levels may no longer be uniformly distributed over the full input range, e.g., the one indicated by the solid line in Fig. 2. The vertical and horizontal misalignments are known as missing codes and missing decision levels, respectively.

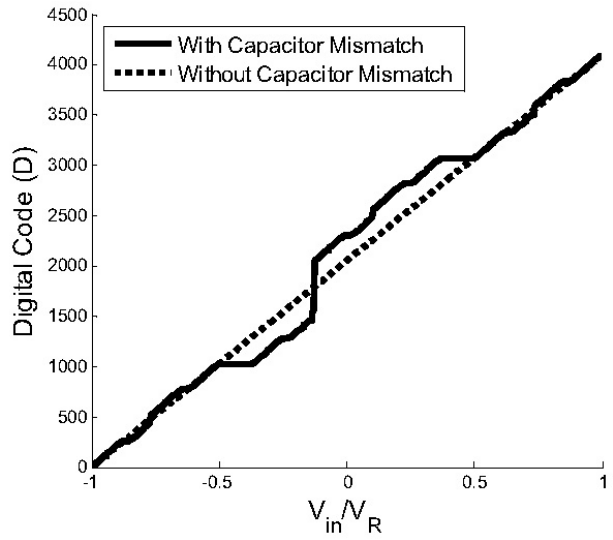

Figure 2 Example of transfer curves of a 12-bit SA-ADC.

In ref. [21], the relationship between capacitor mismatch error δ and the resolution of N-bit charge redistribution SAR ADC is given by Eqn. (2) and (3).

$$N_{\max} = \log_2\left(\frac{1+\delta+\sqrt{1+2\delta-3\delta^2}}{2\delta}\right) \qquad (2)$$

$$\delta_{\max} = \frac{2^N}{2^{2N}-2^N+1} \qquad (3)$$

Equation (2) and (3) describe actually the same relationship in different forms. When the technology is definite, the capacitor mismatch error δ is fixed, the maximum value of capacitor array N can be calculated by Eqn. (2). On the other hand, when the technology is not definite, it can be chosen by the result calculated by Eqn. (3).

Figure 3 shows that the maximum possible resolution of a charge redistribution SAR ADC with a fully binary-weighted capacitor array depends on the matching of a unity capacitor in [22].

B. Offset mismatch

An ADC offset is a random additive error typically resulting from the comparator offset. In a single-channel ADC, the offset error creates a DC tone and the comparator is usually designed to have input-referred noise less than 1 LSB. With low power supply voltage, 1 LSB should be less than $V_{ref}/2^N bit$. For example, 1 LSB is 244.14 μV in the 12bit SAR ADC using 1V V_{ref}. The impact of the offset errors is much more detrimental in time-interleaved ADCs [23]. If $o(i)$ is the offset of the i_{th} channel, then, for a given input signal $v_{in}(t)$, assuming no other errors, the output signal can be written as:

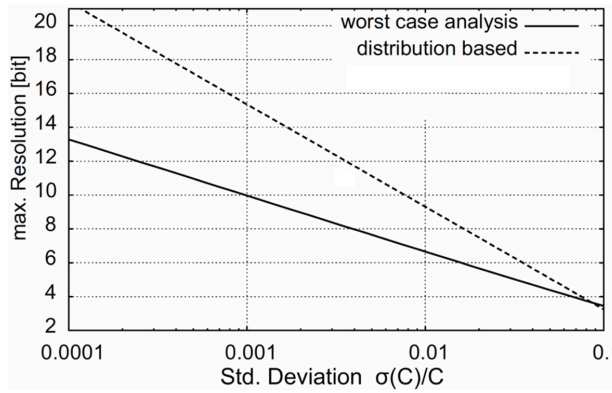

Figure 3. Maximum possible resolution of a charge redistribution SAR ADC with a fully binary-weighted capacitor array depending on the matching of a unity capacitor.

$$D_{out}(n) = v_{in}(nT) + o((n-1)\ mod\ \ M+1) \quad (4)$$

where mod is a modulo operation, $o((n-1)\ mod\ M+1)$ is a periodic discrete signal with a period equal to M. This means that in addition to our desired signal $v_{in}(t)$, the spectrum of the output signal will have tones at frequencies that are multiples of f/M. The magnitude and relative strength of these tones depends on the amplitude and the shape of the introduced periodic error signal.

The input referred offset of the comparator used in the ADC will possibly degrade the overall ADC performance, so it is better to be minimized. Such offset is primarily functions of both threshold mismatch and current factor mismatch, and transistor dimension as follows [24]:

$$\sigma(\Delta V_t) = \frac{A_{Vt}}{\sqrt{W \cdot L}} \quad (5)$$

$$\frac{\sigma(\Delta\beta)}{\beta} = \frac{A_{\beta}}{\sqrt{W \cdot L}} \quad (6)$$

where ΔVt is the threshold voltage differences, current factor differences $\Delta\beta$ ($\beta = \mu C_{ox} W/L$ [25]), W is the gate-width and L the gate-length, and the proportionality constants AV_t and A_β are technology-dependent.

The effect of the mismatch becomes serious with scaling process. The matching of the minimal size device degrades with scaling as can be seen in Fig. 4 for nMOS transistors. This is an important concern for the design of digital circuits since the device mismatch starts affecting the noise margin [26] and mismatch mitigation techniques cannot be widely applied due to their large area overhead [24].

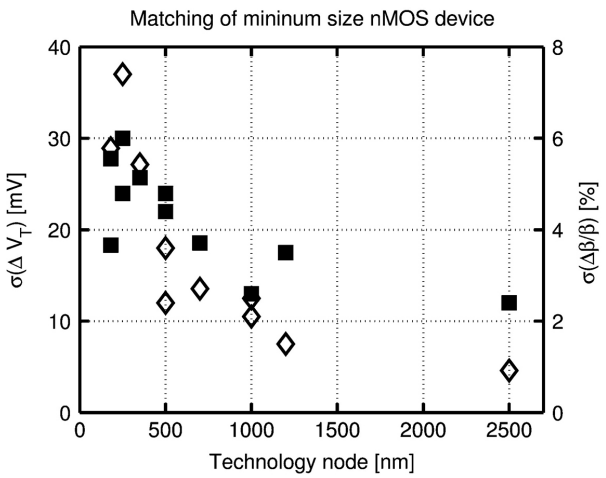

Figure 4. $\sigma(\Delta V_T)$ (black square) and $\sigma(\Delta\beta=\beta)$ (◊) for a minimal nMOS device in different technology nodes.

Obviously, according to Eqn. (5), the transistor sizes need to be increased by 4 times in order to reduce the offset by 2 times. This calculation shows that the sizing is not practical due to the excessive area and power consumption cost. However offset calibration is necessary to efficiently achieve good accuracy.

The basic idea for the calibration is to deliberately introduce some imbalance to compensate for the offset. Such imbalance can be either by capacitance loading [27] or current injection [28], or even voltage difference [29]. To calibrate the offset voltage, the differential inputs of the comparator are usually tied together to a certain common mode voltage, which should be the same when the comparator is in real operation, and the comparator output is monitored and fed back to the state machine to control the imbalance.

C. Gain mismatch

Gain errors manifest itself as a change in the slope of the transfer function of an ADC. The gain error comes from a difference in reference voltages or from the sampling operation (e.g. charge injection). The gain of the i_{th} channel can be expressed as $1 + \Delta g_i$, where Δg_i is the gain error in the i_{th} channel. The composite output of the time-interleaved ADC can be written as:

$$D_{out}(n) = v_{in}(nT) + \Delta g((n-1)\mathrm{mod}M+1)v_{in}(nT) \quad (7)$$

where $\Delta g((n-1)\ mod\ M+1)$ is a periodic discrete signal with a period of M and can be represented in frequency domain by discrete tones at frequencies kf/M, $k = 0..M-1$. If the input signal is a sinusoid with the frequency f_{in}, the mixing effect of multiplying the input signal with the periodic signal $\Delta g\ ((n-1)\ mod\ M+1)$ will create tones at frequencies $kf/M \pm f_{in}$.

III. CURRENT SELF-CALIBRATION TECHNIQUES FOR SAR ADC

As discussed in the previous section, the capacitor mismatches and offset error in SAR ADCs creates non-linearities in the ADC transfer function. Many different calibration techniques have been developed in order to fix the effect of mismatch-caused non-linearities. The techniques can be analog or digital circuitry [39].

A. Analog calibration

One group of analog techniques corrects the mismatches by subtracting a signal equal to the error caused by the mismatches from the output of the capacitive DAC. A single calibration DAC combined

with a digital logic can be used for this subtraction [40] or every capacitor in the main DAC can have its own calibration DAC [41].

The second analog offset calibration circuit was presented for a modified resistive divider based dynamic comparator in SAR ADC for biomedical applications [42]. The calibration circuit works on the basis of the comparator working as a zero crossing detector.

The third group of analog techniques corrects the mismatches by modifying the effective value of the capacitors in the main DAC. This can be achieved by using small trimming capacitors that are connected in parallel with the main DAC capacitors [43]. The mismatches can be measured by using either a known precise input signal or a self-calibration technique [40]. In the self-calibration technique, the difference between each capacitor in the array and the sum of all capacitors at the lower bit-positions is measured and later used for the mismatch correction.

B. Digital calibration

A digital calibration techniques measures or infers the values of the capacitors, represent them as a set of digital coefficients, and then corrects the non-linearities in the digital domain by calculating the weighted sums of those coefficients for each conversion [44].

The calibration method includes additional circuitry to assist the main circuits and uses a different algorithm. The algorithm in ref. [45] uses a dynamic error correction (DEC) capacitor to cancel the static errors occurring in each capacitor of the array as the first step upon power-up and eliminates the need for an extra calibration DAC.

Another group uses a charge-pump-based offset tracking method to reduce offset voltage of the comparators in flash-assisted time-interleaved SAR ADC. The comparator reflects the feedback information from the charge pump [46].

The recently published method is to use redundancy dithering technique [47]. The digital calibration technique of SAR ADC is based on the principle of internal redundancy dithering, a technique in which the bit decision thresholds are dithered by a pseudo-random bit sequence within the redundancy region [47].

C. Foreground & background calibration

Depending on the operation method to calibrate the mismatch error, there are two methodologies to correct the mismatch-caused non-linearities, which are foreground and background performed techniques. The foreground techniques require interruption of the operation of the ADC as can be seen in Fig. 5 [38], [48]-[54]. In Fig. 5, the additional DAC for design for test (DFT), called d-DAC, is added for calibration.

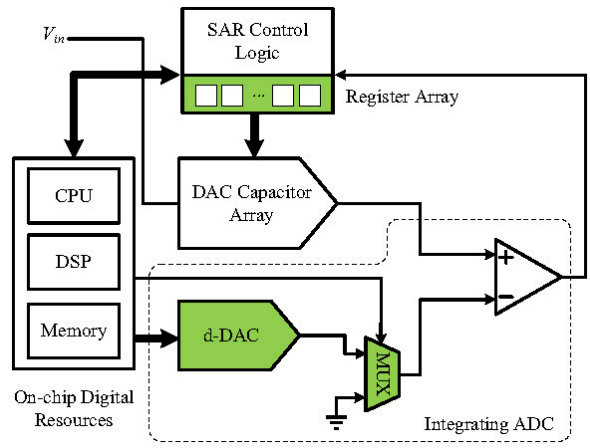

Figure 5. Self-testing and calibration architecture.

However, the circuitry cannot be used during operation of the ADC to save power. The background techniques do not require interruption of the operation of the ADC. However, the circuitries have to work during operation time of the ADC [44], [47], [55], [56].

IV. PROPOSED SELF-CALIBRATION METHODOLOGY

This chapter discuses a digital-compatible self-calibration approach for SOC building blocks such as DAC and comparator to improve the linearity of SAR based ADC. Since the calibrated performance is not sensitive to mismatches and process variations, the calibrated circuits can be easily used without additional cost. Simulation and experimental results verify the test performance of the proposed technique.

A. Offset calibration for comparator

The comparator in SAR ADC should be able to compare the voltage difference of at least 1 LSB. For example, for 10-Bit ADC with 1V reference voltage V_{REF}, the 1 LSB should be $1/2^{10} = 0.976$mV. However, the offset voltage of reported comparators used for offset calibration is larger than 10mV [30]-[33]. Therefore, in order to use the comparator for the proposed self-calibration technique for DAC mismatch, the offset voltage should be minimized.

Figure 6 shows that the schematic of the comparator with preamplifier for the SAR ADC. The output of the *OR* gate is used for the *valid* signal for asynchronous clock operation. When the comparator is in the pre-charge operation, the valid signal is low because the two input voltage of the *OR* gate, i.e, two output of the comparator is low. When the comparator is in comparison operation and the operation is finished, the valid signal is high because the one of the

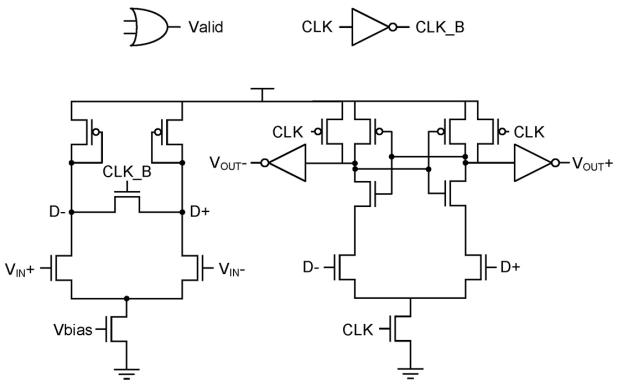

Figure 6. Schematic of the comparator with pre-amplifier for the SAR ADC.

input voltage of the *OR* gate, i.e, one of the output of the comparator is high.

The offset voltage can be compensated by controlling the capacitance, current or threshold voltage of the differential output pair (*D+;D−*) of pre-amplifier [31]-[34]. In order to reduce the offset voltage of the comparator, the proposed self-calibration techd niques change the capacitance of the output node of the pre-amplifier.

The capacitor arrays to control the capacitance of the output pair of the pre-amplifier consisting of MOM (Metal-Oxide- Metal) capacitors by using PMOS transistors are shown in Fig. 7 (a). Each node has 6 capacitor arrays *(C < 0 > ~ C < 5 >, C' < 0 > ~ C' < 5 >*. The capacitor array has the binary-weightr ed size like the capacitor array of DAC in the main SAR ADC, while the size of the unit capacitance is minimized as small as possible.

Figure 7 (b) shows that overall block diagram of the self-calibration approach for the comparator. When the self-calibration mode for the comparator is selected (E_n is on), DAC driver is disconnected from SAR logic and the voltage of the two inputs of the comparator goes to V_{cm}. The function of calibration is similar to the function of SAR ADC, and the SAR logic can be used by modifying the logic for the self-calibration ope eration. The modified SAR logic can be used for both normal ADC operation and self-calibration approach.

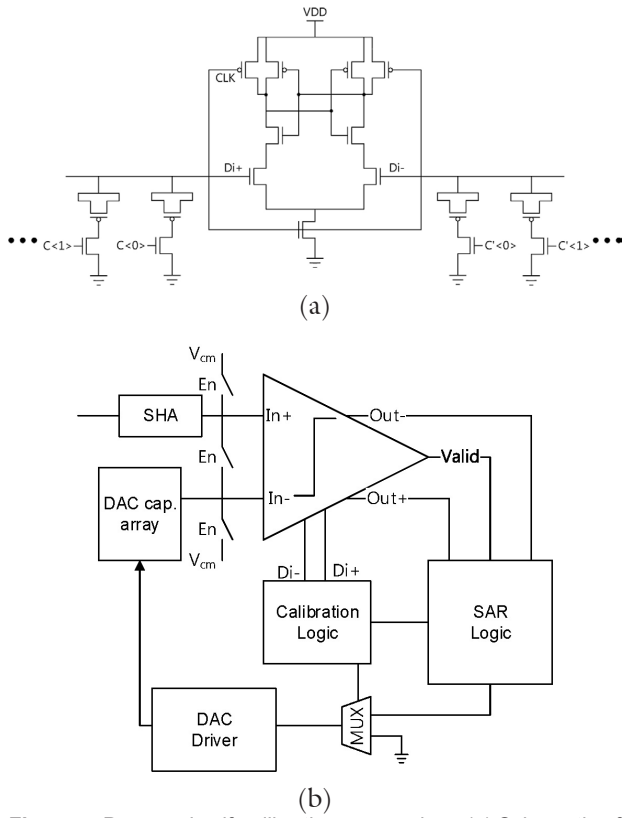

Figure 7. Proposed self-calibration approaches: (a) Schematic of the comparator with capacitor array to reduce the offset voltage; and (b) Block diagram for the self-calibration approach.

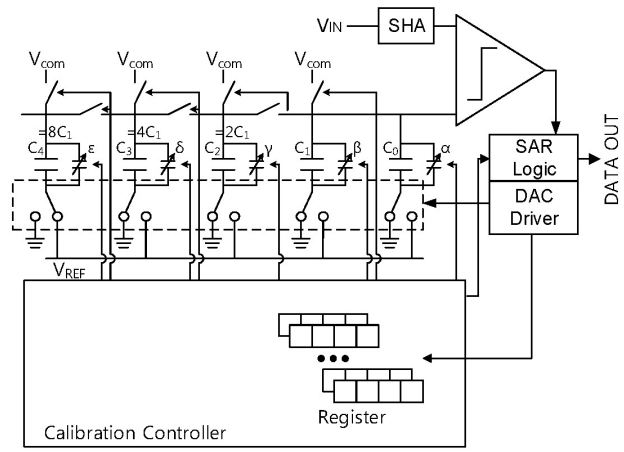

Figure 8. Proposed self-calibration strategy for the DAC in SAR ADC

B.DAC mismatch calibration in SAR ADC

Figure 8 shows the proposed SAR based ADC structure and the main conceptual strategy of the proe posed self-calibration for DAC in SAR based ADC to reduce mismatch error. The proposed self-calibration method adjusts the auxiliary capacitors that are connected in parallel to each capacitor (*C*0,*C*1,*C*2,…,*C*4 in Fig. 1) of the DAC to minimize the mismatch error of the DAC in SAR based ADC. In calibration mode, the auxiliary capacitances are determined using 4-bit control codes, then the digital code to adjust the auxiliary capacitors is stored in the register with 4-bit word-line. For 12-bit SAR based ADC, 12 registers with 4-bit word-line are required to control the auxn iliary capacitance array to compensate the capacitance mismatch error. After all of the 12 codes are saved, the SAR based ADC operates without the calibration controller causing no additional power consumption.

The calibration controller controls the auxiliary capacitors so that the values of the binary weighted capacitors can be nearly mismatch-less values. Each auxiliary capacitors consist of four capacitors which are unit auxiliary capacitor and binary weighted capacitors of the unit auxiliary.

Figure 9 (a) shows the calibration cases and its diagram. The first procedure is to compare the unit capacitor, C_0 and C_1. Depending on the comparison outcome, auxiliary capacitor, α or β are added to C_0 or C_1 to make C_0 and C_1 equal. Any auxiliary capacitance is made larger than the mismatch capacitance, and the compensated capacitance using the auxiliary capacitance is a little larger than the ideal capacitance. In the second procedure, two unit capacitors, C_1 and C_0 are added, and the C_2 (=$2C_1$ ideally) and C_0+C_1 are compared, then the auxiliary capacitor array, γ is connected (added) to C_2. By repeating above operation, the auxiliary capacitors of $2^N C_{N+1}$ are controlled, and the calibration controller saves the each switching code of the axillary capacitors. If *D* case is selected in Fig. 9 (b), it means that *C*2 is larger than C_0+C_1. However, this case is avoided by making any auxiliary capacitance larger than the capacitance mismatch value assuming that the capacitance mismatch value in the given technology node is given. Therefore, the proposed algorithm always choose *C* case, and *D* case is never chosen, i.e. the auxiliary capacitor is only added to the left side. The flow chart of the proposed algorithm for self-calibration is in Fig. 10.

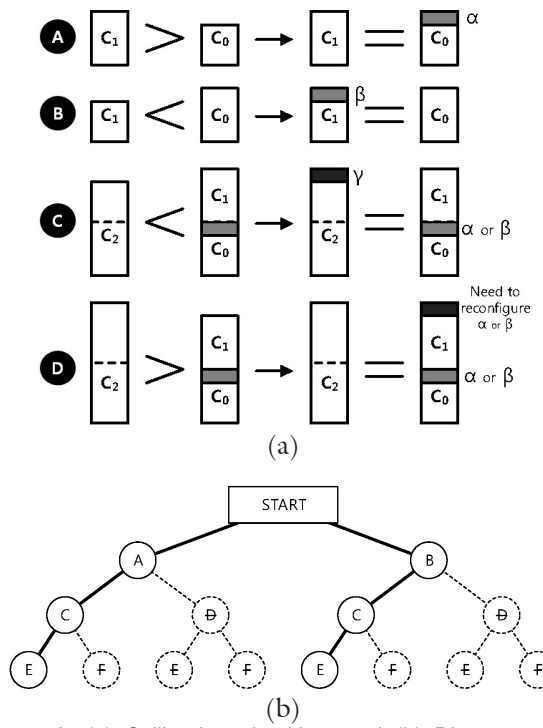

Figure 9. (a) Calibration algorithm; and (b) Diagram of the calibration process

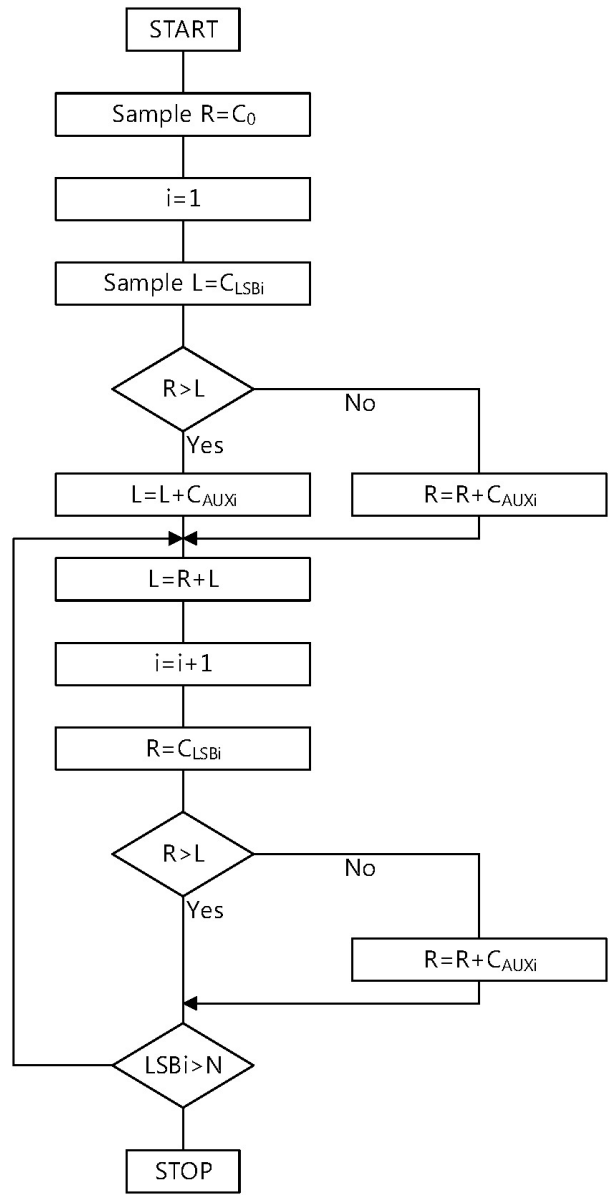

Figure 10. Flow chart of proposed algorithm for N-Bit DAC for self-calibration.

For example, firstly, compare C_0 and C_1 as following:

$$A : C_1 < C_0 \rightarrow C_1 + \alpha = C_0$$
$$B : C_1 > C_0 \rightarrow C_1 = C_0 + \alpha$$

Then, one of the two case, *A* and *B*, should be chosen. Regardless of the choice, the sum of C_1, C_0 and α is the same. Then, compare C_2 and the sum of C_1, C_0, and α.

$$C : 2C_2 < C_0 + C_1 + \alpha \rightarrow 2C_2 + \beta = C_0 + C_1 + \alpha$$
$$D : 2C_2 > C_0 + C_1 + \alpha \rightarrow 2C_2 = C_0 + C_1 + \alpha + \beta$$

In this case, Regardless of the choice of *C* or *D*, the sum of $2C_2$, C_1, C_0, α, and β is also the same. However, if *D* is selected, the β value should be included to $C_a \sim C_c$, which means that the algorithm needs to reconfigure C_c. Therefore, the proposed algorithm let *C* set be chosen, i.e. the auxiliary capacitor is only added to the left side. In order to do this operation, $2C_2$ are set up 10% smaller than $C_0 + C_1 + \alpha$ in second comparison, so that only *C* should be selected. The flow chart of the proposed algorithm for self-calibration is in Fig. 10.

The detailed procedure for the modified proposed algorithm is as follows:

1) compare C_0 and C_1 as follows:

$$A : C_1 < C_0 \rightarrow C_1 + \alpha = C_0$$
$$B : C_1 > C_0 \rightarrow C_1 = C_0 + \alpha$$

2) compare $2C_2$ and $C_1 + C_0 + \alpha$ as follows:

$$2C_2 < C_0 + C_1 + \alpha \rightarrow 2C_2 + \beta = C_0 + C_1 + \alpha$$

3) compare $4C_3$ and $2C_2 + C_1 + C_0 + \beta + \alpha$ as follows:

$$4C_3 < C_2 + C_0 + C_1 + \beta + \alpha \rightarrow 4C_3 + \gamma = 2C_2 + C_1 + C_0 + \beta + \alpha$$

4) compare $2^N C_{N+1}$ and $2^{N-1}C_N + 2^{N-2}C_{N-1} + \cdots + C_0 + \beta + \alpha$ as follows:

$$2^N C_{N+1} < 2^{N-1}C_N + 2^{N-2}C_{N-1} \cdots + C_0 + \beta + \alpha \rightarrow 2^N C_{N+1} + x = 2^{N-1}C_N + 2^{N-2}C_{N+1} \cdots + C_0 + \beta + \alpha + x$$

Each the value of α or β is decided by SAR-logic operation and the SAR-logic for main ADC is reused for the operation. To avoid a high-frequency clock generator and a pulse width modulator (PWM) for SAR logic, the proposed ADC uses an asynchronous control circuit to internally generate the necessary clock signals and to reduce switching power consumption. The generated clock signal is used for the comparator and SAR logic. However, for self-calibration mode, the SAR ADC uses input sampling clock frequency for the self-calibration controller and its operation because the self-calibration mode does not have to be run fast. In the proposed design, the sampling frequency is 32MHz and the calibration controller and the comparator in SAR ADC is operated by the same clock during calibration mode. The calibration controller and 4-bit registers are synthesized using digital standard cell library supported by the process foundry company.

Mismatch errors are inevitable due to process variations. Special layout techniques as well as laser trimming are used to reduce matching errors. However, these methods lead to significant cost increases. For the independent DAC for general purpose, the dynamic element matching (DEM) technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mis-matched elements so that all element values are nearly equal on the average [36]. However, because the DAC in SAR ADC operates with binary search algorithm normally and consists of binary weighted capacitor or resister, the DEM is not suitable technique for DAC in SAR ADC. The proposed approach in this paper is a viable solution because it is both area and power effective approach to reduce the mismatch errors.

C. An inverter based comparator to consider offset error

There is a need to convert the charge level quantities to voltage level quantities in order to compare the value of C_1 and C_0 in Fig. 11 which shows the conventional comparison concept of C_1 and C_0. In first step, C_1 and C_0 are charged to zero. Then, C_1 is charged to V_{REF} as next step. The voltage of the node V_1 is calculated as follows:

$$Q_1 = V_{REF} \times C_1 = V_1 \times (C_1 + C_0) \quad (8)$$

Therefore, the voltage of the node *V1* for the next step should be

$$V_1 = \frac{C_1}{C_1 + C_0} V_{REF} \quad (9)$$

By using the comparator, V_1 and $V_{REF}/2$ are compared. If there are assumptions that the values of C_1 and C_0 are same, the voltage of the node V_1 is should be $V_{REF}/2$. The voltage difference between V_1 and $V_{REF}/2$, ΔV is decided by the difference between the values of C_1 and C_0, i.e, $\Delta C/C$ in Eqn. (1). For instance, the ca-

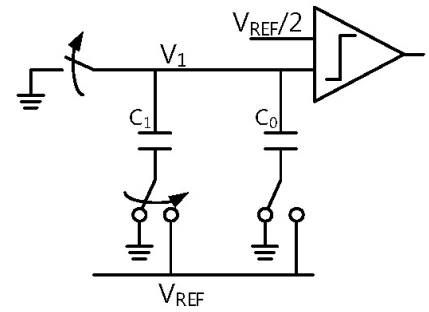

Figure 11. Conventional comparison concept of C_1 and C_0.

pacitor mismatch error δ is estimated about 0.005 for *0.18μm* standard CMOS process from the analysis of the Eqn. (1), where δ in Eqn. (2) is equal to $\Delta C/C$ in Eqn. (1) [35]. In addition, ideal ΔV is 4.5mV for 1.8V supply voltage and the realistic value should be smaller than 4.5mV with *0.18μm* standard CMOS process so that the ΔV is smaller than the offset voltage of normal comparator [37]. The reported offset voltage δV_{os}s are *1.68mV ~ 31.8mV* [30]-[33]. Therefore, the inverter based ΔV sensing circuit is proposed.

Figure 12 shows the schematic of the proposed ΔV sensing circuit. The circuit consists of three switches and one inverter. When the CLK_1 is high, VR_1 is connected to V_1 and then, V_2 and V_3 are connected so that the charge of C_2 is zero. Therefore, the charge of C_1 and C_2 is given by Eqn. (10) and (11), respectively.

$$Q_1 = (V_1 - V_2) \times C_1 = (VR_1 - \frac{VDD}{2}) \times C_1 \quad (10)$$

$$Q_2 = (V_3 - V_2) \times C_2 = 0 \times C_2 \quad (11)$$

When the CLK_2 is high, VR_2 is connected to V_1 and then, V_3 will be changed by Eqn. (12) and (13).

$$Q_1' = (V_1 - V_2) \times C_1 = (VR_2 - \frac{VDD}{2}) \times C_1 \quad (12)$$

$$Q_2' = (V_3 - V_2) \times C_2 = (V_3 - \frac{VDD}{2}) \times C_2 \quad (13)$$

Since the total charge is conserved, V_3 is given by Eqn. (14).

$$Q_1 + Q_2 = Q_1' + Q_2'$$

$$V_3 = (VR_1 - VR_2)\frac{C_1}{C_2} + \frac{VDD}{2} \quad (14)$$

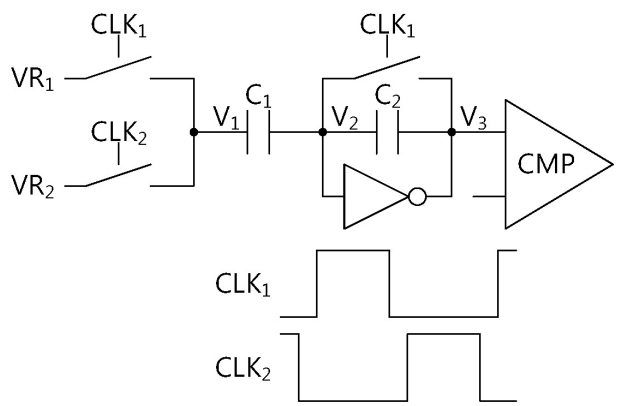

Figure 12. Schematic of proposed ΔV sensing circuit.

where V_3 is decided by the multiplication between the ratio of C_1 and C_2 and the difference V_1 and V_2. By adding the $(V_1 - V_2)$ term, V_3 is amplified. The maximum gain of the proposed circuit is about *3V/V* as verified in simulation.

Figure 13 shows the DAC with the proposed ΔV sensing circuit. The ΔV sensing circuits are only connected to capacitor array of DAC when the self-calibration mode turns on. The operation of calibration does not use the clock for DAC comparn ison but the ADC sampling clock. The ADC sampling clock is at least 10 times slower than the clock for DAC comparison, and the large switch size is not necessary. However, each size of the switch is different to reduce settling time for suitable opert ation margin. For instance, the size of the inverti er of the last sensing circuit connected to the $2^{10}C$ capacitor for MSB decision is 3 times larger than size of inverter of the first sensing circuit of unit C capacitor for LSB decision.

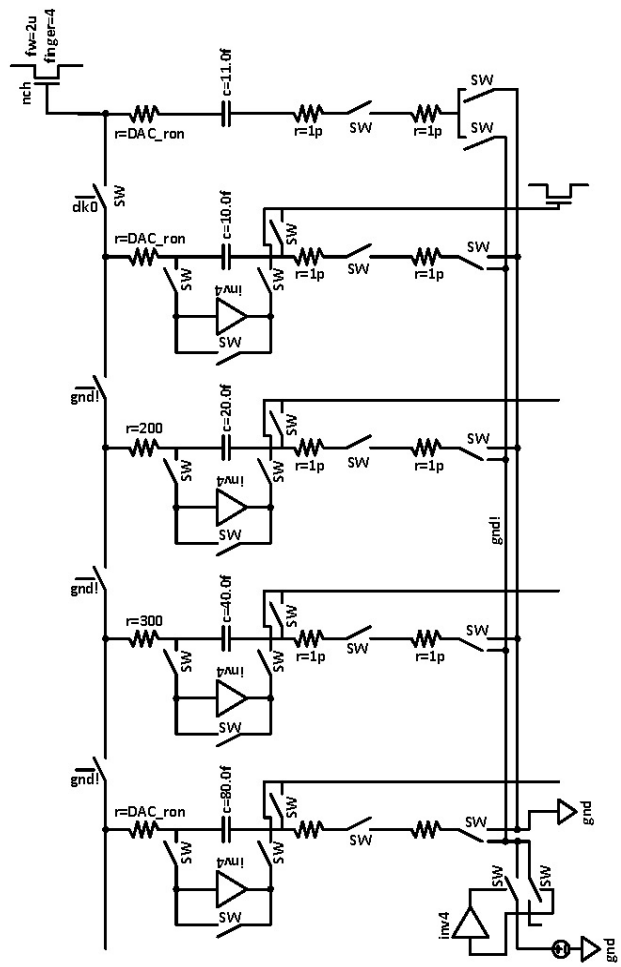

Figure 13. DAC with the integrated ΔV sensing circuit.

V. EXPERIMENTAL RESULTS

The proposed circuits were designed in a 130nm standard CMOS process. The control logic circuit for the self-calibration has been optimized for power consumption and area using asynchronous logic.

A. Offset voltage calibration

Figure 14 shows the simulated histogram of the offset voltage for the comparator. It contains 100 Monte Carlo simulations run with the random mismatch model from Eqn. (5) and (6), where $A_{Vt} = 3.8mV\mu m$ and $A_{\beta} = 0.8\%$, and the total input referred offset voltage was measured by applying slowly varying slope signals to the comparator inputs. The values of A_{Vt} and A_{β} are supported by the PDK (Process Design Kits) document of the foundry. The input differential transistor size is $1.2\mu m/0.15\mu m$. As shown in Fig. 14, 1-sigma the standard deviation for the input referred offset voltage is *14mV*. The result shows that the offset compensation is needed to reuse the comparator for the proposed calibration approach.

Figure 15 shows the compensation range of the digitally controlled capacitive calibration. 6 capacitor arrays control the offset voltage from *-40mV* to *40mV* so that the step of 1 digital code is around *2.5mV*, which means that a compensation range of *±40mV* is larger than the needed 3-sigma offset voltage.

Figure 16 displays the simulated histogram of the offset voltage for the pre-amplifier and comparator with the proposed self-calibration technique by performing 100 Monte Carlo simulations. After calibration, the residual offset voltage is around 3mV. The calibrated comparator is used for 32MS/s 12-bit charge redistribution SAR ADC using the conventional regular capacitor array.

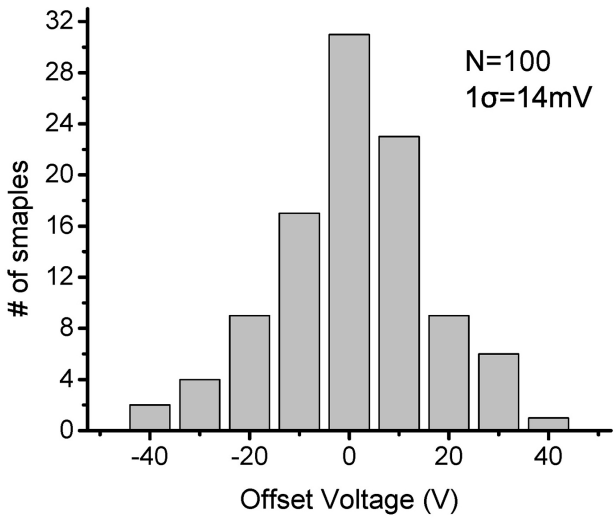

Figure 14. Monte Carlo histogram of the offset voltage of the comparator.

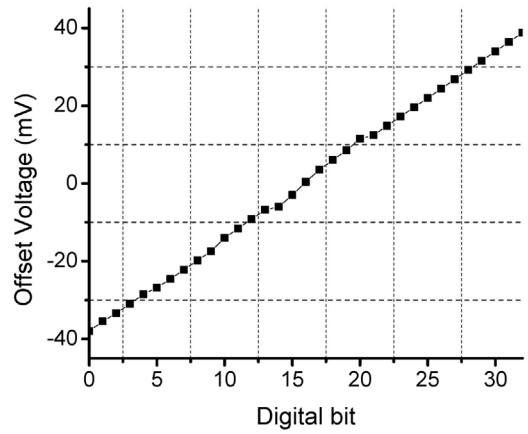

Figure 15. The compensation range of the digitally controlled capacitive calibration.

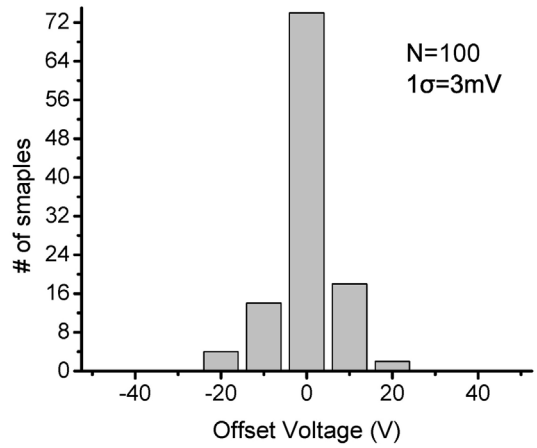

Figure 16. Monte Carlo histogram of the offset voltage of the pre-amplifier and comparator using the proposed calibration approach.

B. Capacitor mismatch calibration

The proposed calibration technique for DAC mismatch error was implemented for 32MS/s 12-bit charge redistribution SAR ADC using the conventional regular capacitor array. The SAR ADC has the DAC capacitor array having intentional 5% capacitance mismatch errors to verify the proposed technique.

The SAR logic, the comparator, and the capacitor array in the SAR ADC is implemented by *130nm* CMOS process and the switch controller to control the auxiliary capacitor array is implemented by Verilog code using behavior model.

Figure 17 (a) shows the raw transfer curve of the 12-bit SAR ADC for a case with 5% mismatch error of capacitance. The X-axis is the analog input and the Y-axis is the raw digital codes from the ADC output. Even if the example assumes 5% capacitor mismatch (σ=5%), the transfer curve only exhibits missing codes. The self-calibration treats the missing codes problem by learning the optimal bit weights, and linearity of the transfer curve can be fixed.

Figure 17 (b) shows the calibrated raw transfer curve with the proposed calibration technique of the 12-bit SAR ADC with +5% mismatch error of capacitance. Compared to Fig. 17(a), the linearity has improved conspicuously with the calibration approach.

The summarized overall performance of the proposed SAR based ADC is shown in Table I. The proposed ADC achieves an ENOB of 11.08 bit and SNDR of 65.2 dB for 16 MHz input frequency. At 32 MS/s, the average power consumption including the output buffers and the offset controller is 3.57 *mW*.

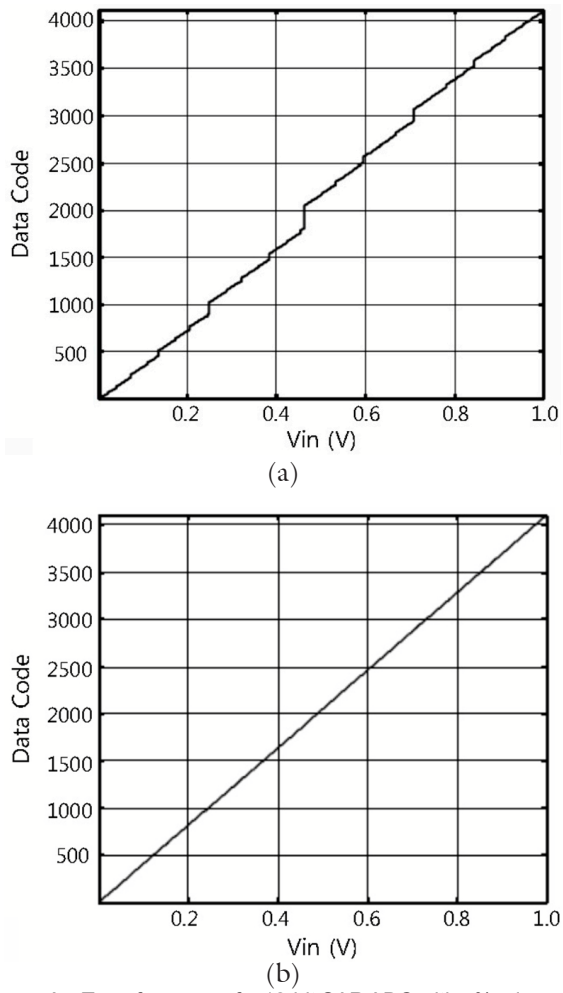

Figure 17. Transfer curve of a 12-bit SAR ADC with 5% mismatch error of capacitance: (a) without proposed calibration technique; and (b) with proposed calibration technique.

Table I. Performance summary for the proposed SAR ADC.

Process	130 nm
Supply	1.2V
Input range	0.2 ~ 1.2V
Sampling rate	32 MS/s
DNL /INL (LSB)	-0.87~0.91 / -1.86~1.12
ENOB	11.08 @ Fin = 16MHz
SNDR	65.2 dB
SFDR	76.1 dB
Power	3.57 mW

Compared to the ADC operation without the offset controller, the power consumption is not increased because the calibration and its controller circuits are active only during the calibration mode before the main circuits are activated. In calibration mode, the power consumption of calibration controller is *723 μW*.

The simulated static performance for differential non-linearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 18. The peak DNL values are between -0.87 to 0.91 LSB and the peak INL values are -1.86 to 1.12 LSB. Figure 19 shows the dynamic performance of the proposed ADC with the data of simulated SNDR and SFDR vs. input frequency at 32MS/s. When the input frequency is 1 MHz, the ADC has peak SNDR and SFDR of 65.2 dB and 76.1 dB, respectively.

Figure 20 shows the layout and floor-plan of the core parts. The total occupied area including power-ring of the ADC is 0.072 mm^2, with the ADC core taking only 0.058 mm^2. The switches for capacitors are placed close to the capacitor arrays to reduce any parasitic components. The logic control circuit has

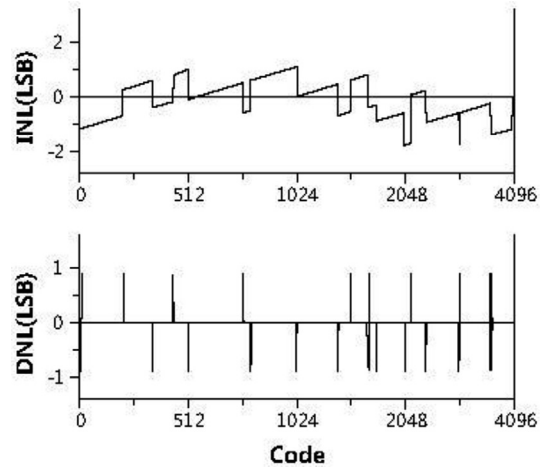

Figure 18. Simulated INL and DNL at 32MS/s.

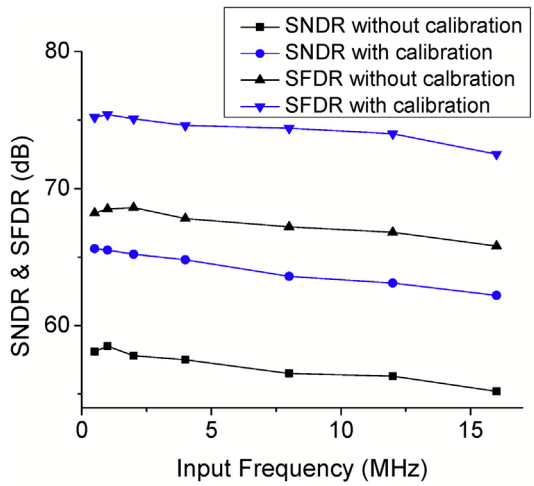

Figure 19. Simulated SNDR and SFDR performance versus input frequency at 32MS/s.

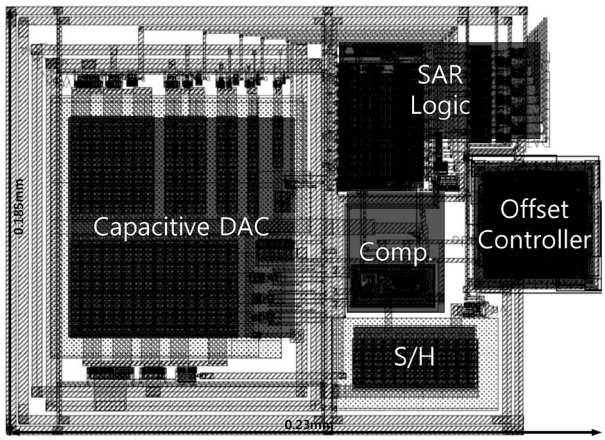

Figure 20. The layout of the proposed ADC.

been optimized for power consumption and area using asynchronous logic, and the layout of the digital logic circuit is more compact. The input signal capacitance for Sample and Hold Amplifier (S/H) and total capacitance of capacitive DAC are 1.05 pF and 20.24 pF, respectively. The size of the synthesized offset controller including registers is 0.0081 mm^2, and the area overhead of the proposed method is 12 %.

VI. CONCLUSION

A 12-bit 32 MS/s SAR based ADC with a novel self-calibration method has been presented in this paper to minimize the mismatch error of capacitive DAC in SAR based ADC. The proposed method diminishes the mismatch error of the DAC by one-time calibration process without complex procedure and extra power consumption, and the linearity of the ADC can be increased by 45% comparing with the conventional technique. Consequently, ENOB is increased by1.6 in spite of the use of single ended-input SAR based ADC. The ADC has been designed and simulated using 130nm standard CMOS process, the results show that the SNDR of 65.2dB for 16MHz input frequency and consumes 3.57 mW with output buffer. The proposed SAR based ADC with self-calibration feature will be a good reference to overcome the presumed limit of the resolution of SAR based ADC using single-ended input

The self-calibration approaches in mixed-mode circuits in a SOC has been proposed in this paper along with novel self-calibration design techniques for an ADC to reduce mismatch error and improve perfor mance. These techniques are essential in future SoCs and their viability has been demonstrated in this paper. The proposed techniques are good for not only calibrap tion of performance but also compensation for PVT variations.

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