A Defects Simulator for Robustness Analysis of QCA Circuits

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ABSTRACT

Although QCA (Quantum-dot Cellular Automata) is a promising nanotechnology to replace CMOS (Complementary Metal-Oxide-Semiconductor), it has several known reliability problems. Consequently, the design of robust QCA structures is a mandatory step towards the consolidation of this new technology. This paper presents a novel methodology for error analysis of QCA structures based on deterministic and random insertion of possible defects to either the cells and to the phase shifts of the clocking circuit. Further features presented are an evaluation of structures robustness and identification of the design elements most susceptible to the defects. Simulation results obtained from the implemented QCA Defects Simulator indicate the feasibility of the proposed error exploration methodology, also revealing starting-points for robustness improvements of known QCA structures.

Index Terms: QCA, robustness, defects modeling, clock shifts.

I. INTRODUCTION

According to the Moore's Law predictions, the amount of transistors in a single chip should be doubled every twenty four months [1]. Practical observations have shown that this forecast has been fulfilled until nowadays, thanks to constant miniaturization of CMOS transistors. The vast knowledge of the manufacturing process of these devices, as well as their reliability, made the CMOS technology widely used for the realization of integrated circuits since the late sixties. However, the size reduction of transistors shall not continue to occur uninterruptedly. There are physical limits about to be reached, as evidenced by the problems that are strongly observed in nanoscale devices, such as high power dissipation due to leakage currents [2].

The nanotechnology QCA (Quantum-dot Cellular Automata) [3] is a candidate for CMOS succession [2]. Its fundamental devices are called cells, which can be arranged in a row or in another particular pattern in order to enable the transmission and processing of information. It is important to highlight that the transmission and processing of information in QCA circuits occurs without flow of electrons (electric current), resulting in considerable less power consumption than in the traditional CMOS circuits [4]. Furthermore, the size of cells is typically in the range of few nanometers, so that the design of QCA circuits generally requires less area than its CMOS counterpart. Furthermore, high clock frequencies in the range of several THz are supposed to be achieved [4].

Despite its many advantages in comparison to CMOS, QCA has to overcome several challenges, such as the physical implementation. So far, prototypes of Metal-Island QCA and NML (Nano Magnetic Logic) devices have been successfully implemented [5] [6]. Molecular QCA have been widely studied [7] [8] [9] and possess good potential for succeeding CMOS, but no devices or even prototypes have been realized yet. Another challenge of QCA technology is its susceptibility to errors that may occur due to defective cells, caused by variations in the manufacturing process [10]. Consequently, several works focus on the creation of robust QCA structures [11] [12] [13] [14] as well as methodologies for error analysis in QCA circuits [15] [16] [17] [18]. In order to enable evaluation of circuit robustness and verification of reliability enhancing techniques, this work presents a QCA Defects Simulator based on a novel methodology for error exploration. By means of this methodology, it is possible iteratively insert distinct kinds of defects into the QCA structures and clocking circuit and analyze their impact to the structures operation. Furthermore, the methodology is designed such that it can be also applied for other nanotechnologies besides QCA as long

as positioning errors are critical for the properly operation of their devices. In this category, self-assembled devices such as DNA-based structures, Nanowires and CNFETs (Carbon Nanotubes Field Effect Transistors) may be highlighted. Some works present the investigation of the influence of defects in the operation of these nanodevices, proposing some error exploration methodologies [19] [20].

The remaining paper is organized as follows. Section II introduces the QCA technology, while section III focuses on conceptualizing defects and errors, presenting the classes of defects considered in this work. Section IV introduces the QCA Defects Simulator, including the novel error-exploration methodology. Section V discusses simulation results and section VI concludes the paper.

II. BACKGROUND

Quantum-dot Cellular Automata (QCA) is a new computation paradigm whose working principle is based on Coulomb interactions between electrons [21]. A cell, which is the basic unit of QCA, can be represented by a square including four circles - one in each of its vertices. The circles refer to quantum dots, which are the specific positions at which an electron can or cannot be. Each cell hosts two electrons confined in those dots. Due to the Coulomb repulsion effect, the two electrons must be as far apart as possible. Consequently, there are two possible logic states (opposite diagonals), which permits a binary logic. By convention, the maximum polarization states are called -1 and +1. A cell can continuously assume any polarization level within those limits. The interpretation of the logic state of a cell depends on two thresholds, which generally have the same absolute value and opposite signals. A polarization value within the boundaries defined by such thresholds may be considered as undefined logic. Nonetheless, the values between -1 and the negative threshold define logic 0, while +1 and the positive threshold delimit the logic 1 region.

QCA cells may be arranged in such a way that is possible to transmit information and to perform logic operations. In the following, representative QCA structures are detailed.

A. QCA Basic Structures

1) Fundamental Components

A QCA Fundamental Component is defined in this work as an arrangement of cells designed under the purpose of transporting and distributing information within a logic component, circuit or even serving as interconnection element for systems comprised of many smaller structures.

The most basic QCA fundamental component is the straight wire, which can be constructed by arranging the cells side by side as an array. When the polarization state of the first cell of the array changes, subsequent cells tend to assume the same polarization state due to Coulomb interaction effect, enabling the information transmission through the wire without electric current flow.

While the straight wire perform logic states transport between aligned structures, the bent wire is used to construct the turning in large circuits.

Besides the wires, the fanouts comprise another important category of fundamental components. They are responsible for the signal distribution task, by ensuring the logic state propagation through different aisles. The fanout of 2 distributes a single signal into other two directions, while the fanout of 3 propagates it into three distinct paths within the structure.

Fig. 1 depicts the aforementioned fundamental components.

2) Logical Components

A QCA Logical Component is defined in this work as an arrangement of cells designed to implement an elementary logic function. The NOT and the Majority, illustrated in Fig. 2, may be considered as the essential gates for QCA, since any other logical component may be implemented from them [7].

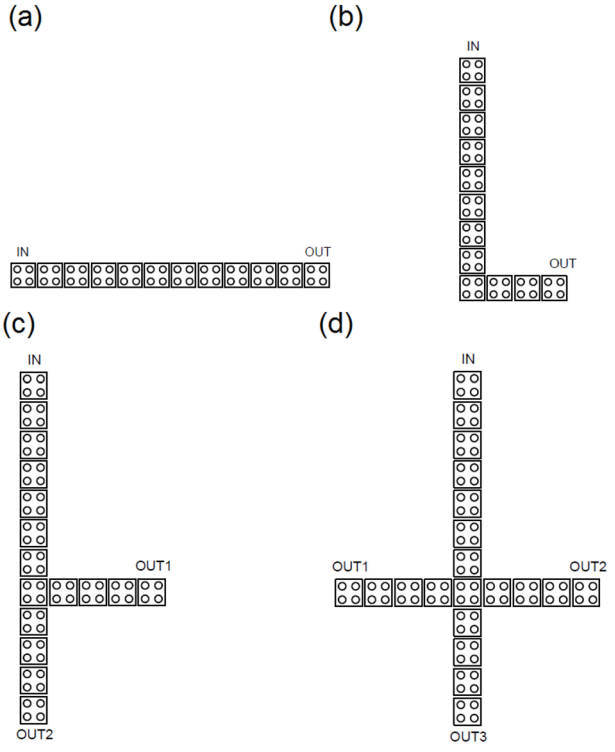

Figure 1. Four of the most important QCA Fundamental Components: (a) A straight wire (b) A bend wire (c) A fanout of 2 (d) A fanout of 3.

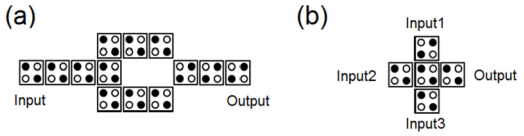

Figure 2. Fig.2 The basic QCA Logical Components: (a) A NOT gate (b) A majority gate

3) Circuits and systems

In the context of this work, a QCA circuit may be understood as a collection of components combined together in order to perform a more specific logic function, i.e. full adders [22] [23], multiplexers [24] and memory cells [25].

A QCA system, in turn, comprises a set of circuits and components that are interconnected in order to process a higher level function, i.e. Ripple Carry Adders (RCAs) [14], processors [26] [27], routers [28] [29] and memory architectures [30].

4) Clocking

One of the main issues of QCA circuits is the switching of QCA arrays, *i.e.* the change of an array of cells from one state to another. For example, when a polarization change in the input cell of the QCA wire in Fig. 1(a) suddenly occurs, the array of cells assumes distinct polarization states at the same time. This could cause the reach of a metastable state of the system which might lead to a significant delay or even to the inability to perform logic or information transport [31]. Adiabatic switching provides a solution for that problem [3]. In its first phase, the interdot barriers of the cells are decreased, removing gradually their old polarization values until they are depolarized. The second phase of adiabatic switching consists in raising cells interdots barriers at the same time as a new state is being applied to the input. The increased interdot barriers allow the repolarization of the cells into well-defined bistable states, reaching the ground state corresponding to the new inputs.

External signals should control the devices adiabatic switching. Those signals are called clock signals, which are provided by an external clock circuit. Interconnects of such external circuit should be positioned underneath the QCA layer, being able to deliver the clock signal to every cell in the system. The inter-dot potential barrier control occurs by means of the interactions between the cells electrical field and its counterpart created by the flow of the clock signals through the interconnects.

A clock signal has four sequential phases: Switch, hold, release and relax [3]. The inter-dot barriers of a cell are differently managed in each phase in order to allow or deny the electron tunneling thus the logic state propagation or change. The conventional approach for the clocking design is to provide synchronous clock signals, i.e. each phase have an individual time of $\pi/4$ radians, which corresponds to a quarter of the clock signal period. Fig. 3 depicts the general behavior of the inter-dot potential barriers level associated to the clock phases.

In the switch phase, the inter-dot potential barriers are linearly raised from the lowest to the highest level possible. At this time, the cell is susceptible to external influences and are able to change it polarization level according to the electrostatic interactions among its neighbors.

In the hold phase, the inter-dot potential barriers are kept at the highest level achieved in the previous (switch) phase, so the cell is insusceptible to external influences despite the electrostatic interactions between itself and its neighbors.

In the release phase, the inter-dot potential barriers are linearly lowered from the highest to the lowest level possible. At this time the cell is able to depolarize. After the end of the depolarizing process, a cell shall not carry remainder polarization.

At last, in the hold phase, the inter-dot potential barriers are kept at the lowest level achieved in the previous (release) phase, so the cell remains depolarized until a new cycle restarts at the switch phase.

The cells of a QCA system are grouped into sequential subarrays, most known as zones. A single clock signal is applied in order to synchronize the polarization change process of all the cells within a zone. In the traditional clocking distribution model, the clock signal of a zone is naturally phase-shifted in relation to its counterpart of the adjacent zone, as depicted in Fig. 4. The phase shift P for the clock signals in the traditional model is given by the relation: $P = (\pi/2)\, i$, where i is a sequential zone identifier: $0 \leq i \leq 3$.

By means of the use of clock zones, a QCA subarray can perform some logic, has its states frozen and finally provide input to the next subarray, which must be in a distinct clock-zone. Moreover, this clocking

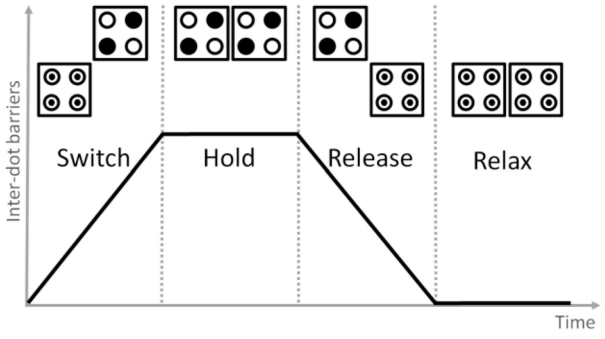

Figure 3. The cell inter-dot potential barrier behavior at the four distinct clock phases.

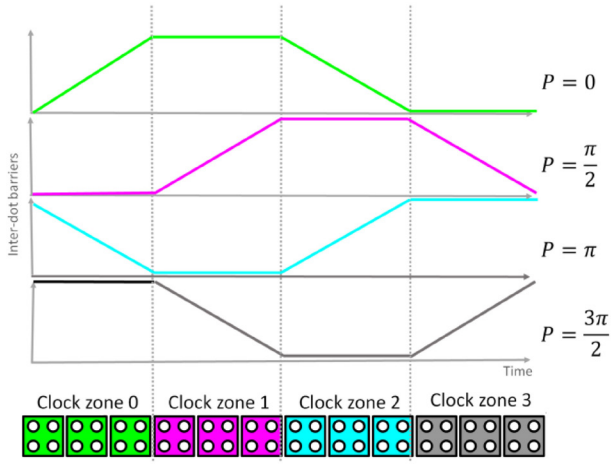

Figure 4. A QCA wire divided into four zones and their respective clock signals (depicted in the same colors). The signal phases (P) are indicated next to the graphs.

strategy allows the information synchronism, avoids backpropagation due to the QCA duplex nature (symmetric behavior) and increases the probability of successful switching by limiting the length of QCA wires in a circuit [3].

III. ERRORS IN QCA CIRCUITS

Errors are unexpected deviations in the behavior of a system. In the circuits context, an error occurs when, given a known input vector, the state of the outputs is unexpected. Errors are likely to happen due to the presence of defects or unusual conditions of operation.

A. Structural defects

Structural defects are flaws of the cells of a component or circuit, generally caused by manufacturing process variations. Defects can occur regardless of the technology and are subject of several researches for different technologies, such as CMOS [32] and Carbon nanotubes [33].

A defective structure can or cannot lead to an erroneous circuit behavior, depending on the integrity of the response of its outputs. Whether the structure is able to perform correctly its function, even when defects are present, it cannot be considered as erroneous. A great challenge for designers is to design reliable systems, which are able to get along with structural defects and other external factors.

Most of the reports in the literature regarding structural defects in QCA circuits are related to displacement and misalignment of the cells. Temperature effects are also occasionally investigated [6]. Defect classes of this work have a nomenclature similar to those reported in [17], which is based on an analogy to a two-dimensional crystal lattice. They are more detailed in the following.

1) Structural defects modeling

The defects modeling adopted in this work is depicted in Fig. 5. It comprises four defect classes, which were named accordingly to the classes reported in [17].

The dislocation defects are caused by cells that are moved around its axis (rotated), as depicted in Fig. 5(a), while the dopant defect occurs when a QCA cell has one or more extra or missing dots. Such situation is exemplified in Fig. 5(b). Futhermore, a misaligned (in relation to the horizontal, vertical or both axes) device, illustrated in Fig. 5(c), is called an interstitial-defective cell. The absence of the entire device is referred as the vacancy defect Fig. 5(d).

The consequences of a defect vary from one defect class to the others, implying in distinct levels of concerns on robustness. The effects of a dopant-defective cell to the behavior of a QCA circuit are almost always fatal. Besides the missing or extra dot hinders the freely switch of the cell between the logic states, it can also introduces wrong information to be propagated forward. On the other hand, a misplacement-related defect offers less damage to the circuit operation, since only significant positioning deviations are likely to induce the erroneous behavior of the circuit [34].

2) QCA Clocking Shifts Modeling

Besides the defective cells, the behavior of a QCA system may be substantially affected due to deviations in the clock signals [18] [35]. As previous exposed in the Section II, the clock signals are provided by an external circuit, which is also subjected to defects and unusual operation conditions, such as temperature effects. A defective clocking circuit may result in the addition of a standard deviation σ to the natural phase shift P of the clock signals. Since the QCA is highly dependent on a synchronous infor-

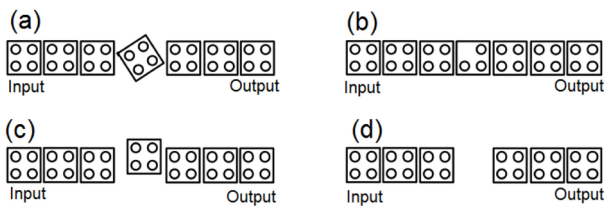

Figure 5. The four defect classes used in this work. (a) dislocation, (b) dopant, (c) interstitial and (d) vacancy. They are exemplified through a wire where the fourth (middle) cell is always defective.

mation flow, such unusual condition may lead the outputs of the QCA circuit to an erroneous state.

The phase shift P for deviated clock signals may be modeled as: $P = (\pi/2)\ i \pm \sigma$, where i is the sequential clocking zone identifier, such as $0 \leq i \leq 3$, and σ is the standard deviation introduced by the external clocking circuit defective condition. According to [35], σ values higher than $\pi/4$ radians would increase the probability of having two clocking zones whose phases are inverted, a condition that is unlikely in reality.

Thus, a reasonable interval for the clocking phase shift standard deviation is $0 \leq \sigma \leq \pi/4$. The regions shaded in gray on both graphs depicted in Fig. 6 represent the $\pi/4$ radians boundaries for the standard deviation σ in the clock signal phase. According to the model adopted in this work, the clock signal is allowed to assume any phase shift between such boundaries.

The standard deviations in the clock signals phases are likely to cause errors in the output signals of the QCA circuits, since they potentially affect the correct information sequencing. Such errors may manifest themselves in one of two possible ways, which are unwanted delays or inversions at the primary outputs [18]. The unwanted delay error occurs because the clocking zone attributed to the output cell latches out of sequence, so the information is propagated forward either sooner or later than expected.

Finally, errors due to inversions are likely to occur whether a out of sync latching takes place in a diagonal arrangement of QCA cells.

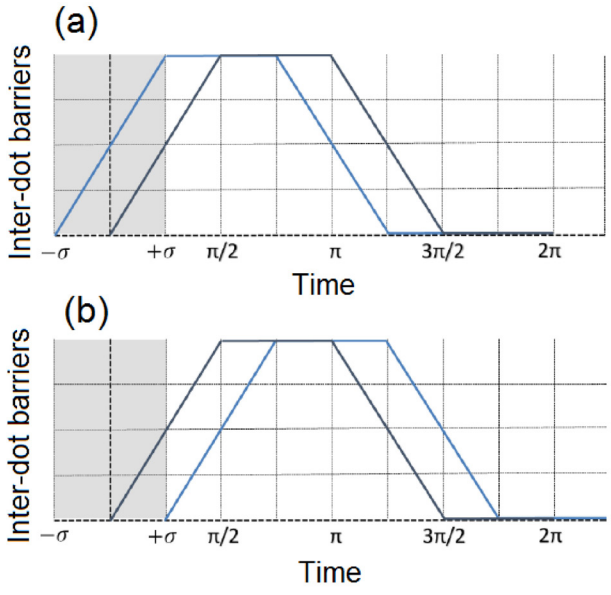

Figure 6. Two clock signals, depicted in blue, whose phases are advanced (a) and delayed (b) by π/4 radians relative to the references signals, shown in black.

IV. QCA DEFECTS SIMULATOR

This section introduces the QCA Defects Simulator developed in this work, which aims to analyze the likelihood of error events due to defective cells or phase-shifted clock signals. The simulator was implemented as an extension module to the widely used open-source simulation tool QCADesigner version 2.0.3, which was launched in the early 2000s through a joint effort of some researchers from the ATIPS laboratory at the University of Calgary, Canada [36].

The QCA error analysis module is based on the precepts of a novel methodology for errors analysis described in the next subsection.

B. Novel methodology

To date, the majority of the automatized methods for QCA errors analysis [16] [37] [18] are not flexible enough to deal with the simultaneous insertion of defects of multiple classes into the cells within a structure. Moreover, other current error analysis approaches usually use fixed parameters for the defects levels, as the displacement/ misalignment shifts, rotation angles and the number of extra/ missing dots in a cell [38] [10] and [39]. Despite those methods, a more complete tool for QCA error analysis is reported in [17]. It allows a flexible defects insertion by means of probability values and further settings. However, the paper neither reports results nor mention the existence of visual resources which are helpful to correlate defective cells to eventual erroneous behavior of the outputs.

This work introduces a novel simulation-based methodology for QCA error analysis, which provides support for two defect insertion frameworks. The first one allows the insertion of random phase shifts to the clock signals, while the remaining refers to the structural defects inserted into the cells of a structure. In the latter case, four defect classes can be freely combined. The testing process runs accordingly to one of three possible user-set probability models. The error detection relies on comparisons between simulations results of a reference circuit (defect-free) and of the very same circuit subjected to defects. Error events are registered for each simulation performed, so that when the whole process is completed, the percentage of error-free simulations can be obtained as well as a design heat map. The methodology flow chart is illustrated in Fig. 7. Subsections 1-3 provide a detailed explanation of each of the its steps, grouped into three primary categories.

1) Initial procedures

The initial procedures of the novel methodology require user interaction. They comprise the circuit selection, the parameters setting and the start of the iterative process for error simulation. First of all, a design

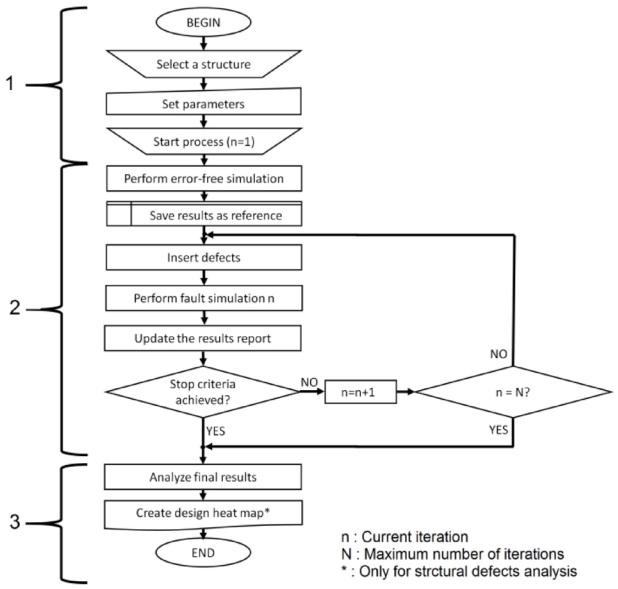

Figure 7. The methodology flow chart, where the main steps are identified with numbers 1-3.

to be analyzed must be selected. It should be implemented in a tool like QCADesigner. Once the design is selected, error simulation parameters must be set. The predicted parameters are briefly described in items a-h.

a) Sample interval: Defines the frequency with which the output signals of a QCA circuit should be read. The parameter value is a percentage of the frequency of the clock signals, e.g. a value of 50% means that the sample frequency is half of the frequency of the clock signals.

b) HIGH/ LOW thresholds: Determines the percentage of the value of polarization (+1) from which the logic state is interpreted as logic 1. Likewise, "LOW logic level" parameter determines the percentage of the value of polarization (-1) from which the logic state is interpreted as logic 0.

c) Error-free rate tolerance: Such value establishes the reasonable level for the error-free simulations rate percentage variation, i.e. the maximum variation allowed for the rate which may considered as stable.

d) Stable Iterations: Determines a number of iterations for such the error-free rate tolerance rate must be met before the round ending. For instance, if the tolerance is set to 10% and the number of stable iterations required is 100, the stop criteria to be accomplished is that the error-free simulations rate variation remains within that 10% variation limit for at least 100 successive simulation rounds.

e) Maximum number of iterations: Determines a maximum quantity for the number of simulation rounds. Such parameter aims to avoid that the stop algorithm remains stuck at any eventual unstable condition.

f) Simulator framework: This parameter regards to the choice of a framework for error analysis procedures. Two options are possible in such context: The first one, named "Structural defects", allow the insertion of fabrication defects, from one of those classes described in the section III, into the cells within a QCA structure. On the other hand, whether the "Clock Shifts" option is checked, values for shifts are randomly chosen within a pre-selected range for each one of the four clock signals in the circuit.

The next settings (items g and h) are dependent on whether the "Structural defects" framework is selected, otherwise no more parameters need to be set before proceeding to the methodology intermediate procedures.

g) Defect classes: This parameter defines one or more kind of defects that can be inserted into a cell during analysis. Several possibilities were previously detailed in section III. The actual insertion of a defect into each cell depends on the probability value assigned to every defined defect class. This assignment may vary according to the probability model chosen. Probability models are explained in the following.

h) Probability model: Defines the strategy of defect insertion into each cell of a design. There are three possible options for this parameter, as described in the following items.

- *Sequential: Defects are inserted into every cell in a design in a sequential manner. That means, a defect is selected out of the defined defect classes and inserted into a single cell at a time. Each defect class has a selection probability equal to the inverse of the total number of classes defined. Next, a simulation is performed. The two processes (defect insertion and simulation) must be run for all cells of the design.*
- *Assignable: One or more defects out of the defined defect classes might be inserted into the cells of a design. The probability of a defect insertion into each cell is manually assigned to every defined defect class. Defect insertion process must run repeatedly from the first to last cell in the design. Afterwards, a simulation is performed.*
- *Uniform: The defect insertion process for "Uniform" probability model is analogous to "Assignable" probability model. However, the probability value for defect insertion into each cell is now fixed. Its value is given by the inverse of the amount of cells in the design. Hence, it is expected to have an average of one defect per simulation*

Probability model selection as well as value assignment for probabilities should consider the device manufacturing process in question. That attribution may not be trivial, especially for emerging nanotechnologies such as QCA, since their manufacturing process is not yet established. Thus, the parameter setting may be based on other mature technologies, whose manufacturing processes are already well consolidated.

2) Intermediate procedures

The intermediate procedures of the methodology comprise the process of defect insertion, simulation

and error detection. First of all, a defect-free simulation is performed. The result of this simulation is saved as reference for determining error events in next simulations. After, defects are inserted either to the clocking circuit of the QCA system or into some cells of the design, according to the probability model set. Defect levels, e.g. absolute values of dislocation, interstitial and dopant (dot chosen to be removed) from each cell, as well as the clock phase shifts values are randomly defined. In the case in which the structural defects option is set in the "Simulator Framework" parameter, the interstitial displacement and misalignment limits correspond to fractions of the defective cell size (width/ length), within the 0 to 100% range. Thus, quantum dots may exceed the limits of a cell, entering the subsequent cell, depending on the interstitial defect values defined. Bigger values of the "Maximum Number of iterations" parameter might lead to more possibilities for error analysis, except when the round stop criteria is achieved at an early stage or the parameters "Probability Model" and "Defect Class" are set simultaneously to "Sequential" and "Vacancy". At this specific situation, the concept of defect level may not be applied and the defective cell in each simulation is pre-defined.

After the completion of the defect insertion, a simulation is performed for the QCA structure in which either the cells or the clocking circuit are defective. At this point, the analysis process is ready to start. The output signal(s) obtained from the latter simulation are compared to those from the reference. The errors eventually detected, along with a summary of the defect levels and clock phase shifts are registered. Moreover, the error-free simulations rate is iteratively updated and saved. The simulations round ends at the achievement of the stop criteria defined by the settings of the parameters "Error-free rate tolerance", "Stable Iterations" and "Maximum Number of Iterations". From this moment on, the flow continues to the design heat map creation that take place at the methodology final procedures step.

3) Final procedures

The final procedures of the methodology regard to the results analysis. Based on the registered information of all simulations, the percentage of error-free simulations is calculated. Further, a cross-reference between error events and defective cells is established, which allows the creation of a heat map.

A heat map is a graphical representation of the cross-reference between error events and defective cells. For each cell in a circuit, a color from a pre-defined range of colors is used to indicate how often defects inserted into that cell lead to an error. Fig. 9 shows the range of colors applied here.

C. Implementation

This subsection describes the module for QCA error analysis developed in this work, as an extension to the QCADesigner version 2.0.3.

Two distinct interfaces were designed for the module. Both of them may be accessed through the corresponding shortcuts added to the "Simulation" division at the QCADesigner main menu, as depicted in Fig. 8(a). Before starting a new round of simulations, all the methodology parameters defined in the Initial Procedures (subsection A) must be set through the first interface, which consists of a window entitled "Error Exploration Settings". Such interface is depicted in Fig. 8(b).

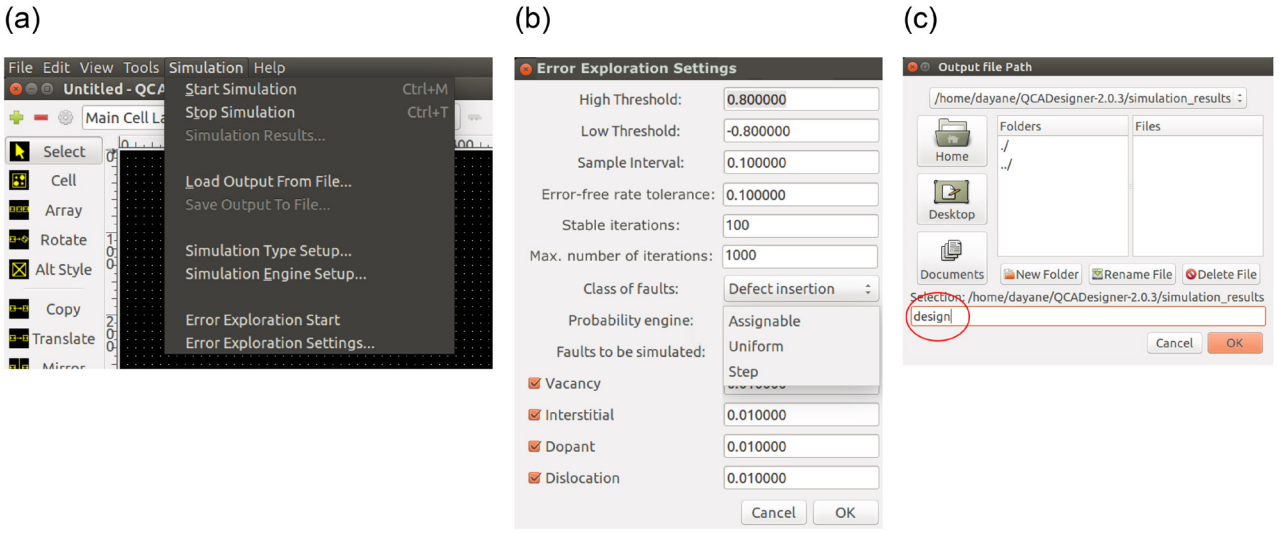

Figure 8. (a) The shortcuts into the Simulation menu in QCADesigner. (b) The interface for parameters settings. (c) The pop-up window for the selection of the path and the base name for output files.

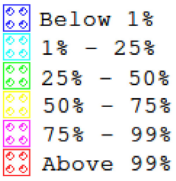

Figure 9. Colors and their respective ranges for heat maps. Defects inserted into dark blue cells led to error events in a circuit in less than 1% of the simulations, i.e. for every 100 defects inserted into the cell, no more than one of them resulted in an error event. Defects inserted into light blue colored cells led in 1-25% of all simulations to an error. Analogous reasoning may be applied to light green, yellow and pink colored cells complying with their respective percentage ranges indicated in the illustration. Defects inserted into red colored cells led in more than 99% of the simulations to an error.

Once all parameters are set, the user should proceed to the "Intermediate Procedures" step by clicking on the second shortcut inserted into the QCADesigner "Simulation" menu. This shortcut is labeled as "Error Exploration Start". By accessing the shortcut, a second pop up window, depicted in 8(c), is opened. Through this window is possible to indicate an output path and a base name for the files generated and updated along all the process.

Once a valid path and a valid base name are informed, the simulations round officially begins. The module for QCA error analysis might prompt some messages at the QCADesigner status bar while processing. For instance, while the module is performing a simulation or manipulating files, the message at the status bar indicates its current iteration and the pendant operations executed at that time.

Once a simulations round is complete, no more messages are shown at the QCADesigner status bar. The final files may be found in the path indicated through the window depicted in the Fig. 8(c). Their contents are updated to correspond the data gathered from the last iteration.

The heat map of the design is created. It consists of a design file similar to the original but with modified colors which represent the distinct levels of weaknesses of the cells throughout the QCA structure, as previously explained in the end of the subsection A.

V. RESULTS

Two different implementations of two logical components and one circuit (INVERTER [40] [12], MAJORITY [40] [11] and FULL ADDER [13] [14]) were subjected to defects insertion through the QCA Defects Simulator. Furthermore, four fundamental components (WIRE, BEND WIRE, FANOUT OF 2 and FANOUT OF 3 [16]) underwent the same error analysis module, under the clock shifts framework.

For all tests, QCADesigner simulation engine was set to "Coherence Vector". Further explanations about this engine may be found in [7]. Error simulation parameters "Sample Interval" and "LOW/HIGH Threshold" were set to 10%, 80% and 80% respectively. For the first set of experiments, Assignable probability model with a 5% probability value was used. As pointed out in Section IV, the definition of a probability model for defects insertion, as well as a probability value, may not be a trivial task for a non-mature nanotechnology such as QCA. Therefore, this value has been defined based on other mature well-consolidated technologies such as CMOS.

Results can be found in TABLE I, TABLE II and TABLE III. In the defects insertion framework, two probability models were used for all the four defect classes. Moreover, the clock shifts panorama considered uniform and random insertion of shifts in the signals from the clocking circuit. The fundamental components aforementioned are put into test for shifts within the subranges of 0 to $\pi/4$ radians and $\pi/4$ to $\pi/2$ radians.

For each defect insertion test performed, a design heat map was created. Six exemplary heat maps are depicted in Figs. 10-12.

Table I. Error-free simulations (%)*

	INVERTERS		3-INPUT MAJORITIES		FULL ADDERS	
	INV1 [3]	INV2 [11]	MAJ1 [3]	MAJ2 [10]	FA1 [16]	FA2 [17]
VACANCY	74.6	**86.1**	**60.6**	30.3	2.8	**16.2**
INTERSTITIAL	97.4	**99.9**	**94.3**	87.9	54.9	**76.0**
DOPANT	83.7	**88.6**	**75.8**	31.1	3.7	**26.2**
DISLOCATION	88.6	**93.9**	**78.5**	67.2	25.9	**51.0**

*Testing Framework=Defects insertion; Probability model=Assignable; Maximum Number of iterations=1000; Probability value for individual defect classes=5%.

Table II. Error-free simulations (%)*

	INVERTERS		3-INPUT MAJORITIES		FULL ADDERS	
	INV1 [3]	INV2 [11]	MAJ1 [3]	MAJ2 [10]	FA1 [16]	FA2 [17]
VACANCY	60.0	**83.3**	11.1	**89.9**	**26.6**	0.0
INTERSTITIAL	96.0	**100**	87.8	**98.9**	50.9	**83.9**
DOPANT	69.0	**80.8**	42.2	**85.2**	0.0	**37.4**
DISLOCATION	88.0	**90.8**	61.1	**95.2**	**77.2**	39.0

* Testing Framework=Defects insertion; Probability model=Sequential; Maximum Number of iterations=10 for interstitial, dopant and dislocation defect classes. 1 for vacancy defect class.

Table III. Error-free simulations (%)*

	SUBRANGES		COMPREHENSIVE RANGE (0 TO π/2)
	0 TO π/4	π/4 TO π/2	AVERAGE
WIRE	96.5	**72.3**	**84.4**
BEND WIRE	**96.8**	50.3	73.5
FANOUT OF 2	96.1	50.0	73.1
FANOUT OF 3	95.7	50.6	73.1

* Testing Framework=Clock shifts; Probability model=Uniform (fixed); Maximum Number of iterations=2000 per subrange.

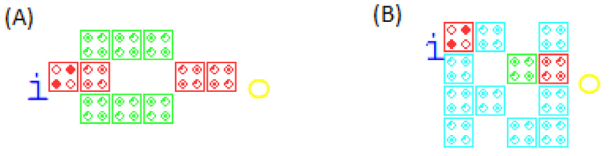

Figure 10. Heat maps of INV1 (A) and INV2 (B) for 1000 tests under vacancy defects where "Assignable" probability model was set.

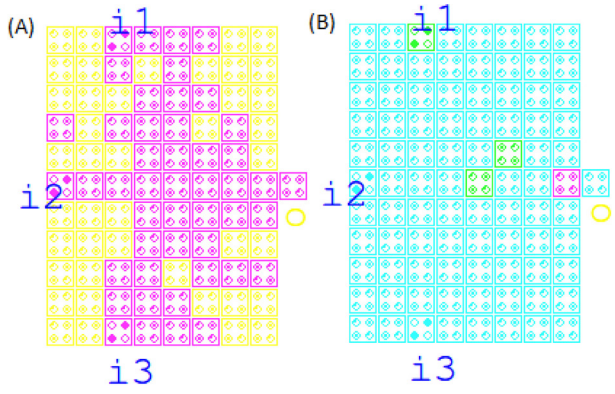

Figure 11. Heat maps of 3-input majority gate MAJ2 for 1000 tests under dopant defects (A) and interstitial defects (B). Probability model was "Assignable".

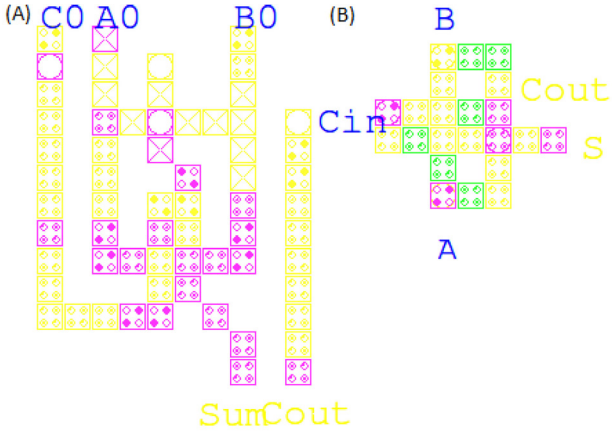

Figure 12. Heat maps of 1-bit full adder FA1 (A) and FA2 (B) for 1000 tests under dislocation defects where "Assignable" probability model was set.

D. Discussion

1) Structural Defects Insertion Test

Results shown in the Tables I and II indicate that INV2 had a higher percentage of error-free simulations for the probability models "Assignable" and "Sequential". Error-free simulation percentage for INV2 was always above 80%, and among all the circuits tested, it was the most reliable.

According to [11] majority gate MAJ2 is supposed to be more reliable than gate MAJ1, but the results of the tests revealed no superiority in terms of robustness for the probability model "Assignable". When the probability model "Sequential" was applied, MAJ2 had an absolutely higher performance in all classes of defects. One possible explanation for this is that MAJ2 has a large number of critical cells. When several of these cells present defects at the same time, the circuit integrity is affected.

Regarding Full Adders FA1 and FA2, the error-free simulations values found were in most cases very low, surpassing the percentage of 70% in just 18.75% of the simulations. This demonstrates that there is still plenty of room for proposals of more reliable adders. Comparing FA1 and FA2, only the tests that used "Assignable" probability model showed superiority of FA2 compared to FA1.

Fig. 10 shows that INV1, less robust than INV2, has in

fact a great proportion of high critical cells (identifiable by the amount of red cells). Based on the heat maps in Fig. 11 it is interesting to note that tests performed under the same probability model provide distinct results, because different defect classes have been used in both cases. Therefore, it can be concluded that the circuit robustness and cross-reference between defective cells and errors also depends on the defect class that the circuit is subjected to.

Finally, the heat maps in Fig. 12 indicate that circuits have critical regions. In those regions, defects will result in errors more easily. Generally, critical regions perform logic operations, as can be observed in FA1: Its critical region comprises mostly the cells that form the 5-input Majority Gate built-in within its structure.

Based on error simulation results, defect classes that cause errors in a circuit more frequently can be identified. Similarly, critical regions of a structure can be mapped, i.e. regions where the presence of defects often leads to error events. Such information may provide support to establish production requirements for different structures. Moreover, results allow identifying the weaknesses of the circuits aiming to propose specific changes in existing structures or design novel structures that are more reliable. In both situations, the use of the methodology described in this work provides support to enhance robustness techniques.

2) Clock Shifts Test

From the data presented in Table III, one may note that at least two factors strongly interfere in the robustness of a QCA structure under phase-shifted clock signals. The more evident condition is the range of shifts applied in the test. All the fundamental components tested manifest limited robustness when submitted to extreme clock signals deviations, in the range of $\pi/4$ to $\pi/2$ radians. On the other hand, the same four structures performed similarly well when the shifts applied were in the range of 0 to $\pi/4$ radians. Such result is attributed to the phase inversion that is likely to occur for great phase shifts, as already highlighted in [18]. Nonetheless, no further results for shifts beyond $\pi/4$ are reported in the literature.

The second observable fact is that the wire performed significantly superior than the remaining structures. Such observation may be attributed to its straightforward characteristic, that is, the regular wire does not use bends or curves. Any QCA structure which has a point of turning embedded within its structure tend to create weak polarization points, as demonstrated by the heat maps presented in the beginning of the current subsection. This weak points are strict related to the cell-to-cell interactions, which are guided by the timing rules established in the clocking scheme, as exposed in section II. The investigation of the relation between clocking and polarization strengthen is carried out in details in [18].

The related works regarding QCA errors caused by clock phases shifts [35] [18] [41] seems to point to the same direction; that is, modifications in clocking scheme instead of the structures may be a possible solution for the problem of errors caused by clock shifts in QCA.

VI. CONCLUSION

QCA is a promising technology candidate for CMOS succession. The development of more reliable structures is one important step, though, to enhance the probability that QCA might be applied for future applications. Although there are some researches in the field of defects and error simulation for QCA circuits, there are not many tools available for turn the design of these structures into a less tough task. This paper presents a QCA Defects Simulator implemented according to the precepts of a novel methodology for error analysis. that can be valuable for designers developing new robust QCA structures. The feasibility of the presented methodology could be proven by simulation results. Further, it could be identified initial points for robustness improvements of know QCA structures and clocking circuits.

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