12 dBm OCP_{1dB} Millimeter-wave 28 nm CMOS Power Amplifier using Integrated Transformers

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ABSTRACT

This paper describes the design of mm-wave integrated transformers and their application within a power amplifier (PA) in a 28 nm CMOS technology. The PA presents a 2-stage common-source differential topology and uses one transformer at the input and another at the output to perform single-ended to differential conversion, as well as another transformer to perform interstage matching. The baluns are sized to provide low insertion losses and high common-mode rejection rate (CMRR) as well as integrating the input and output matching networks. The designed baluns achieve minimum insertion losses better than 0.8 dB and CMRR superior to 27 dB. The output-stage transistors have a measured 1 dB output compression point (OCP_{1dB}) of 10.2 dBm, 10.1 dB gain and peak power added efficiency (PAE) as high as 35%. Thanks to the transformers, the PA presents a compact implementation, occupying only 0.037 mm² on silicon. The fabricated PA achieves 12 dBm OCP_{1dB}, 15.3 dB gain and peak PAE better than 20%.

Index Terms: 28 nm CMOS, millimeter-waves, power amplifier (PA), transformers, WiGig.

I. INTRODUCTION

The need of ever-increasing data rates for wireless networks has led recently to the emergence of millimeter-wave systems. For short-range indoor applications such as WLANs and WPANs, the 60 GHz band is of special interest. This frequency band is particularly suited to such applications since atmospheric absorption caused by oxygen is considerably high, favoring frequency reuse [1]. Moreover, several gigahertz around 60 GHz are available for unlicensed use in different parts of the world. In the European Union, for instance, this band extends from 57 GHz to 66 GHz, whereas in the United States the 66-71 GHz band is additionally included, totaling a 14-GHz range [2-3]. As a consequence, a number of standards targeting WLANs and WPANs have been issued in the past few years. One of the most noteworthy efforts concern the mm-wave amendment to the IEEE 802.11 standard, labeled 802.11ad, and commonly referred to as WiGig. Its specifications provide full network interoperability with Wi-Fi systems operating at 2.4 GHz and 5 GHz while allowing for data rates as high as 7 Gbit/s [4].

Such applications require a low-cost and low-power implementation for the RF transceivers. This favors the adoption of System-on-Chip solutions. Therefore, due to the large amount of digital circuitry integrated in such systems, advanced CMOS nodes become the most suitable technology choices. Nevertheless, the use of downscaled processes poses a number of challenges in the design of analog and RF blocks. Namely, for the design of power amplifiers (PAs), the low breakdown voltage makes it increasingly difficult to obtain high output power levels. Moreover, as the back-end-of-line (BEOL) of the technologies is scaled, their passive devices tend to become increasingly lossy.

Therefore, the careful design of passives is of utmost importance in order to obtain good performances in a fully integrated PA. The use of transformers in such circuits is advantageous in a number of aspects. They allow performing single-ended to differential conversion, impedance matching and power combining and splitting with a broadband and significantly more compact implementation than using transmission-line-based solutions or single inductors. The main drawback of their use is that transformers models are not usually supplied within the process design kits of

CMOS foundries. Therefore, in order to take advantage of their use, it is necessary that the IC designer carry out the design of the transformers.

A number of realizations of 60-GHz PAs in 65-nm CMOS have been reported [5-9]. As a means of attaining high output power levels, parallel amplifying topologies including power combining structures are widely used. The drawback has been that most of these implementations have displayed a considerably large area occupations and power-added efficiencies (PAE) inferior to 10%. The design presented in [9], for instance, employ 4 parallel cells and use a transformer-based power combiner. Whilst presenting an output saturation power as high as 15.6 dBm and 20 dB gain, the peak PAE is limited to 6.6% and the total area occupation amounts to 2.25 mm^2.

For sub-65 nm CMOS technologies, fewer 60-GHz power amplifiers have been published yet. For the 28-nm node, specifically the circuits in [10] and [11] have been reported to this point. Whilst the limitation on the supported voltage levels over the transistors become more stringent, the technological evolution has allowed significant improvement on the frequency performance of the devices, allowing higher gain levels at mm-waves. Thus, employing such devices as well as careful design and modeling of passive components has allowed the development of high output power amplifiers without resorting to cumbersome additional components and reducing DC power dissipation.

This paper presents the design of a transformer-coupled 28 nm CMOS PA targeting WiGig applications in the 60 GHz band. Section II presents a description of the 28 nm CMOS technology, the PA topology and the design and electromagnetic simulation results of the transformers, highlighting their minimum insertion losses (IL_m) and common mode rejection ratio ($CMRR$). Experimental results of the power transistor and the designed PA are presented, discussed and compared to the state-of-the-art in Section III.

II. PA DESIGN

The PA in this work was designed in a bulk 28 nm CMOS technology from STMicroelectronics solely using low-power, low-V_t transistors. The adopted topology for the power amplifier is shown in Fig. 1. It consists of a 2-stage pseudo-differential common source [12].

The substrate of the adopted technology presents a moderate resistivity which impacts in significant losses for the passive devices. The BEOL comprises a total of 10 copper metallization layers in addition to an aluminum cap at the top of the stack. Fig. 2 highlights the uppermost and thickest layers of the BEOL. These layers are used for transformer design in order to minimize parasitic capacitances to the substrate and resistive metallic losses. In this process, the top copper layers are referred to as IA and IB, and the aluminum level is called LB.

In order to enhance the reverse isolation of the PA and ensure its stability, cross-coupled capacitive neutralization allowing an adequate compensation for the feedback effect of the transistors' gate-drain capac-

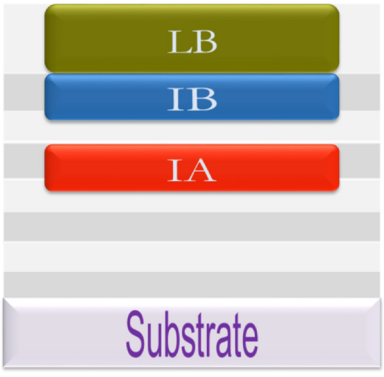

Figure 2. Cross-section of the top layers of the 28 nm BEOL (*dimensions not to scale*).

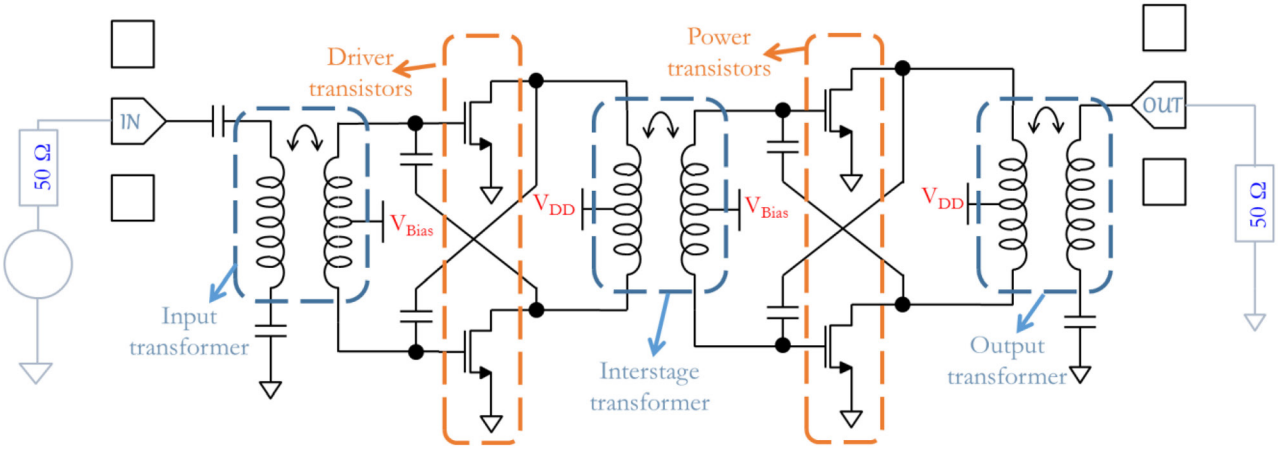

Figure 1. Schematic of the 60 GHz 28 nm CMOS PA.

itances was adopted [13]. All of the used capacitors present a MOM constitution. The design and modeling of the transformers, RF pads and in interconnections, witch special attention to the cross-connections of neutralization capacitors, were carried out using electromagnetic (EM) simulations.

A. Transformer design

Transformers play an essential role within this circuit. They are used at the input, output and between stages, performing multiple tasks. First, the input transformer provides power splitting by converting the single-ended input signal into differential mode. Conversely, the output transformer is responsible for power combining as they convert the differential output RF signal into single-ended form. Furthermore, they provide ESD protection at both the input and output. Another relevant function of the three transformers is to provide biasing of the transistors. Both the supply V_{DD} and V_{Bias} are introduced through the center taps of primaries and secondaries for both stages of the amplifier. Finally, along with MOM capacitors as well as the RF pads, the transformers are responsible for the input, output and interstage impedance matching.

The proposed transformers present a stacked octagonal topology illustrated in Fig. 3. Both primaries and secondaries present a single-turn layout, but impedance transformation is achieved through concurrent dimensioning of their average diameters (D) and trace widths (W_P and W_S) as described in [14]. No ground shield is inserted between the conductors and the substrate in order to ensure sufficiently high resonant frequencies and reduce insertion losses [15]. Due to the topology of the PA, the transformers were designed to operate under two different conditions: whereas the input and output transformers are required to present one single-ended port and one differential port, the interstage transformers must operate with two differential ports. The topology of the transformers that operate as baluns is illustrated in Fig. 4, where the center tap of the differential port must be connected to an RF ground.

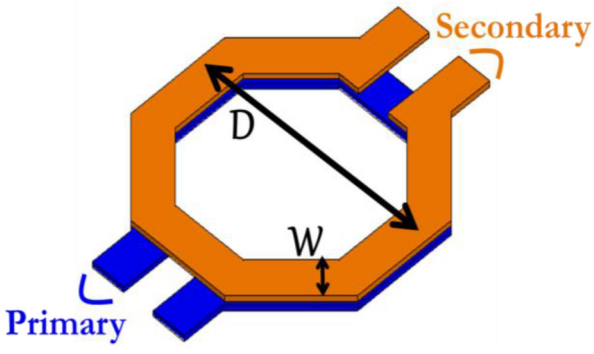

Figure 3. Transformer topology

Ideal balun operation would ensure an equal power magnitude at both differential terminals with a 180° phase difference. One useful metric to compute both amplitude and phase imbalances for a balun is the common-mode rejection ratio [16]. Another essential metric for transformers, whether they operate as baluns or not, is the minimum insertion loss. It corresponds to the power loss introduced in the circuit when both ports of the transformers are matched.

Transformer sizing proceeded as follows. A number of components were simulated using the ANSYS HFSS electromagnetic field solver. In all cases, the primary had a fixed trace width W_P = 12 μm. Furthermore, the primary and secondary average diameters were identical, i.e., the secondary was perfectly centered above the primary. Then, the diameter of the windings was varied from 50 μm to 70 μm, and the secondary trace width was varied from 4 μm to 12 μm, which corresponds to the minimum and maximum widths allowed in the adopted process. The computed *CMRR* and IL_m at 60 GHz are summarized in Fig. 5.

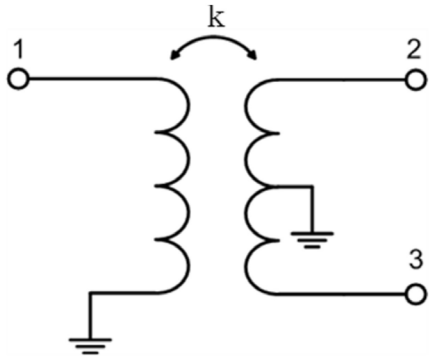

Figure 4. Transformer in a balun configuration.

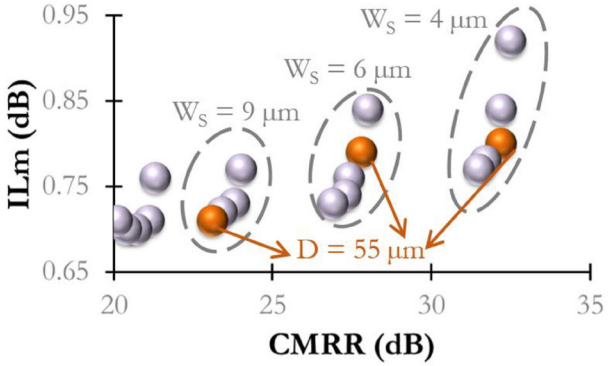

Figure 5. Simulated *CMRR* and *ILm* for transformers presenting average diameters from 55 µm to 70 µm and secondary trace widths from 4 µm to 12 µm. Each point corresponds to a different transformer.

For the input transformer, the dimensions were chosen so that the *CMRR* would be maximized. As shown in Fig. 5, the best attained *CMRR* was 32 dB, for transformers with a 4 μm secondary width. Among those transformers, the one with the lowest IL_m (0.8 dB) was selected. Therefore, the dimensions of the input transformer is D = 55 μm. Fig. 6 presents the final layout of this transformer including the bias feed connected to the primary center tap. Additionally, its simulated parameters are shown in Fig. 7 and 8. The results in Fig. 7 show that amplitude imbalance between the differential terminals is inferior to 0.5 dB up to 100 GHz and is as low as 0.2 dB at 60 GHz, whereas a 2.5° phase imbalance is observed at 60 GHz and it does not exceed 5° in the considered frequency band. In Fig. 8, it is shown that the low-frequency value of the primary inductance (L_P) is 100 pH and the secondary's (L_S) is 125pH, and the equivalent coupling coefficient (k) is 0.75 at 60 GHz.

The design of the output transformer presented one additional challenge. Due to high current values at the output of the PA, a 4 μm metal width could not be used. Therefore, the minimum trace width with sufficient current capability was found to be 6 μm, when the secondary was implemented as a stack of IB and LB. Hence, the criterion for dimensioning was the same as for the input transformer, once discarded the narrowest secondaries. Following this procedure, the transformer with a 6 μm secondary width and a 55 μm average diameter was selected, presenting a 0.79 dB IL_m and a 27.8 dB *CMRR*. The layout of the output transformer is presented in Fig. 9, and simulation results are shown in Fig. 10 and Fig. 11. As predicted by the simulated *CMRR*, the amplitude and phase balances are degraded in comparison to the input balun, but, at 60 GHz, the amplitude imbalance remains inferior to 0.35 dB and the phase imbalance is 4°. The primary low-frequency inductance remains the same and, due to the increased width and thickness of the secondary, its low-frequency inductance is reduced to 115 pH and the coupling coefficient at 60 GHz is improved to 0.81.

Finally, as the interstage transformer is not intended for mode conversion, its simulated *CMRR* was disregarded. Alternatively, one of the transformers with the lowest IL_m (0.71 dB) was chosen. In this case as well, the diameter of the windings was 55 μm, and the secondary width was 9 μm, as illustrated in Figure 12. As presented in Figure 13, the low-frequency secondary inductance is 105 pH and the coupling coefficient at 60 GHz is 0.86.

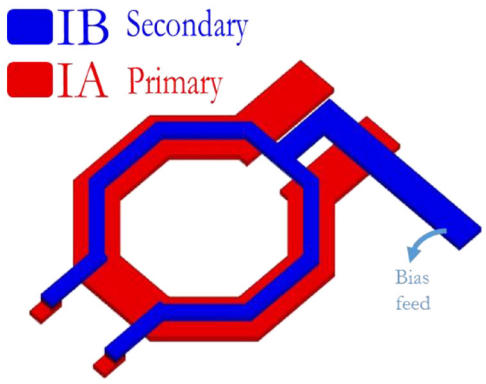

Figure 6. Layout of the input transformer.

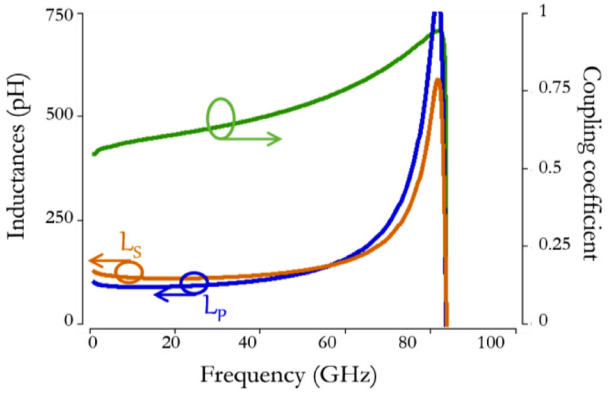

Figure 8. Simulated inductances and coupling coefficient of the input transformer.

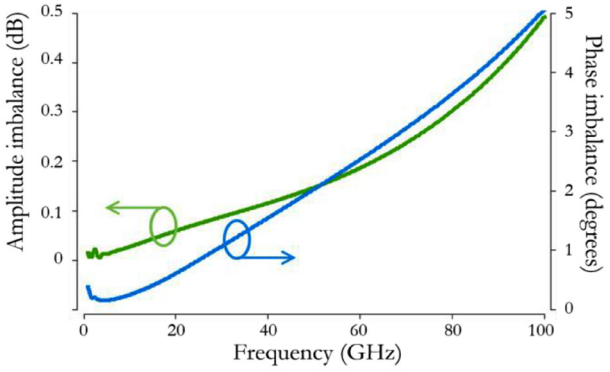

Figure 7. Simulated amplitude and phase imbalances of the input balun.

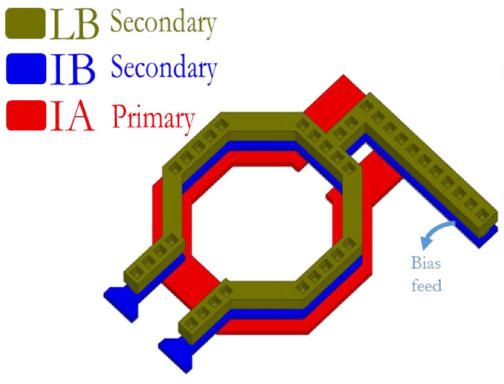

Figure 9. Layout of the output transformer.

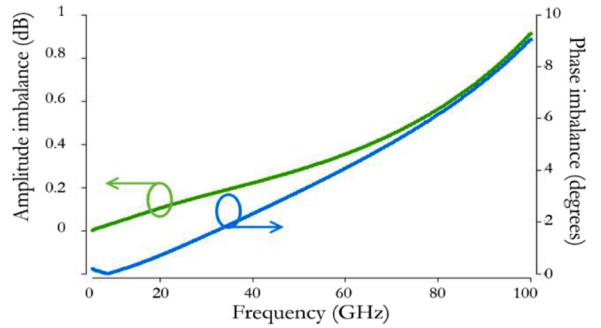

Figure 10. Simulated amplitude and phase imbalances of the output balun.

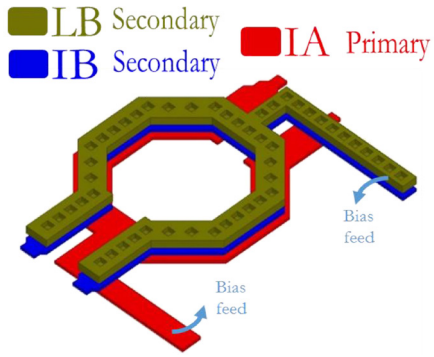

Figure 12. Layout of the interstage transformer.

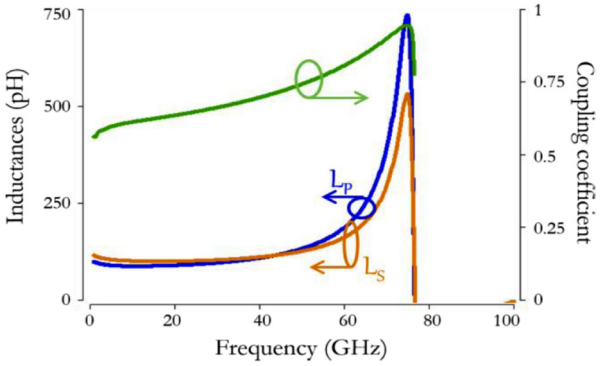

Figure 11. Simulated inductances and coupling coefficient of the output transformer.

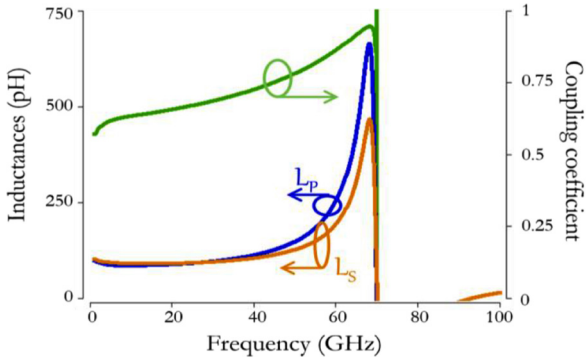

Figure 13. Simulated inductances and coupling coefficient of the interstage transformer.

B. Active devices

Transistors were sized taking into account their power capability and gain as well as the layout parasitics, whose influence increase for wider transistors. Following this trade-off, a 1 μm finger width was adopted for all transistors. The power transistors were then sized to a total 90 μm width, whereas driver transistors presented half this width. Since the transistor cells supplied by the foundry includes only connections to the lowest metal level, the layout of the connections up to the highest metal (IB) was drawn using a stair-shaped layout as depicted in Fig. 14a for the power transistor and Fig. 14b for the driver transistor.

The parasitic elements introduced by these transistors' accesses were extracted by EM simulation on Keysight ADS and combined with the intrinsic transistor model supplied by the foundry to constitute the extrinsic model presented in the circuit of Fig. 14c. The parasitics inherent to the structure were therefore represented by a gate-drain, a gate-source, and a drain-source capacitances, along with gate, drain and source series resistances, and drain and source series inductances.

Fig. 15 and Fig. 16 compare the simulated results for the maximum gain for both transistors for the intrinsic and extrinsic models. It can be observed that the introduced parasitics account for, approximately, 1 dB loss in the power gain.

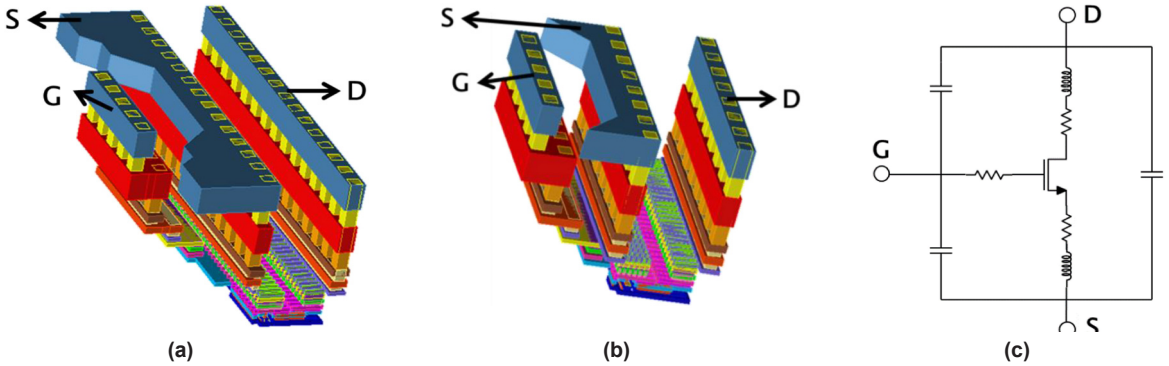

Figure 14. (a) Layout of the power transistor, (b) Layout of the driver transistor, (c) Extracted transistor model including parasitic elements.

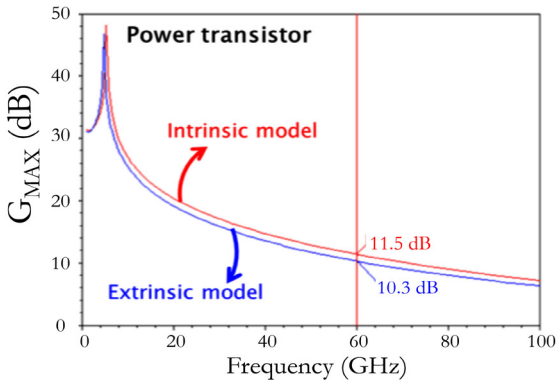

Figure 15. Simulated maximum gain for the intrinsic and extrinsic power transistor model.

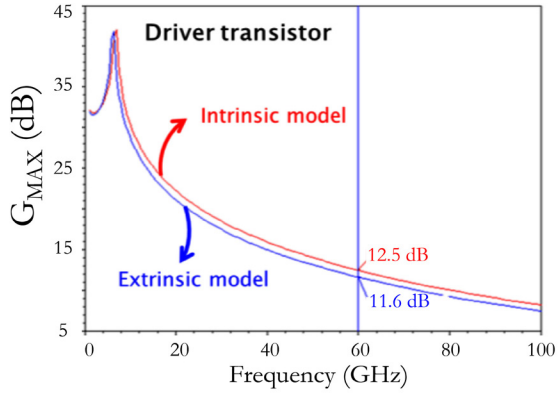

Figure 16. Simulated maximum gain for the intrinsic and extrinsic driver transistor model.

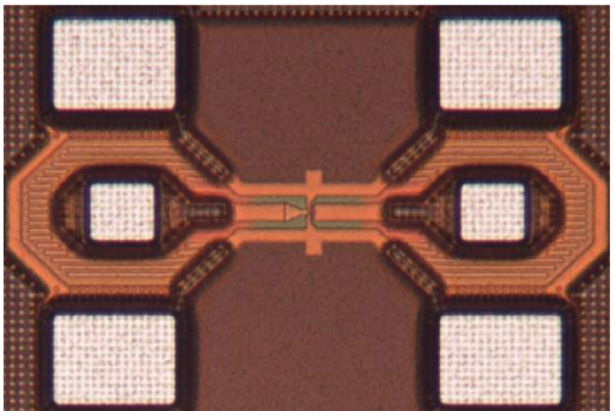

Figure 17. Micrograph of the fabricated power transistor.

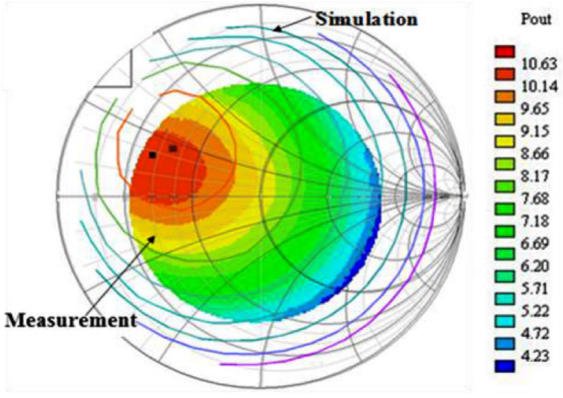

Figure 18. Load-pull output power measurements and simulation at 60 GHz.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Power transistor

The micrograph of the fabricated power transistor is presented in Fig. 17. Large-signal measurements were carried out on-wafer at room temperature and an open-short de-embedding technique was used in order to compensate the effect of the RF pads and feed lines.

Using a Focus load–pull system, the output power contours at 60 GHz presented in Fig. 18 were measured for biasing at V_{GS} = 0.75 V and V_{DS} = 1.1 V, and the optimal load impedance was found to be Z_{Load} = 14+j·10 Ω. Applying this load impedance, the large signal characterization presented in Fig. 19 was carried out. A 10.1 dB small-signal gain was found, which is very close to the maximum simulated value presented in Fig. 15. A peak *PAE* as high as 35% was observed as well with a 1 dB output compression point (OCP_{1dB}) of 10.2 dBm, and a 12.6 dBm maximum output power. Since at this maximum measured power level, the output is still not saturated, it can be concluded that this transistor is capable of providing an even higher output power.

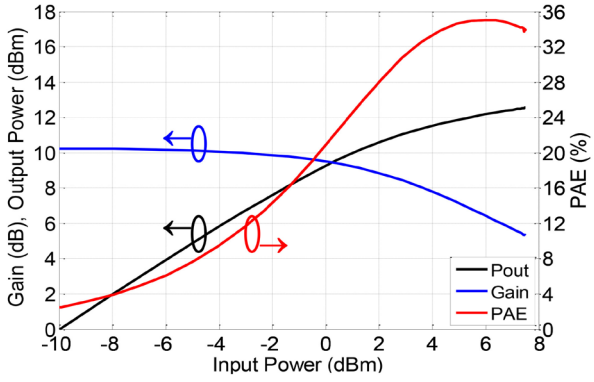

Figure 19. Measured gain, output power and PAE of the power transistor at 60 GHz.

B. Power amplifier

The proposed PA integrating the three designed transformers was fabricated and its micrograph is shown in Fig. 20. Due to the extensive use of transformers, the circuit presents a very compact implementation with a 0.037 mm² area for the core of the circuit and 0.255 mm² as the total surface including pads.

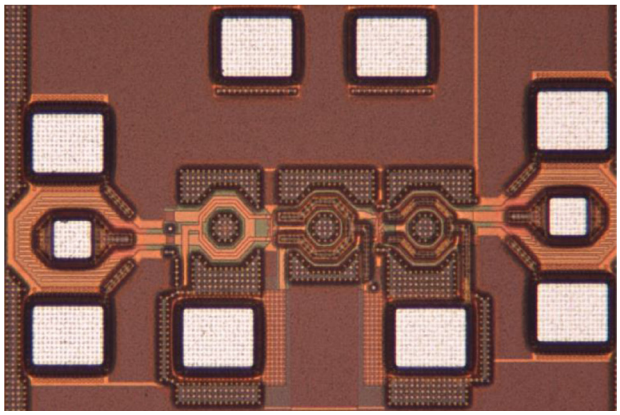

Figure 20. Micrograph of the fabricated power amplifier.

Biasing of the circuit was performed with V_{DD} = 1.1 V and V_{Bias} = 0.75 V.

Small-signal characterization was carried out on-wafer at room temperature with an Agilent E83612 vector network analyzer and are presented in Fig. 21. The small-signal power gain is 13 dB at 60 GHz and is superior to 15 dB between 64 GHz and 69 GHz. Thanks to the capacitive neutralization, isolation is better than 40 dB up to 80 GHz and the amplifier is unconditionally stable in the whole considered frequency range, as evidenced by the μ-factor superior to unity in Fig. 22.

The large signal performances of the circuit were obtained using the same setup as for the single power transistors and are depicted in Fig. 23 and Fig. 24. It can be observed that at 60 GHz the saturation power (P_{Sat}) reaches 15.1 dBm, the output referred 1 dB compression point is 11.7 dBm and the peak *PAE* value is as high as 19.6%. At 64 GHz, the OCP_{1dB} is improved to 12 dBm, the peak *PAE* reaches 20.2% and P_{Sat} is slightly decreased to 14.8 dBm. Moreover, it can be observed that the output saturation power as well as the OCP_{1dB} are relatively flat in the band between 60 GHz and 70 GHz.

An overall good matching is observed between measured and simulated results. The most pronounced divergence appears for higher power levels (P_{in} > 10 dBm). A frequency shift compared to targeted band is observed as well, as we can see gain and input matching peaking beyond 64 GHz. It is important to note that working with such a recent technologic process poses a number of challenges in the designers' point of view. First, device modeling was not fully validated at the time of design. This means that, especially for high power levels, the disparity between simulated and measured data was observable. Moreover, the models available at the time of design did not include data for statistical analysis. Thus, as the chip was fabricated in a less favorable slow-slow corner, actual gain and *PAE* results were degraded. Finally, as the 28-nm CMOS design kit

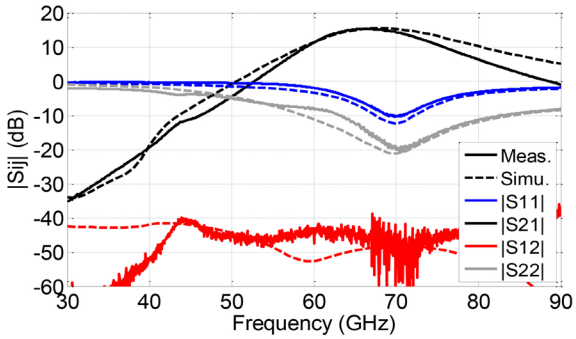

Figure 21. Measured and simulated S-parameters of the PA.

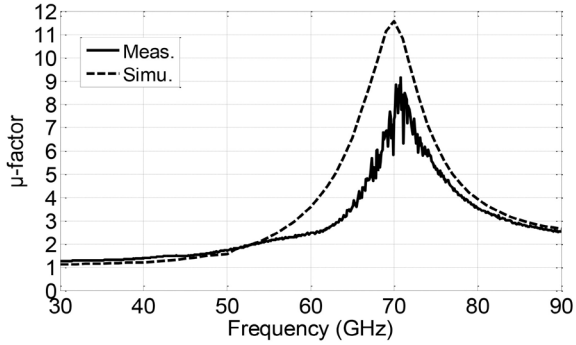

Figure 22. Measured and simulated μ-factor of the PA.

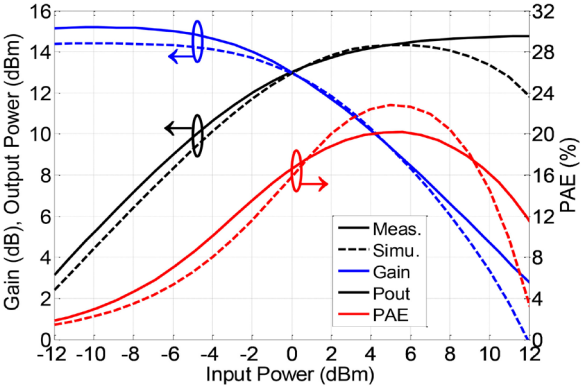

Figure 23. Measured and simulated gain, output power and PAE at 64 GHz.

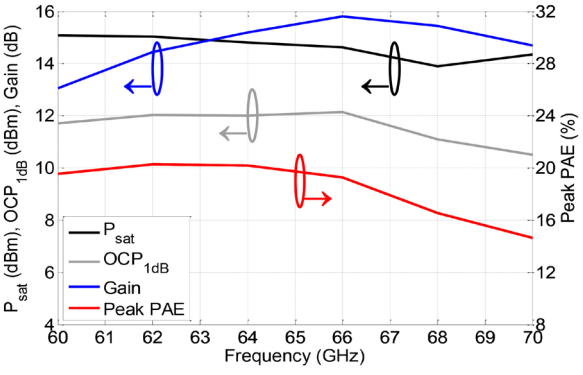

Figure 24. Measured saturation power, OCP1dB, gain and peak PAE.

was based on a 32-nm DK, data preparation before fabrication included the shrinkage of certain layout components. This was not an issue for components provided within the DK, but the transformers, which were specifically drawn by the designers, presented dimensions reduced by a 10% factor after fabrication. This was a significant source for the frequency deviation.\

C. Comparison with the State-of-the-Art

The experimental results of this PA are compared in Table 1 to previous 60 GHz realization in the state-of-the-art using sub-65 nm CMOS processes. The power performance in [17] is superior as it employs twice as many amplifying cells as in our work, therefore occupying twice as much silicon area as well. This circuit employs a parallel topology including transformer-based power splitter and combiner. This technique is exploited even further in [18], which makes use of 32 cells in parallel and occupies an area superior to 2 mm². Its saturation output power, on the other hand, is the highest reported in this comparison. One of the PAs which achieve the highest *PAEs* is the one in [19]. This is mostly due to the use of a class-E topology as well as the fact that it employs a SOI process, minimizing the loss of passive components. The output power and gain, on the other hand, are considerably lower than the ones achieved in this work. 60 GHz PAs in 45-nm CMOS are presented in [20-24]. While [20], [21] and [23] achieve higher gains, but inferior output powers and PAE; [24] provides higher output powers but the gain is limited to 6 dB and the *PAE* remains inferior to 10%.

Table 1. Comparison of 60 GHz sub-65 nm CMOS PAs

Ref.	Technology (nm)	Gain (dB)	P_{sat} (dBm)	OCP_{1dB} (dBm)	Peak PAE (%)	Area (mm²)
This work	**28**	**15.3**	**14.8**	**12**	**20.2**	**0.037**
[10]	28	24.4	16.5	11.7	12.6	0.122
[11]	28 (SOI)	35	18.9	15	17.7	0.162
[11]	28 (SOI)	15.4	18.8	18.2	21	0.162
[19]	32 (SOI)	10	12.5	-	30	0.605
[17]	40	17	17	13.8	30.3	0.074
[17]	40	21.2	17.4	14	28.5	0.074
[25]	40	22	10.5	10.2	10.8	0.033
[18]	40	29	22.6	17	7	2.16
[20]	45	19	7.9	-	19.4	0.034
[21]	45	20	14.5	11.2	14.4	0.039
[22]	45	6	13.8	11	7	0.056
[23]	45	17	13.5	8.7	13.4	0.018
[24]	45	6	16.3	13.2	8.7	0.057

One realization in 28 nm CMOS is the dual-mode PA presented in [11]. It achieves the highest reported gain when operating in high gain mode and the highest OCP_{1dB} in the high linearity mode. These performances are made possible by the use of a SOI process as well as a 0.162 mm² area occupation. To the authors' knowledge, the sole other 60 GHz realization using 28 nm bulk CMOS is the PA in [10]. Their work present a 24.4 dB gain due to the use of an additional gain stage. Our PA, on the other hand, achieves a considerably higher *PAE* and a slightly superior OCP_{1dB} while occupying a significantly reduced area.

IV. CONCLUSION

The design of a 28 nm CMOS mm-wave PA including integrated transformers was presented in this paper. The transformers present a stacked single-turn topology and perform single-ended to differential conversion and impedance matching. The input transformer-based balun achieves a 32 dB *CMRR* and a 0.8 dB minimum insertion loss, whereas the output balun has a 27.8 dB *CMRR* and a 0.79 dB IL_m, and the interstage transformer presents a 0.71 dB IL_m. The PA presents a 2-stage pseudo-differential common source topology and uses the three designed transformers.

The design of transistors was detailed highlighting the modeling of parasitics in the transistors accesses. Measurement results of the designed power transistor show a 1 dB output compression point of 10.2 dBm and a saturation power superior to 12.6 dBm. The measured small-signal gain was 10.1 dB and a peak *PAE* of 35% was reported.

Thanks to the use of the transformers, the fabricated PA occupies a silicon area of solely 0.037 mm². Experimental results show that the fabricated PA is unconditionally stable a 14.8 dBm P_{Sat}, a 12 dBm OCP_{1dB}, a 15.3 dB gain and a 20.2% peak *PAE*. To the authors' knowledge, this is the highest reported *PAE* and OCP_{1dB} in a 28 nm bulk CMOS PA.

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