A 1 to 10-bit, 85.3 fJ/Conv-step ADC for RFID Sensors

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ABSTRACT

This paper presents the design results of an ultra-low power 1 to 10 bit arbitrary resolution switched capacitor analog to digital converter. In addition to using low-power elements, his project also used a library specifically optimized for the proposed converter rather than a standard library as in traditional approach. This approach enabled the overall converter consumption to be reduced by about 70 %. Consuming 7.29 µA at 1 V supply and taking less than 9 µs per conversion (10 bit mode) it can be used in LF, HF or UHF RFID passive sensor tags. The presented converter was designed in 180 nm CMOS technology occupying about 0.052 mm^2 of silicon area. A simulation result shows a figure of merit equal to 85.3 fJ/Conversion-step and 9.5 effective number of bits.

Index Terms: Ultra-low Power, ADC, Switched Capacitor, RFID Sensor.

I. INTRODUCTION

The recent rise of market demand for wireless sensors has caught attention to RFID sensors as an attractive solution. The RFID technology offers a robust communication in different frequency bands, unique identification, collision management, well stablished standards and a great number of readers, some of them being present even in popular smartphones (NFC readers).

A RFID sensor tag is basically constructed by modifying a standard RFID tag. There are several ways to do that transformation. They can be grouped in three categories. The first one exploits the sensitivity of the tag antenna to the physical change that appears in its near field region. The second category is more related to the behavior of the RFID chip and the variation of its electrical response as function of some external parameters such RF power, temperature etc. The third category consists in the integration of an external sensor to the RFID chip circuitry [1].

Except for some simplistic sensors like seal break detectors [2], threshold passing detectors [3] or specific architectures as the one designed in [4], the integration of an external sensor to the RFID chip circuit usually needs an analog to digital converter. Since the energy available for entire tag supply is very limited, especially for passive RFID tags, this integration can be quite challenging.

Passive RFID tags harvest their energy from the communication field generated by reader´s antenna, which means that it decays when communication distance increases. Low frequency RFID tags (125 kHz to 134 kHz) and high frequency tags (13.56 MHz) operate at near field by magnetic coupling. For those tags, the energy delivered by the reader´s antenna depends on the magnitude of the generated magnetic field [5]. For UHF tags the power transfer occurs no more by magnetic coupling, as in LF and HF cases, but by electromagnetic radiated field.

For typical card size HF RFID tags the energy harvested is not greater than some tens of mW at distance of few centimeters from the reader and not greater than some tens of μW at few meters of distance from the reader´s antenna for UHF tags. In despite of the available energy for LF and HF systems be much greater than UHF systems, is important to note that it decays faster since its magnitude is inversely proportional to the cube of communication distance while in UHF systems the power magnitude is inversely proportional to the square of communication distance. Moreover, most of RFID tags are designed to operate without a critical alignment between its antenna and reader´s antenna which impose a several limitation on quality factor for LF and HF systems and on tag´s antenna gain for UHF systems. That limitation also implicates on a reduction of maximum received power on tag´s front-end constraining once more the available energy to the tag´s circuitry.

The proposed ADC is targeted to compose a passive RFID sensor tag for HF band designed to operate with a very small planar antenna being able to harvest about 250 μW from the reader´s communication field.

The designed ADC allows conversions with intermediary resolutions, giving the possibility to save power in less accurate applications or situations. For instance, a sensor used to detect a hazardous gas can have 2 operation modes. The first one, with 2 resolution bits, can only detect the presence or absence of that gas. Since it consumes only a fraction of the energy need for full resolution operation, the tag can operate at longer distances. If the gas is detected the second operation mode can be set (by using a different interrogation word), returning a full resolution measure, this time at shorter reading distance.

In the following chapters a brief survey analysis on the most suitable ADCs for RFID sensor tags is presented and the design of an ultra-low power 10-bit SAR ADC is proposed in accordance with this same analysis. Finally, simulated results are presented and discussed.

II. ADCS FOR RFID SENSING APPLICATIONS

A good indication of the most appropriated ADCs for RFID sensing applications can be found looking for the most energy-efficient implementations reported on VLSI and ISSC conferences. Taking the power consumption as the main guideline, the figure of merit (FoM) of more than 400 ADCs reported on VLSI and ISSC [6] over the last ten years were classified according technology node as can be seen in Figure 1. The result is a clear advantage of SAR type for all nodes below 350 nm [7].

It is important to note that a good analog-to-digital converter for passive RFID sensing applications should have not only a low FoM but also very low power consumption. Some solutions as the asynchronous converter proposed in [8] or the pipeline converter proposed in [9] achieves a very low FoM but under high sampling rates and higher overall power consumption than other similar solutions with lower sampling rates. Moreover, there are other aspects to be considered before to choose a specific design for a given application. The target technology node, silicon area, operating temperature and calibration procedures are only some of most common aspects. All the things considered, the choice can fall on an ADC which the power consumption is not exactly the lowest one. Naturally, all the energy saved on analog to digital conversion will allow a greater communication distance between the RFID sensor tag and reader or can used to other devices like signal conditioning circuit or sensors.

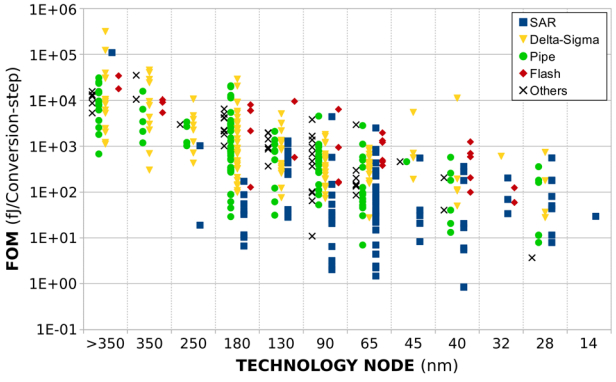

Figure 1. Figure of merit (FOM) of the reported ADCs on ISSCC versus technology node. Only designs on CMOS processes were considered.

Summarizing, in order to be appropriate for passive HF RFID sensing at a reasonable distance from reader (about 10 cm), the ADC together with the signal conditioning circuit and the sensor itself should have a maximum power consumption of few tens of μW. Concerning the timing constraints, a minimum sample rate of 3.5 kSample/s should be satisfied.

In fact, the charge redistribution SAR ADC is a very suitable solution for passive RFID sensing. In [10], an ultra-low power 8-bit SAR ADC has been designed and used to implement a passive temperature sensor UHF RFID tag able to establish a stable communication up to 6.5m from the reader.

III. PROPOSED ADC

Aiming a maximum communication distance between the sensing tag and reader equal to 10 m, where the available power for a 2 dBi tag antenna working with a 36 dBm EIRP reader is about 50 μW [11], the power consumption of proposed ADC was been constrained to 10 μW, leaving about 40 μW to feed the tag circuitry and the sensor.

According to the analysis made on the previous section, the charge redistribution successive approximation register ADC seems to be the best choice for passive RFID sensing. Among different approaches to implement SAR ADCs, the one based on charge redistribution achieves the best FoM. This way, a 10-bit capacitive SAR ADC was chosen for this application. This ADC, first proposed by [12], is basically composed by a capacitive array that gathers both DAC and sample and hold roles, a comparator and a successive approximation register (SAR) in charge of control the capacitive array switches and generate the output word. Its general diagram block is sketched on Figure 2.

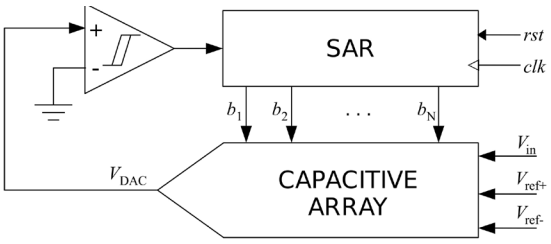

Figure 2. Block diagram of designed ADC.

The working principle of this ADC is based on the charge sharing between binary weighted capacitors, using only CMOS controlled switches as depicted in Figure 3. Its conversion sequence can be resumed in 4 steps as follows:

i. Φ_1: switch S_1 is turned to V_{IN} and switches b_0 to b_9 are turned to S_1 node connecting all lower capacitance plates to V_{IN} potential. At the same time, switches S_{2a} and S_{2b} are closed discharging any residual voltage on the nodes V_X and V_{OUT} thus setting V_{OUT} to zero (Figure 3.a).

ii. Φ_2: switches S_{2a} and S_{2b} are opened and switch S_1 is turned to V_{REF-} setting the voltage on the upper capacitance plates to V_{REF-} - V_{IN} (Figure 3.b).

iii. Φ_3: switch S_9 is turned to V_{REF+} setting and V_x node to $(V_{REF+} - V_{REF-})/2 - V_{IN}$. Since the C_S capacitor was discharged during Φ_1 phase, this same potential will appear on V_{OUT}. At this point, the voltage signal on V_{OUT} node will indicate the value of b_9 output. A negative voltage means that the sampled voltage (V_{IN}) is less than half the reference voltage, resulting as $b_9 = 0$ or $b_9 = 1$ otherwise. If the resulting bit was zero, the SAR controller should turn the S_9 switch back to V_{REF-} at beginning of the next step (Figure 3.c).

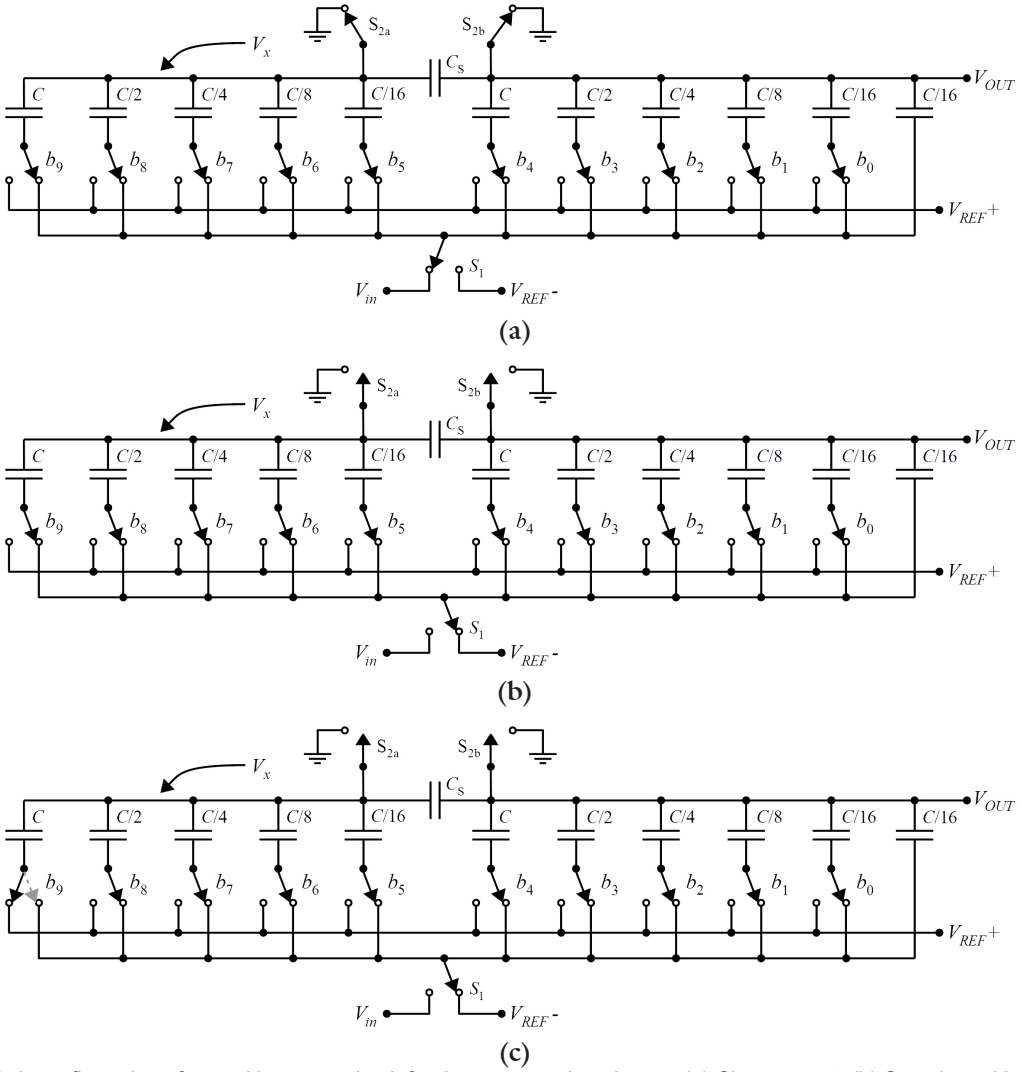

Figure 3. Switch configuration of capacitive array circuit for three conversion phases. (a) Charge reset; (b) Sample and hold; (c) Charge redistribution.

iv. Φ_4 to Φ_{13}: the testing sequence described in previous step should be repeated for switches S_8 down to S_0. At the end of last phase, all output bits (b_0,…,b_9) will be known, completing the analog-to-digital conversion.

The capacitance associated to b_0 (C/16 in this case) is commonly called *unity capacitance* (C_U). The C_S capacitor connecting V_X and V_{OUT} nets is a scaling charge element used to split the full capacitor array in two smaller arrays, avoiding the use of too big capacitors (in a straight implementation of N bits, the biggest capacitance will be 2^{N-1} times the unity capacitance). Its value can be calculated as:

$$C_S = \frac{2^{N/2}}{2^{N/2}-1} C_U \quad (1)$$

A time diagram of the main signals related to the above described ADC for a middle scale analog voltage input is presented on Figure 4. The *dac_out*, *adc_output* and *cmp_out* signals corresponds to the DAC output voltage (V_{OUT} in Figure 3), the control word of switches b_0,...,b_9 in Figure 3 and the output of the comparator connected to *dac_out*, respectively. In the same way, *smp*, *end_conv*, *rst* and *clk* are generic signals for S_1 switch control, $S_{2a,b}$ switches control, end of conversion output, main reset input and clock input, respectively.

It is important to note that both V_X and V_{OUT} nets on DAC circuit assumes negative voltage values during the conversion process (refer to *DAC Out* signal in Figure 4). That voltage inversion requires a special care on the design of S_{2a} and S_{2b} switches, usually some kind of bootstrap architecture [13].

IV. SAR

The successive approximation register in charge of all control signals was implemented by a finite state machine (FSM) customized to save power. Rather than performing this improvement by traditional method, that is, by using the vendor standard cell library, which is for general purpose, this design adopts a full top-down approach which can be resumed in three main steps:

1. The FSM is designed in terms of basic logic components (logical gates, latches and flip-flops);
2. A custom library is created with the required components to implement the FSM designed in the step 1. All components are modeled at transistor level with sizes and ratios optimized to work at maximum desired operating conditions (input switching at 1.4 MHz and supply voltage equal to 1 V, in this case). A compact and simplistic design was

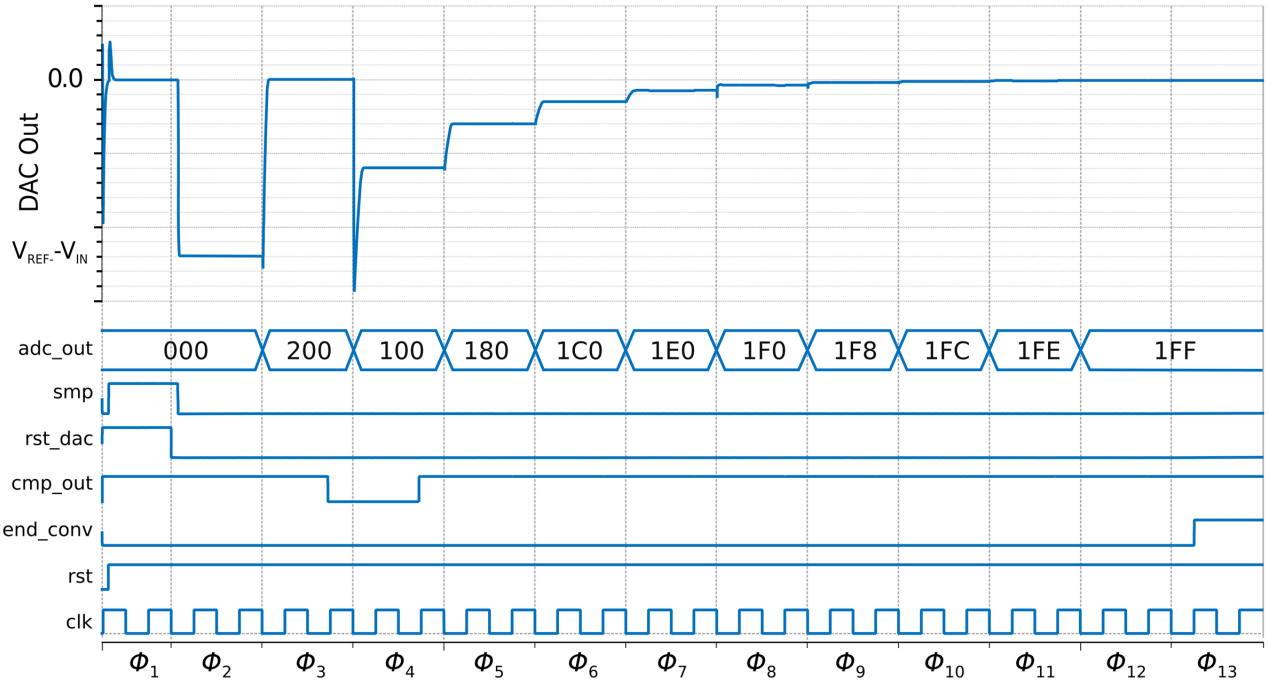

Figure 4. Time diagram of the main charge redistribution ADC signals.

been chosen to implement latches and flip-flops [14] in order to reduce the number of switching elements;

3. A last optimization is made by identifying and eliminating the redundant structures in the FSM at transistor level. For instance, clock signal inverters present inside of flip-flops sharing the same clock signal can be eliminated and replaced by a single inverter for all these flip-flops.

In order to allow conversions with reduced resolution bits, the entire DAC controlling word is directly shared with the ADC output, instead of copied to an output register at rise of *end of conversion* signal. This way, if the ADC is synchronously interfaced, the analog to digital conversion can be finished with the desired resolution bits (N) by simply stopping the input clock signal at proper conversion phase, Φ_M, according to the equation $M = N + 3$. Otherwise, if the ADC is asynchronously interfaced, the *end_conv* output signalizes the completion of full resolution conversion and puts the ADC on sleeping mode until the next reset command.

Finally, two different implementations were been made for the entire SAR circuit designed. One according to the purposed method, that is, using the fully customized library, and another using the standard cell library as in traditional method. Both implementations were simulated for supply voltages from 0.6 V to 1.8 V with a fixed clock frequency of 1.4 MHz. The results are depicted in Figure 5. As one can see the circuit designed by the purposed method consumes only one tenth of its equivalent designed by traditional method (1.98 μW @ 1.0 V and 21.72 μW @ 1.0 V, respectively).

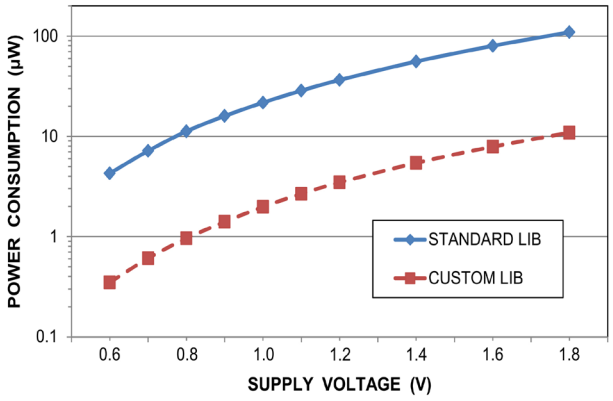

Figure 5. Simulated power consumption of SAR circuit for two different implementations: using the standard library (solid trace) and using the customised library (dashed trace).

V. CAPACITIVE ARRAY

As any switched capacitor circuit, the capacitive array is subject to thermal noise which power is expressed by

$$\sigma_T^2 = \frac{k_B T}{C_T} \tag{2}$$

where k_B is the Boltzmann constant, T is the absolute temperature and C_T the total capacitance. For this circuit, all capacitances are subject to charging and discharging during the same conversion, therefore, the thermal noise power expressed in Equation (2) should be doubled. On the other hand, the quantization noise power of an N-bit analog to digital converter is expressed by

$$\sigma_Q^2 = \frac{{V_{IR}}^2}{12 \cdot 2^{2N}} \tag{3}$$

where V_{IR} is the voltage input range of ADC, being equal to $V_{REF+} - V_{REF-}$. The proper sizing of unit capacitance (C_U) should be done to obtain a thermal noise power always smaller than the quantization noise power. Since the total capacitance of the described capacitive DAC can be calculated as

$$C_T = C_U(2^{N/2} + 1)\,, \tag{4}$$

the unit capacitance that generates a thermal noise power smaller than the quantization noise power is

$$C_U \geq \frac{24 \cdot k_B T 2^{2N}}{{V_{IR}}^2 (2^{N/2}+1)} \tag{5}$$

Moreover, two additional non idealities should be considered: the capacitance mismatch related to the parasitic capacitances along of all capacitor connections and the mismatch caused by process inaccuracies. Capacitance mismatches caused by process inaccuracies can be minimized by implementing each capacitor as a set of unit capacitors. For instance, the layout of the capacitor associated with b_4 will be made as 16 unit capacitors connected in parallel instead of a single capacitor with the same area. This way, mismatch errors caused by mask misplacement will equally affect all unit capacitors, changing its individual values but keeping the ratio between the capacitances in each array branch. Furthermore, the capacitance mismatch caused by other process variations can be minimized by distributing these unit capacitors in a common-centroid manner [15]. The mismatch related to parasitic

capacitances of interconnections can be virtually eliminated by a careful layout which ensures the same parasitic capacitance for each unit capacitor. Unfortunately, the relationship between the unit capacitance and scaling capacitance (C_S) is not an integer factor. In fact, according to Eq. 1, for a 10-bit ADC $C_U/C_S = 31/32$, which makes difficult cancel mismatch errors caused by mask misplacement since their dimensions will be slightly different. The small difference between C_S and C_U also difficult the adoption of small values for C_U because a small difference is difficult to obtain without a large error during the layout of small capacitors since their sizing can only be changed by fixed steps. In the same way, the capacitance mismatch is inversely proportional to capacitor perimeter [15]. In other words, a good matching between real and theoretical C_U/C_S requires increasing the value of unit capacitance. .

For the designed ADC $N = 10$ bit, $T = 300$ K and $V_{IR} = 500$ mV, so the smaller unit capacitance which can satisfy the noise criteria expressed by Eq. 5 is nearly 13 fF. Finally, the smallest value for unit capacitance which allows a corresponding scaling capacitance near to the theoretical value is 120 fF. This capacitance satisfies the noise criteria ($C_U \geq 13$ fF) and meets the C_U/C_S ratio with less than 0.4 % of error, almost the same capacitance mismatch estimated for both capacitors witch is equal to 0.3 %, according to the fab process data. The layout of all DAC capacitors and were made according to common centroid techniques. Each capacitor is controlled by a complementary CMOS switch with binary weighted size. The size of b_0 switch transistors are approximately (1/0.18) μm and (5.0/0.18) μm for pMOS and nMOS respectively. For this design the nMOS *W/L* ratio was increased over pMOS *W/L* ratio in order to allow a V_{REF-} voltage as low as 100 mV.

VI. COMPARATOR

With the view to improve the converter accuracy without increase the energy demand, a low power and low offset time domain comparator (TDC), first proposed by [16], was adopted.

Instead of compare input voltages using a preamplifier and a latch as conventional ones, the time domain comparator first transform both inputs form the voltage domain to the time domain by means of a simple ramp generator as illustrated in Figure 6.

When *compare* signal is low, the capacitor C_1 is charged through M_1 while any parasitic charge in R_1 is discharged through M_5 and the *cmpOut* net is cleared by M_7. When *compare* signal rises, M_2 becomes a closed switch and M_4 acts like a constant current source proportional to the input voltage (V_{in}), discharging C_1 at constant time rate through $R_1 + r_{ds2} + r_{ds4}$. When the

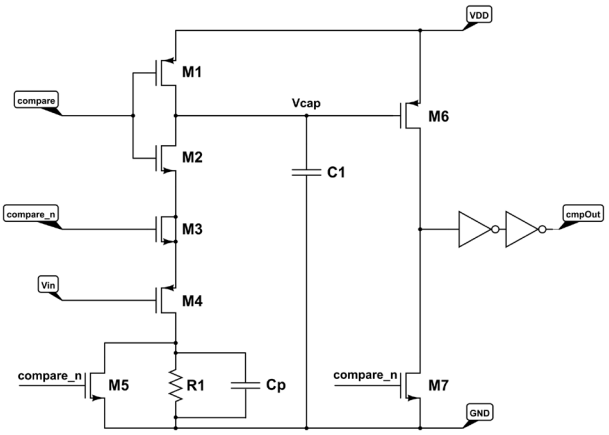

Figure 6. Voltage to time converter used in time domain comparator.

voltage at the top plate of capacitor C_1 fall below the threshold voltage of M_6 the *cmpOut* output goes high. The same procedure is made simultaneously to both inputs. The greater voltage will provoke a faster rising of *cmpOut* output which can be easily identified with the help of a D type flip-flop. Parasitic charges induced by M_2 are compensated by the dummy transistor M_3. The complete diagram of designed time domain comparator is represented in Figure 7.

The minimum detectable voltage difference at input is given by:

$$\Delta V_{in} = \frac{\Delta T \cdot {V_{R_1}}^2}{R_1 C_1 \Delta V_{out}} \tag{6}$$

where $\Delta V_{in} = V_{in\_p} - V_{in\_n}$, ΔT is the minimum delay between flip-flop inputs to guarantee a correct output, V_{R1} is the voltage across R_1 and ΔV_{out} the voltage drop on V_{cap} net [16].

In order to maximize the comparator accuracy a fully customized D flip-flop was designed. Transistor level simulations (including parasitics) reveal a $\Delta T \approx 26$ ps, which is more than five times faster than the corresponding standard cell. Furthermore, the R_1C_1 product

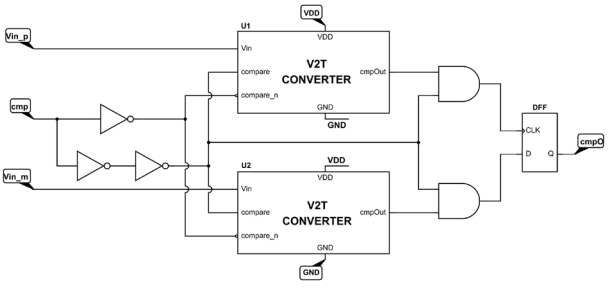

Figure 7. Diagram of designed time domain comparator.

is approximately 0.87 μs, $V_{R1} \approx 180$ mV and $\Delta V_{out} \approx 490$ mV resulting $\Delta V_{in} \approx 20\,\mu$V. Post layout simulations indicates a slightly greater value for ΔV_{in}, $\approx 30\,\mu$V, but this result should be suppressed by the thermal voltage noise associated to C_1 which is about 108 μV.

VII. SIMULATED RESULTS

The ADC was designed in 1P6M 180 nm CMOS process. A chip layout is shown in Figure 8. The total chip occupies 2.0 × 1.0 mm^2 and the ADC core area is 238 × 214 μm^2. A similar converter with less resolution bits was been experimentally evaluated in [7].

Static simulations were performed in order to measure the differential non-linearity (DNL) and the integral nonlinearity (INL) which gives +0.56/−0.12 and +0.69/−0.88 LSB, respectively.

The FFT spectrum was evaluated using 65536 points with 0 dB normalized sinusoid inputs at 2.92 kHz and 44.8 kHz as shown in Figure 10 and Figure 11. The measured SNDR is 58.93 dB and the SFDR is 78.04 dB.

Results indicate ENOB equals 9.5 bits. The total power consumption with 1 V supply voltage is 7.29 μW at 118 kS/s which corresponds to a figure of merit (FoM) equals to 85.3 fJ/conversion-step. According to these results, the proposed ADC is suitable to integrate a fully passive HF RFID sensor tag working at few centimeters to the reader´s antenna or a passive UHF RFID sensor tag at ~10 m from the reader [7] which meets the stablished power constraint as explained in section III.

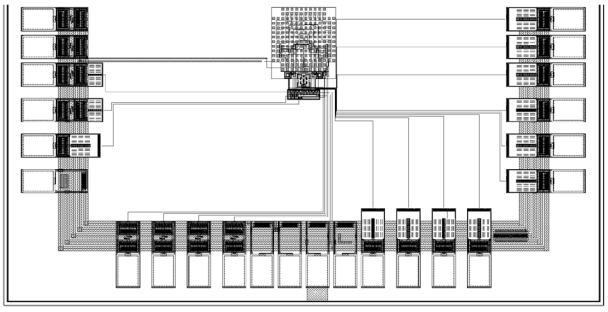

Figure 8. ADC layout in 1P6M 180 nm CMPOS process.

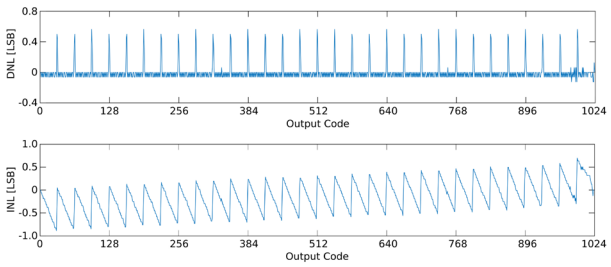

Figure 9. Measured DNL and INL error of fabricated ADC

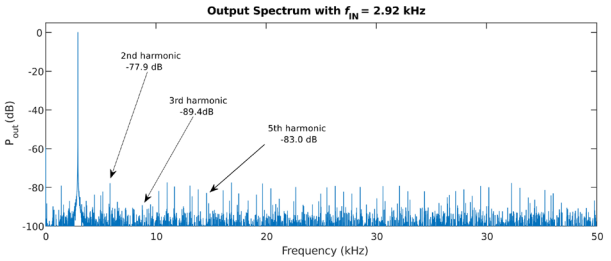

Figure 10. Output spectrum of designed ADC for an input frequency of 2.92 kHz.

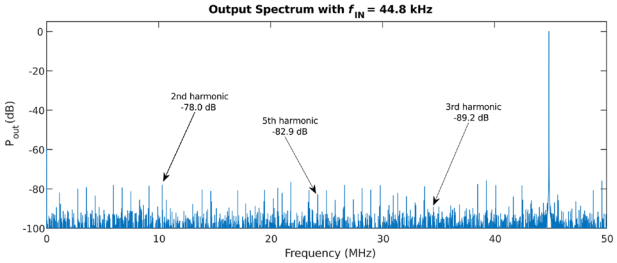

Figure 11. Output spectrum of designed ADC for an input frequency of 44.8 kHz.

CONCLUSION

The main considerations to design an analog to digital converter for RFID sensor tags was been presented. A survey analysis on analog to digital converters was been made over more than 400 reported converters. Analysis shows that over the last eight years, the successive approximation register A/D based on capacitive DAC is the most appropriated solution achieving the best results in technology nodes below 350 nm. An ultra-low power 10-bit SAR ADC was designed according to the main characteristics suitable for passive RFID sensors found on the previous survey analysis. The main design guidelines of the proposed ADC were discussed and simulation results were presented. The optimization method proposed for SAR circuit enabled its power consumption to be reduced by 90 % which represents a reduction of about 70% in overall converter consumption when compared with one achieved using the vendor standard cell library. The reliability of simulation results is reinforced by a previous similar implementation in the same technology process experimentally validated. The figure of merit of designed ADC achieves 85.3 fJ/Conversion-step at 118 kS/s and 1V supply. Finally, static analysis indicates an ENOB equal to 9.5 bits.

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