Analysis and Design of a Low Noise Shunt-Shunt CMOS Transimpedance Amplifier for 10 Gbps Optoelectronic Receivers

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***Abstract*—This article presents a complete design flow of a low noise transimpedance amplifier for 10 Gbps optoelectronic receivers. The proposed topology is based on the shunt-shunt structure with negative feedback. A set of equations was deduced from the frequency analysis and noise analysis. An optimization algorithm is proposed in order to maximize the bandwidth and improve the noise performance simultaneously. Experimental results shown a 51 dBΩ transimpedance gain, a 10.54 Ghz bandwidth and an input referred current noise equal to 6.8, the lowest one between other state-of-art designs. The circuit was manufactured in 130 nm RF CMOS technology.**

Index Terms—Transimpedance Amplifier, Optoelectronic Receiver, Low Noise Amplifier, RF CMOS.

I. Introduction

The huge growth in communication systems due to multimedia systems, high speed data-centers and other applications requires a corresponding bandwidth. Optical technology can overcome traditional limitations of electrical interconnects and keep the necessary bandwidth growth for the emerging applications [1-4]. The demand for higher bit rates on optical networks pushes the systems' noise limits to the lowest possible levels and the design of state-of-the art integrated electronic devices are definitely helping pave the way to make communication systems much faster and more reliable.

The first electronic device in an optical receiver after the photodetector is the transimpedance amplifier (TIA), which is responsible to convert the photodetector current into a voltage signal. The TIA must have a low input referred current noise to maximize the overall receiver sensitivity and mitigate the noise from succeeding stages [5]. In addition, the bandwidth of the TIA needs to be large enough for the required bit rate in order to minimize the intersymbol interference (ISI) [6].

A well known TIA topology is the RGC (regulated gain cascode) [7-12]. RGC TIA offers some attractive features like low input impedance and small area but the noise performance is not adequate for long-haul optical communication systems. The input referred noise of RGC based TIAs is tightly related with gain and bandwidth requirements that make this topology not attractive when noise performance is critical.

In this paper, we present a low-noise transimpedance amplifier implemented in 130 nm CMOS technology with 10.5 GHz bandwidth and 51 dBΩ transimpedance gain suitable for 10 Gbps optical receiver applications. A new design methodology is proposed in order to minimize the input referred current noise and maximize the bandwidth.

II. The Shunt-Shunt Topology

Shunt-shunt feedback transimpedance amplifiers are by far the most popular circuit for converting small photodetector current into a voltage signal. In this section is presented the frequency analysis and a general equation for the maximum transresistance gain as a function the number stages of the shunt-shunt topology.

A. Frequency Analysis

The shunt-shunt TIA topology is shown in Fig. 1 [6]. This topology is composed by a voltage amplifier with a transfer function given by A(s) and a feedback resistor R_f connected between its input and output nodes. This configuration is also known by "voltage-current" feedback, where a negative feedback network (the feedback resistor) senses the voltage at the output and returns a proportional current to the input. This type of feedback is chosen for a TIA circuit because it lowers both the input and output re-sistances, thus increasing the input pole magnitude and allowing the amplifier to absorb the photodetector current, and also yielding a better drive capability [6].

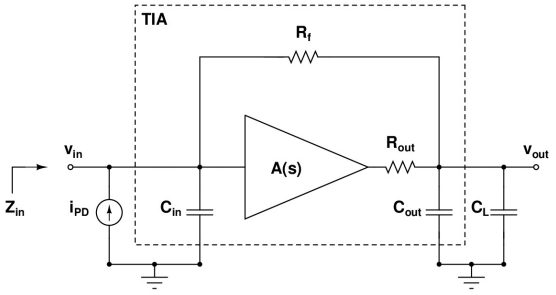


Fig.1 Shunt-shunt feedback TIA.

The transimpedance equation and some design equations can be obtained if we apply the Kirchhoff's Current Law

(KCL) in the input node of the voltage amplifier in Fig. 1. The transimpedance ZT can be obtained as follows. Sup-pose that the voltage amplifier has a transfer function given by the equation 1 and Av >> 1:

$$A(s) = \frac{A_v}{1 + \frac{s}{\omega_v}} \tag{1}$$

If we apply the KCL at the input node in Fig. 1, we have:

$$i_{PD}(s) = \left(sC_{in} + \frac{1}{R_f}\right)v_{in}(s) + \left(-\frac{1}{R_f}\right)v_{out}(s), \tag{2}$$

where i_{PD} is the photodetector current. Since

$v_{in}(s) = \frac{v_{out}(s)}{A(s)}$, from equation 1 we obtain the following expression for the transimpedance:

$$Z_T(s) = \frac{v_{out}(s)}{i_{PD}(s)} = \frac{-A_v R_f}{\left(\frac{R_f C_{in}}{\omega_v}\right)s^2 + \left(R_f C_{in} + \frac{1}{\omega_v}\right)s + (1 + A_v)} \tag{3}$$

The input impedance Z_{in} is obtained in a similar procedure by substituting $v_{out}(s) = A(s) \cdot v_{in}(s)$ into the equation (2) into the equation 2, according to the equation 4:

$$Z_{in}(s) = \frac{R_f\omega_v + R_f s}{R_f C_{in} s^2 + \left(R_f C_{in}\omega_v + 1\right)s + \omega_v(1 + A_v)}. \tag{4}$$

From equations 3 and 4, we can evaluate the transimpedance gain and the input impedance at low frequencies (s ≈ 0) according to the equation 5 and 6, respectively:

$$R_T(s) = -\frac{A_v}{(1 + A_v)}R_f \approx -R_f \tag{5}$$

$$R_{in}(s) = \frac{R_f}{(1 + A_v)} \tag{6}$$

Equation 5 reveals that the feedback resistor R_f sets the transimpedance value and must be maximized to minimize its noise contribution at the TIA input. Equation 6 relates R_f and the voltage amplifier gain Av at low frequencies. This equation suggests that there is a trade-off between the DC transimpedance value and bandwidth, since the input pole sets the overall TIA bandwidth.

A first approximation for the TIA poles can be evaluated if we write the denominator of equation 3 like a second order system transfer function [12], expressed by the equation 7:

$$\left(\frac{R_f C_{in}}{\omega_v}\right)s^2 + \left(R_f C_{in} + \frac{1}{\omega_v}\right)s + (1 + A_v) = s^2 + 2\zeta\omega_{TIA}s + \omega_{TIA}^2 \tag{7}$$

where ζ is the "damping factor" and ω_{TIA} is the natural frequency of the TIA. For a critical damping, ζ must be equal to $\sqrt{2}/2$. If ζ < $\sqrt{2}/2$ the step response exhibits ringing, creating ISI and corrupting the high and low levels of the transmitted data. Rewriting equation 3, we have:

$$Z_T(s) = \frac{v_{out}(s)}{i_{PD}(s)} = \frac{\left(\frac{A_v\omega_v}{C_{in}}\right)}{\left(s^2 + \frac{R_f C_{in} + 1/\omega_s}{R_f C_{in}/\omega_v}s + \frac{1}{\omega_v}\right)s + \frac{(A_v + 1)\omega_v}{R_f C_{in}}}. \tag{8}$$

A comparison between equation 7 and denominator in the equation 8 give us the following equation for the "damping factor":

$$\zeta = \frac{1}{2}\frac{R_f C_{in}\omega_v + 1}{\sqrt{R_f C_{in}\omega_v(A_v + 1)}}. \tag{9}$$

The voltage amplifier bandwidth is obtained from equation 9 for $\zeta = \frac{\sqrt{2}}{2}$, according to equation 10:

$$\omega_v = \frac{A_v \pm \sqrt{A_v^2 - 1}}{R_f C_{in}} \approx \frac{2A_v}{R_f C_{in}}. \tag{10}$$

Finally, the -3 dB bandwidth of the second-order TIA is obtained by comparing the last terms of equation 7 and the polynomial in equation 8, according to equation 11:

$$\omega_{TIA} = \sqrt{\frac{(A_v + 1)\omega_v}{R_f C_{in}}} \approx \frac{2A_v}{R_f C_{in}}. \tag{11}$$

Equation 11 shows that the TIA and the voltage amplifier must have the same bandwidth when the critical damping condition is satisfied. We also conclude that voltage gain of the voltage amplifier in Fig. 1 must be maximized as much as possible in order to improve the TIA bandwidth.

B. Maximum Transimpedance Gain for n Stages

An estimate of the maximum transimpedance value of the shunt-shunt topology can be obtained from the TIA gain-bandwidth product. Fig 2 shows a TIA diagram with n post amplifier stages:

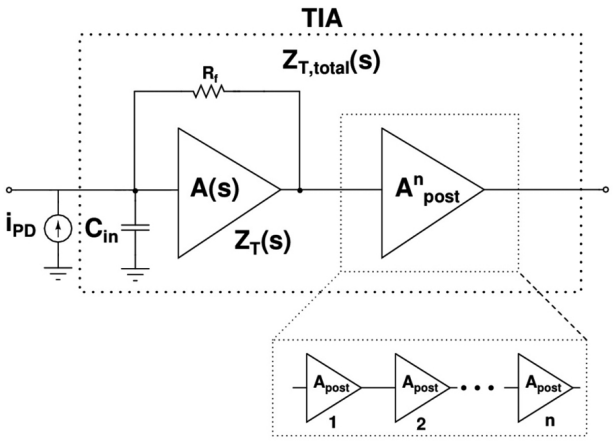


Fig.2 Shunt-shunt TIA with n voltage gain stages.

Thus, Fig. 1 is a particular case for the TIA with only 1 stage. In this condition and assuming that the voltage amplifier in Fig. 1 has only one dominant pole, the relationship between the gain-band product (GBW) and the transition frequency f_T is given by equation 12:

$$\left[A_v\left(2\pi f_{3dB}\right)\right]_{GBW} \le f_T \tag{12}$$

where

$$f_{3dB} \approx \frac{1}{R_{in}C_{in}} \tag{13}$$

is the required -3dB bandwidth. From equations 12 and 13 and assuming that $R_{in} \approx R_T / A_v$ for $A_v \gg 1$, the maximum transimpedance value for low frequencies is given by equation 14:

$$R_{T,\max} \le \frac{f_T}{2\pi C_{in} f_{3dB}^2} \tag{14}$$

Equation 14 gives an important relation between f_T, C_{in} and f_{3dB}. This result can be extended for multiple gain stages, according to equations 15 and 16:

$$Z_{T,total}(s) = Z_T(s)\prod \frac{A_{post}}{\left(\frac{s}{\omega_{post}}\right)^2 + \left(\frac{s}{Q_{post}\omega_{post}}\right) + 1} \tag{15}$$

$$R_{T,\max} = R_T A_{post}^n = R_f \frac{A_v A_{post}^n}{A_v + 1} \tag{16}$$

In equation 15, A_{post}^n is the voltage gain of each post amplifier stage according to Fig. 2. The total bandwidth drops rapidly when the subsequent stages are added to the shunt-shunt TIA. Assuming that the TIA and the voltage amplifiers have the same cutoff frequency, the total bandwidth is given by Equation 17:

$$f_{3dB,total} = f_{post}\left(2^{1/(n+1)} - 1\right)^{1/4}, \tag{17}$$

where f_{post} is the 3 dB frequency of each additional amplifier.

The total bandwidth of the shunt-shunt TIA with n stages of amplification can be expressed as a function of the voltage gain A_v of the core amplifier, the input capacitance C_{in}, the transresistance R_T and the voltage gain of each additional voltage amplifier A_{post}. If we plug equation 11 into equation 17, we obtain the total bandwidth of the TIA according to equation 18:

$$BW_{total} = \frac{A_{post}^n}{2\pi C_{in} R_{T,total}} \cdot A_v \sqrt{\frac{2A_v}{A_v + 1}} \left(2^{1/(n+1)} - 1\right)^{1/4}, \tag{18}$$

From equation 17, the 3 dB frequency of each postamplifier in Fig. 2 is given by equation 19:

$$f_{post} = \frac{f_{3dB,total}}{\left(2^{1/(n+1)} - 1\right)^{1/4}}, \tag{19}$$

Since the gain-bandwidth product of each postamplifier satisfies the expression 20:

$$A_{post} f_{post} \le f_T, \tag{20}$$

the voltage gain of each post amplifier is obtained if we plug equation 19 into equation 20, according to equation 21:

$$A_{post} \le \frac{f_T\left(2^{1/(n+1)} - 1\right)^{1/4}}{f_{3dB,total}}. \tag{21}$$

Finally, the maximum transimpedance gain at low frequencies for the shunt-shunt topology with n post amplifier stages is given by equation 22:

$$\begin{aligned} R_{T,total} &\le \frac{\left[\frac{f_T\left(2^{1/(n+1)} - 1\right)^{1/4}}{f_{3dB,total}}\right]^n}{2\pi C_{in} f_{3dB,total}} \\ &\times \frac{f_T\left(2^{1/(n+1)} - 1\right)^{1/4}}{f_{3dB,total}} \left(2^{1/(n+1)} - 1\right)^{1/4} \\ &\le \frac{\left(f_T\right)^{n+1}}{2\pi C_{in}\left(f_{3dB,total}\right)^{n+2}} \left(2^{1/(n+1)} - 1\right)^{(n+2)/4}. \end{aligned} \tag{22}$$

Fig. 3 shows the maximum transresistance gain as a function of the number of stages and the transit frequency for different technologies nodes.

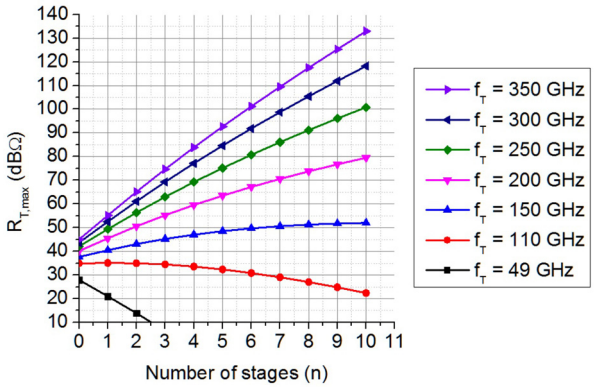


Fig.3 Maximum transimpedance gain for BW_{total} = 56GHz.

In this example, a 56 GHz bandwidth was considered for a 80 Gbps data rate[1]. In many applications, the transimpedance gain has a typical value in the range of 48 dBΩ − 60 dBΩ. Thus, for a 80 Gbps application the designer must choose a technology that offers, at least, a transit frequency greater or equal to 200GHz. In this example, a 56 GHz bandwidth was considered for a 80 Gbps data rate[1]. In many applications, the transimpedance gain has a typical value in the range of 48 dBΩ − 60 dBΩ. Thus, for a 80 Gbps application the designer must choose a technology that offers, at least, a transit frequency greater or equal to 200GHz.

III. The Proposed Circuit and Design Methodology

The proposed topology is a double cascode TIA with negative shunt-shunt feedback and inductive peaking techniques, optimized for very low noise performance [14-17]. Fig. 4 shows the TIA schematic.

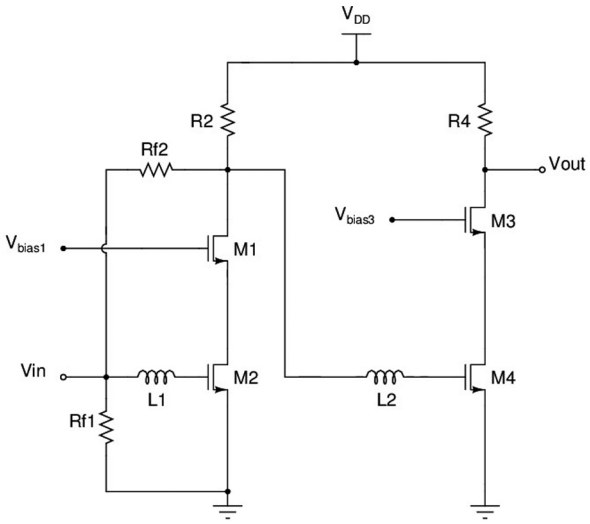


Fig.4 Two stage cascode schematic (bias circuits not shown).

The cascode topology was selected since it presents high output resistance and low Miller effect at the TIA input node. The number of postamplifier stages was defined ac-cording to equation 22 and Fig. 5:

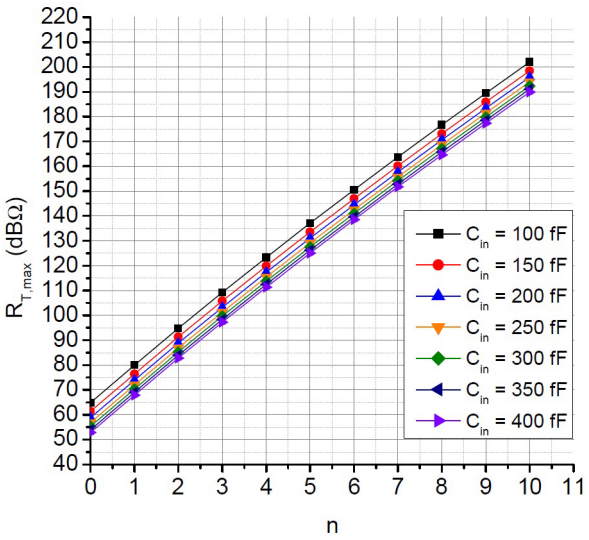
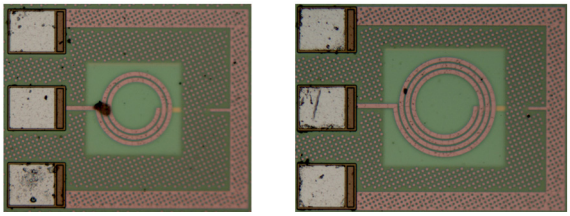


Fig.5 Number of post amplifier stages and $R_{T,max}$.

Fig. 5 shows the maximum transimpedance as a function of number of post amplifier stages for f_T = 110GHz, f_{3dB}=10GHz and $C_{in} \approx 400fF$. Thus, in our case, for a maximum transimpedance gain between 52 dBΩ ≤ $R_{T,max}$ ≤ 67 dBΩ, n = 1 is enough for a 10 Gbps speed. The bias point of each transistor was carefully selected in order to guarantee a low noise performance. The inductors were designed for high Q performance. The microphotographs of each inductor are shown in Fig. 6(a) and 6(b).



(a) L1 = 700 pH. (b) L2 = 1:7 nH.

Fig.6 Microphotograph of the circular inductors.

Each inductor was designed at the top metal layer (metal 8) in order to minimize the parasitic capacitance to the substrate. The inductance values were obtained in step 6 of the proposed noise optimization algorithm presented in D sub-section. The TIA input capacitance was optimized consider-ing the current density ($I_{DS/W}$) defined in table II. This bias-ing point guarantees that the transistors are close to the NF minimum (fig.11(a)). Fig. 7 shows the double cascode microphotograph.

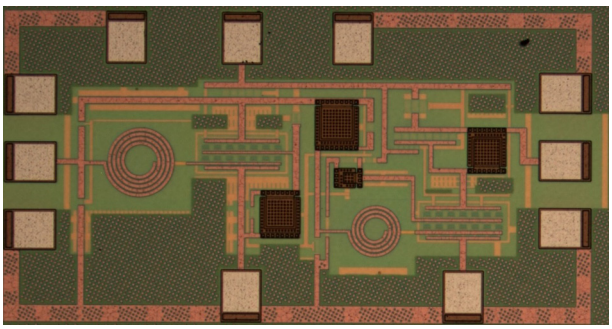


Fig.7 TIA microphotograph.

All metal line in the TIA layout were designed as microstrip transmission lines in order to minimize the losses and improve the overall performance [18-22]. Dummy blockers for metal fillers were included in final layout in order to avoid metal fillers over the active area of the circuit. Fig. 8 shows the microprotograph of the manufactured microstrip line.

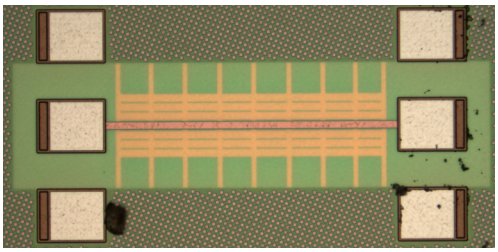


Fig.8 Microstrip line microphotograph.

The microstripline was designed at the top metal layer. Fig. 9 shows the microstripline S-parameters obtained from simulations and experimental results.

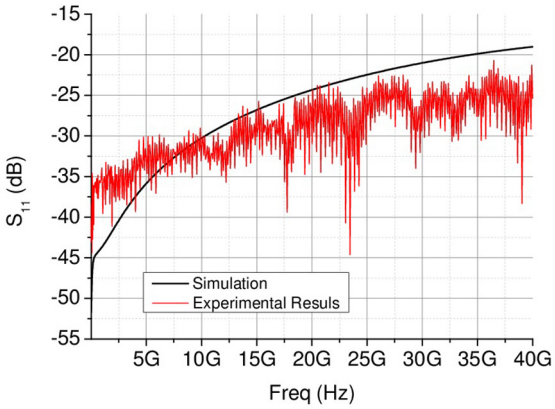


Fig.9 S11 parameter of the microstrip line.

The microstrip was designed to a 50 Ω characteristic impedance. S-parameters were performed up to 40 GHz. Fig.9 shows that the microstrip is matched to 50Ω from 10 MHz up to 40 GHz, as predicted from simulations.

B. Biasing Optimization for Low Noise Performance

The biasing point of the TIA transistors was carefully defined by the characterization of the nMOS transistor. Some simulations were performed with the testbench shown in Fig.10 in order to find the best biasing operation point.

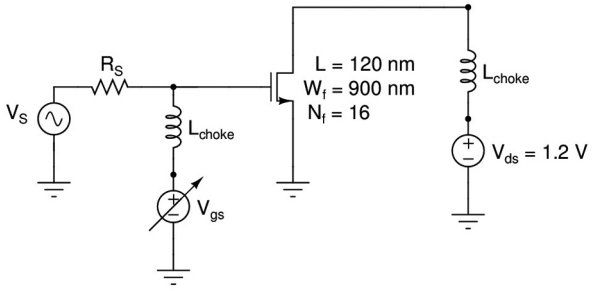


Fig.10 nMOS transistor test bench.

The transit frequency (f_T), minimum noise figure (NF_{min}), intrinsic gain ($g_m r_o$) and current density (I_{Dens}) plots, as a function of the gate-source voltage (V_{gs}), were obtained from the nMOS test bench shown in Fig. 8. These plots are shown in Fig. 11(a) in the same horizontal axis. The g_m/I_{ds} plot was also obtained and it is shown in Fig. 11(b).

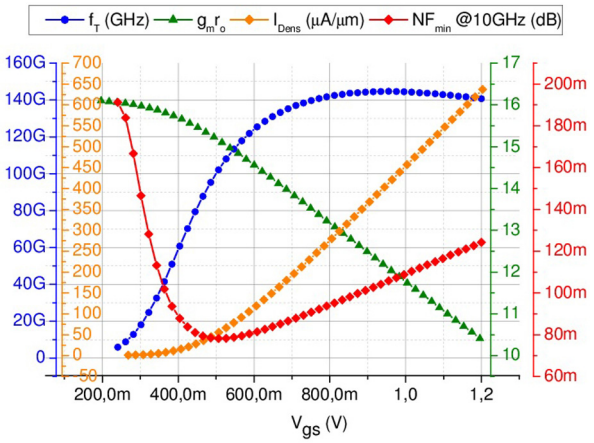
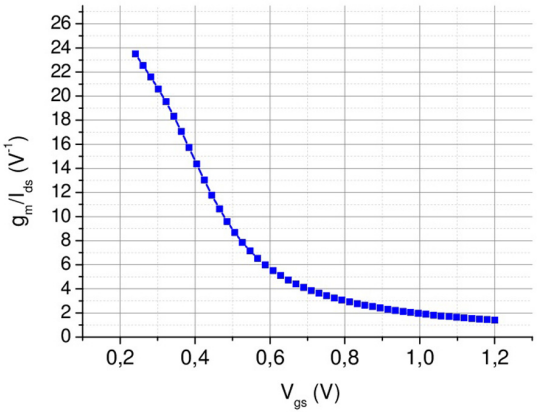


Fig.10 nMOS transistor test bench.

(a) nMOS plots for biasing optimization.



(a) gm=Ids plot for the nMOS transistor

Fig.11 nMOS transistor plots for biasing optimization.

From these plots, a set of constraints was defined for the circuit biasing point:

$$400mV \le V_{gs} \le 600mV, \quad (23)$$

$$6 \le \left(\frac{g_m}{I_{ds}}\right) \le 15 \quad (24)$$

$$25\mu A/\mu m \le \left(\frac{I_{ds}}{W}\right) \le 125\mu A/\mu m \quad (25)$$

Equations 23, 24 and 25 define the target biasing operation point for the TIA. The gate-source voltage (V*gs*) defined by equation 23 assures that the transistors operates near the noise figure minimum and equations 24 and 25 help to define the transistors dimensions [23,24].

C. Noise analysis

The Noise performance of transimpedance amplifiers is evaluated by the input referred noise current normalized in the passband [15-17]. The noise generators in transimpedance amplifiers are modeled by current sources because the input signal is also given by a current source (i_{PD}). This representation facilitates the calculation of the signal-to-noise ratio (SNR) at the TIA input. It is important to highlight that the noise referred to the input is a more adequate metric to quantify the degradation of the SNR, since it does not depend on the voltage gain [6]. Fig. 12 shows the double cascode diagram with the noise sources.

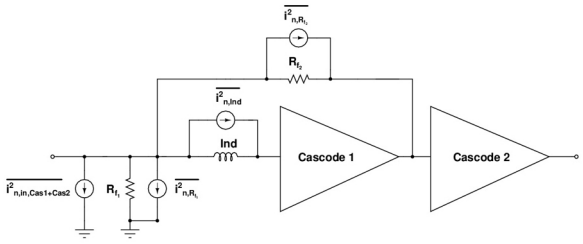


Fig.12 TIA diagram with noise sources.

In the diagram shown in Fig. 12, the current sources $\overline{i^2_{n,ind,Cas_1}}$ and $\overline{i^2_{n,ind,Cas_2}}$ represent the input referred noise of the first and second stages, respectively. Since each noise source is considered statistically independent from each other, the total TIA input referred noise is given by equation 26:

$$\overline{i^2_{n,in,TIA}} \approx \overline{i^2_{n,R_{f1}}} + \overline{i^2_{n,R_{f2}}} + \overline{i^2_{n,ind}} + \overline{i^2_{n,ind,Cas_1+Cas_2}}, \quad (26)$$

The noise generators of each cascode stage is obtained by the small signal analysis of the circuit [25-28] in Fig. 13.

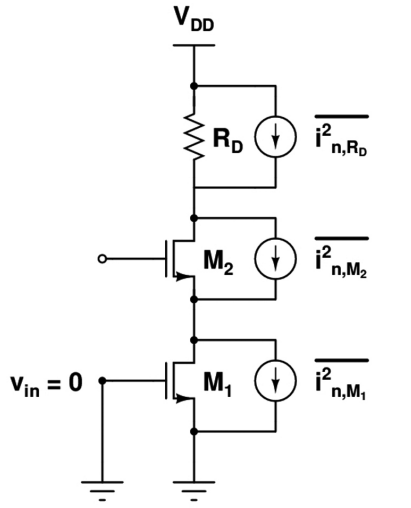


Fig.13 Cascode schematic to evaluate $\overline{v^2_{n,out,Cas_2}}$.

The input referred noise voltage of the TIA is given by equation 27

$$\overline{v^2_{n,in,Cas}} \approx \frac{\overline{v^2_{n,out,Cas}}}{A^2_{v,Cas}}, \quad (27)$$

where $\overline{v^2_{n,out,Cas}}$ is the output noise voltage and $A^2_{v,Cas}$ is the cascode voltage gain. Since the input signal of the TIA is the photodetector current, the noise at the input must be represented by a current source. This noise source is calculated as follows.

In equation 27, $\overline{v^2_{n,out,Cas}}$ is given by equation 28,

$$\overline{v^2_{n,out,Cas}} \approx \overline{i^2_{n,out,Cas}} \times R^2_D \approx 4kT\left\{\gamma(g_{m_1}+g_{m_2})+\frac{1}{R_D}\right\}\times R^2_D, \quad (28)$$

where R^2_D is the cascode stage transresistance (Z_T for s ≈ 0). The substitution of equation 28 into equation 27, give us the TIA input referred noise voltage:

$$\overline{v^2_{n,out,Cas}} \approx \frac{4kT\left\{\gamma(g_{m_1}+g_{m_2})+\frac{1}{R_D}\right\}\times R^2_D}{(g_{m_1}R_{out,Cas})^2}, \quad (29)$$

The small signal analysis of the cascode schematic results in equation 30 that relates the TIA output noise voltage with the input noise current [25]:

$$\overline{v^2_{n,out,Cas}} \approx \left[\overline{i^2_{n,out,Cas}}\left(\frac{1}{C_{in}\omega}\right)^2\right]_{\overline{v^2_{n,in,Cas}}} \cdot (g_{m_1}R_{out,Cas})^2, \quad (30)$$

Finally, the comparison between equation 29 and the term in brackets in equation 30, gives an approximation for the total input referred noise current:

$$\overline{i_{n,out,Cas}^2} \approx (C_{in}\omega)^2 \cdot \frac{4kTR_D\left\{\gamma R_D(g_{m_1}+g_{m_2})+1\right\}}{(g_{m_1}R_{out,Cas})^2} \quad (31)$$

Equation 31 reveals that the TIA input referred noise current has a quadratic behavior with frequency. A more accurate estimation of the noise at the TIA input can be obtained directly from S-parameters simulations according to equation 32 [29]:

$$\overline{i_{n,in}^2} = |1-S_{11}|\sqrt{\frac{(10^{\frac{NF}{10}})kT_0}{Z_0}} \quad (A^2/Hz) \quad (32)$$

In order to obtain the input referred noise current of the double cascode TIA, it is necessary to consider the noise contribution of the two stages, indicated by the current source $\overline{i_{n,in,Cas_1+Cas_2}^2}$ in Fig.12. An expression for this noise source can be evaluated by following steps:

1. *Find out the input referred noise voltage of the second stage (Cascode 2).*
   The input referred noise voltage of the second stage is calculated following the sequence given by equations 27, 28 and 29. The obtained expression is given by equation 33:

$$\overline{v_{n,in,Cas2}^2} \approx \frac{4kT\left\{\gamma(g_{m_3}+g_{m_4})+\frac{1}{R_4}\right\}\times R_4^2}{(g_{m_3}R_{out,Cas2})^2} \quad (33)$$

2. *Find out the input referred noise voltage of the first stage (Cascode 1),considering the noise source at the output of this stage and the noise source at the input of the second stage.*
   The input referred noise of the TIA, modeled by a voltage source is given by equation 34:

$$\overline{v_{n,in,Cas1+Cas2}^2} \approx \frac{\overline{v_{n,out,Cas1}^2}+\overline{v_{n,in,Cas2}^2}}{(A_{v,Cas1})^2} \quad (34)$$

where $v_{n,out,Cas1}^2$ and $v_{n,in,Cas2}^2$ are given by equations 35 and 36, respectively:

$$\overline{v_{n,out,Cas1}^2} \approx \frac{4kTR_2^2\left\{\gamma(g_{m_1}+g_{m_2})+\frac{1}{R_2}\right\}}{(g_{m_1}R_{out,Cas})^2}, \quad (35)$$

$$\overline{v_{n,in,Cas2}^2} \approx \frac{4kTR_2^2\left\{\gamma(g_{m_3}+g_{m_4})+\frac{1}{R_4}\right\}}{(A_{v,Cas2})^2}, \quad (36)$$

3. *Find out the noise contribution of the two cascodes referred to the TIA input considering the noise voltage source obtained in the previous step.*
   Following the same procedure for the single-stage cascade according to equations 30 and 31, the input referred current noise of the double cascode is given by equation 37,

$$\overline{i_{n,in,Cas1+Cas2}^2} \approx (C_{in}\omega)^2 \cdot \overline{v_{n,in,Cas1+Cas2}^2}, \quad (37)$$

where $\overline{v_{n,in,Cas1+Cas2}^2}$ is given by equation 38:

$$\overline{v_{n,in,Cas1+Cas2}^2} \approx \frac{\overline{v_{n,out,Cas1}^2}+\overline{v_{n,in,Cas2}^2}}{(v_{n,Cas1}^2)}, \quad (38)$$

4. *Add the noise source obtained in the previous step to the noise generators of the remaining elements.*
   Finally, the total noise at the input of the TIA is given by equation 39:

$$\overline{i_{n,in,TIA}^2} \approx \frac{4kT}{R_{f_1}}+\frac{4kT}{R_{f_2}}+\overline{i_{n,ind}^2}+\overline{i_{n,ind,Cas_1+Cas_2}^2}, \quad (39)$$

5. *The final step is to obtain the normalized mean square value of the equation 39.*
   The normalized root mean square value of is given by equation 40 [29]:

$$\overline{i_{n,in,TIA}^{RMS,BW}} = \sqrt{\frac{\int_0^{2BW}\overline{i_{n,in,TIA}^2}\,df}{BW}}\left(\frac{pA}{\sqrt{Hz}}\right), \quad (40)$$

Equation 40 is the final expression of the total input referred noise current. This expression is used to compare the performance of the proposed TIA with other published works. According to equation 39, it is necessary to optimize the thermal noise contribution of all circuit components in order to make the TIA noise as low as possible. The noise generated by the two cascodes has the greatest contribution to the total noise at the TIA input with the cascode 1 as the main contributor to the total noise at the input. The next subsection presents the proposed design flow to optimize noise and bandwidth of the TIA.

D. Proposed Design Flow

The proposed design flow for the low noise TIA is given by the following steps:

1) *Define an initial value to the feedback resistor R_{f2} from the DC transimpedance value:*

$$Z_{T_{(DC)}} \geq 48dB\Omega \Rightarrow R_{f_2} \geq 251.2\,\Omega,$$

2) *Plot the curves of f^T, NF_{min}, I_{ds}/W and g_m/I_{ds} for the nMOS transistor as a function of V_{gs}.*

3) *Define an interval for V_{gs} from the plots obtained in the previous step that ensures a DC operation near the NF_{min} minimum.*
4) *Find an initial approximation for I_{ds} / W e $g_m = I_{ds}$ from V_{gs} obtained in the previous step.*
5) *Define an initial value for the transconductance and output resistance of each cascode stage from the voltage gain and power consumption requirements. From these as-sumptions and the gm=Ids plot a initial value for the W/L relation can be obtained.*
6) *Optimize the input capacitance C_{in} of the cascode from the model defined by equations 37 and 38.*
7) *Repeat previous steps until the specifications are met.*

Table I shows the obtained components values of the TIA after the execution of the proposed algorithm described by the steps listed above.

TABLE I: Values and components of the TIA circuit.

TIA Stage	Components	Values and Dimensions
Cascode 1	M_1	$(W/L)_1$ = (7 x 16 x 2.5µm / 120 nm
	M_2	$(W/L)_2$ = (7 x 16 x 2.5µm / 120 nm
	L_1	1.6 nH
	R_{f1}	1 kΩ
	R_{f2}	300 Ω
	R_2	52 Ω
Cascode 2	M_2	$(W/L)_3$ = (7 x 16 x 2.5µm / 120 nm
	M_3	$(W/L)_4$ = (7 x 16 x 2.5µm / 120 nm
	L_2	720 pH
	R_4	50.6 Ω

Table II shows the bias point obtained after the proposed design flow was completed.

TABLE II: nMOS transistors biasing point.

Trans	Parameters					
	(W/L)	I_{DS}	V_{DS}	g_m	I_{DS}/W	g_m/i_{DS}
	µm/nm	mA	mV	mS	µA/µm	V^{-1}
M_1	(280)/(120)	14.5	544.4	127.3	51.6	8.8
M_2	(280)/(120)	14.5	526.4	134.8	51.6	9.31
M_3	(280)/(120)	17.0	551.5	142.5	61.0	8.33
M_4	(280)/(120)	17.2	546.3	141.0	61.5	8.19

The optimization of the double cascode input capacitance was obtained from the calculation of equation 31. The normalized RMS noise graph obtained by equation 39 is shown in Fig. 14 as a function of the TIA total input capacitance C_{in}.

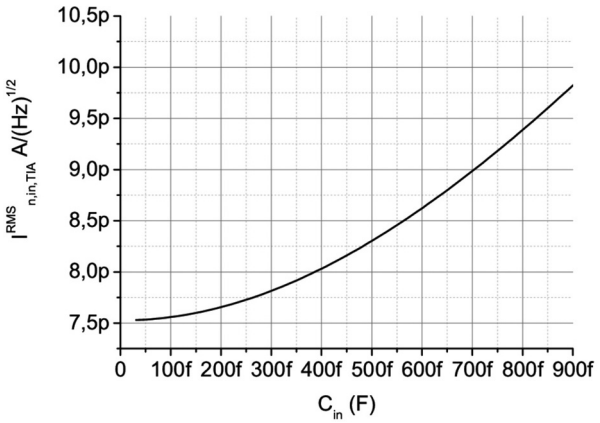


Fig.14 RMS input noise against TIA input capacitance (C_{in}).

The graph shown in Fig. 14 provides an estimate of M1 transistor width (W) at the TIA input. An approximation for the TIA input capacitance is given by equation 41:

$$C_{in} \approx C_{PD} + C_{PAD} + C_{in,M_1}, \quad (41)$$

The capacitances in equation 41 are described as follows:

- CPD is the photodiode capacitance, whose complete electrical model is given by Fig. 15 [30].

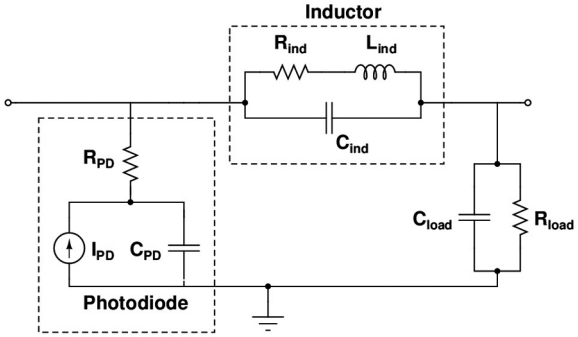


Fig.15 Equivalent circuit for the photodiode.

- In the equivalent circuit shown in Fig. 15, CPD = 15 fF RPD = 125Ω is the photodiode series resistance. The current source iPD models the electrical current generated by the photodiode. This model also includes an integrated inductor that enhances the photodiode bandwidth up to 67 GHz [30].
- C_{PAD} RF PAD parasitic capacitance. For the RF CMOS technology adopted in this work, C_{PAD} = 29 fF
- $C_{in;M1}$ is the parasitic capacitance of the transistor M1, given by equation 42:

$$C_{in,M_1} \approx C_{gs_1} + \left(1 + \frac{g_{m_1}}{g_{m_2}}\right) C_{gd_1}, \quad (42)$$

According to Figure 14, the total input capacitance of the TIA must be kept below 700 fF in order to keep the RMS input noise below 9 $pA/\sqrt{Hz}$. The width of the input transistor M1 can be obtained from equation 42 as follows:

$$\frac{2}{3}(WL)_{M_1} C_{ox} \leq 700 - 29 - 35f \; F \Rightarrow W_{M1} = 440\mu m.$$

A set of curves can be obtained for different values for the photodiode capacitance as shown in Fig. 16.

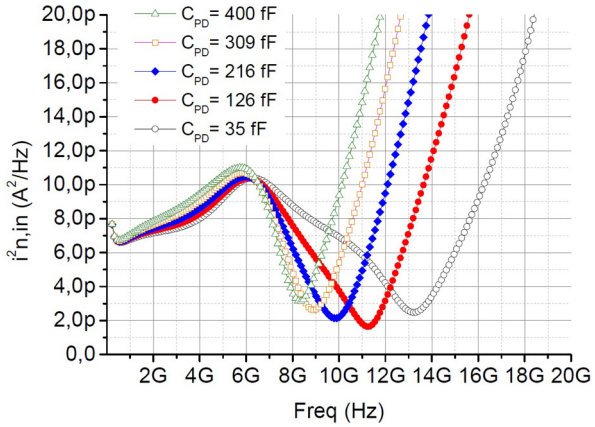


Fig.16 Input referred noise for different values of C_{PD}.

Fig. 16 shows that the input capacitance must be kept as low as possible since the input referred noise goes up with frequency.

In order for the TIA to be unconditionally stable over the whole bandwidth, the following conditions must be satisfied [5,31,32]:

$$K_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{|2S_{12}S_{21}|} > 1, \quad (43)$$

$$B_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2 > 0, \quad (44)$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}\cdot, \quad (45)$$

In equation 43, Kf is the stability factor and, in equation 44, B_{1f} is the auxiliary stability factor. The stability can also be evaluated by equation 46, where a single parameter is evaluated as reported by [33]:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22}\Delta S_{11}^*| + |S_{12}S_{21}|} > 1, \quad (46)$$

Simulations were performed up to the maximum oscillation of the adopted CMOS technology in this work (f_{max} = 110GHz). Fig. 17 and 18 show the stability factors K_f and B_{1f} obtained for the schematic and layout.

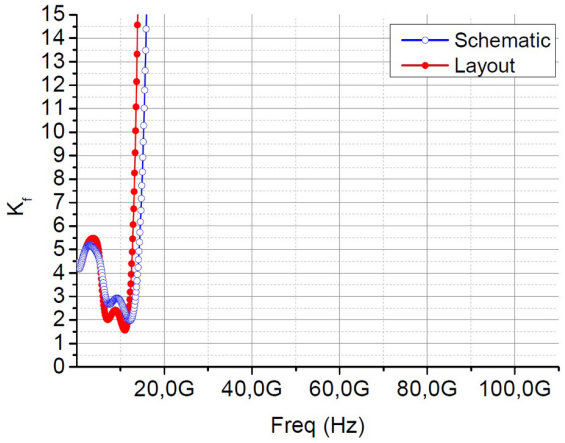


Fig.17 Stability factor K_f

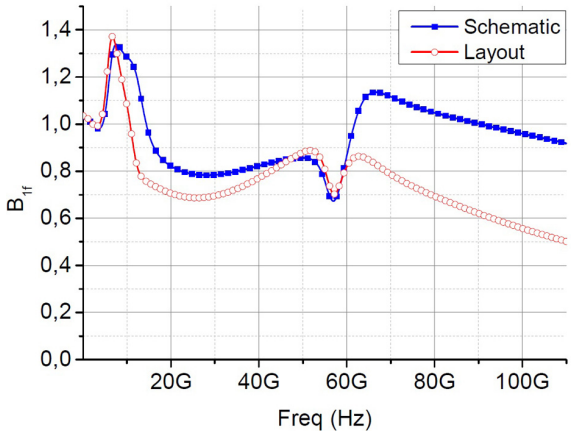
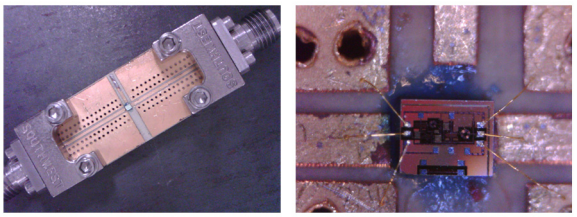


Fig.18 Auxiliary stability factor B_{1f}

The experimental results are presented in the next section.

IV. Experimental Results

The circuit was tested via on-wafer probing and mounted onto a RF microwave board. Fig. 19(a) and 19(b) show the chip mounted onto the PCB with connectors and the chip detail with bondwires connections, respectively.



(a) L1 = 700pH. (b) L2 = 1:7 nH.

Fig.19 Chip mounted onto a RF PCB board.

The RF PCB was designed and manufactured in our lab. The transmission lines were designed with the aid of 3D electromagnetic simulations.

Fig. 20 and 21 show the forward transmission gain (S_{21}) and the transimpedance gain (Z_T) of the TIA obtained from simulations and by experimental measurements, respectively.

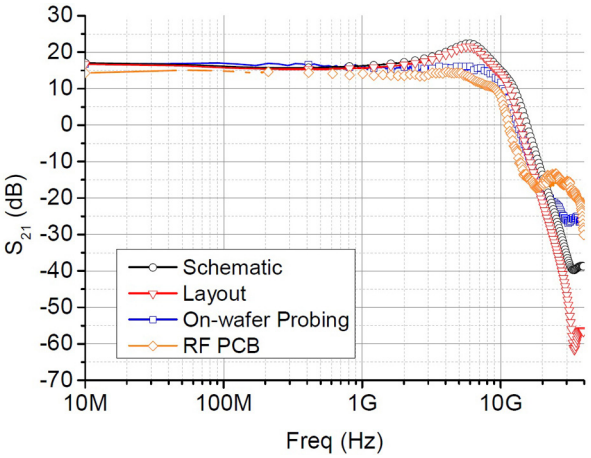


Fig.20 Simulated and measured forward transmission gain (S_{21}).

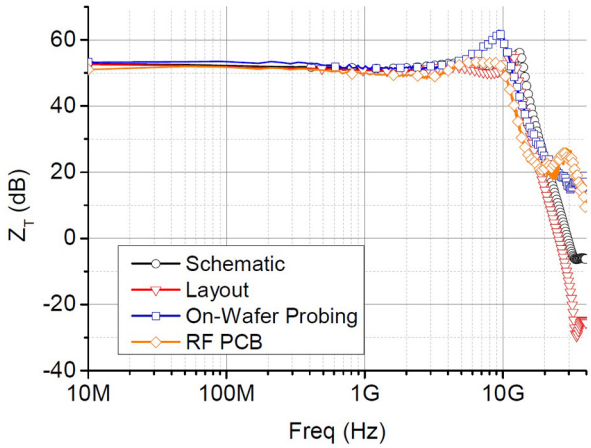


Fig.21 Simulated and measured transimpedance gain (Z_T).

The results presented on Fig. 20 show us that the TIA has a 14 dB forward transmission gain with a 7.4 GHz bandwidth. The circuit draws a bias current equal to 35 mA from a 1.2 V DC supply. The simulations were performed considering a 15 fF photodetector capacitance. Fig. 21 shows the results for the transimpedance gain that were obtained by the equation 43 from the S-parameters simulations [30]:

$$Z_T = 50\frac{S_{21}}{1-S_{11}} > 1 \quad , \tag{47}$$

The circuit has a 51 dBΩ transimpedance gain and a 10.54 GHz bandwidth for the experimental results obtained with the chip mounted onto the PCB. From Fig. 20 it is possible to see that there is a reduction on the bandwidth, from the schematic to the PCB measurements, approximately equal to 3.5 GHz.

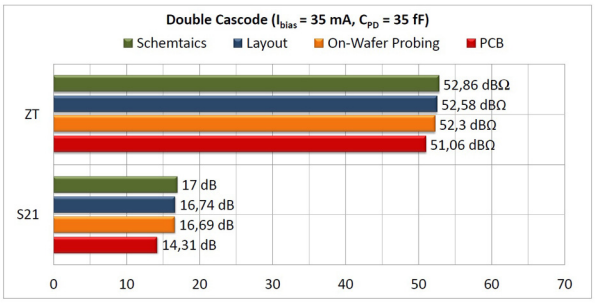


Fig.22 Z_T and S_{21} DC values.

The overall bandwidth reduction is due the board and bondwires parasitics. The circuit has enough bandwidth to operate in 10 Gbps data rates [6]. Fig. 22 and 23 show the DC values and the bandwidth for Z_T and S_{21} obtained from simulations and experimental results. From table II we can conclude that the biasing point of the double cascode TIA obey the set of constrains given by the equations 23, 24 and 25, necessary to keep the transistors working near the minimum of noise figure plot. Table III shows a complete summary and comparison with other state-of-art CMOS TIAs for 10 Gbps.

TABLE III: Sumary and comparison with other 10 Gbps TIAs.

Reference Year	[7]	[8]	[9]	[10]	[11]	This work
	2013	2015	2015	2015	2013	2015
Technology	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS
	130 nm	130 nm	130 nm	130 nm	130 nm	130 nm
Topology	RGC	RGC	RGC	RGC	RGC	Double Casc.
Z_T (dBΩ)	52,9	50,1	59	57	52,2	51
Vdd (V)	1.8	1.5	1.3	1.8	1.2	1.2
BW (GHz)	14,3	7.0	6,\.9	8.2	9.81	11.5
Noise $pA/\sqrt{Hz}$	39	31.3	20	21	12.8	6.8
Sensitivity (dBm)	-16.9	-17.8	-19.8	-19.6	-	-24.5
Power (mW)	2.7	2.5	16.9	22	1.88	30
Area (mm²)	0.002	0.02	0.051	0.6	-	0.16
FOM $\left(\frac{GHz\times dB\Omega}{pA/\sqrt{Hz}}\right)$	3592	74.70	23.62	1.69	-	17.97

From Table III, we can see that the proposed TIA has the lowest input referred noise current2 when compared to other state-of-art designs. The outstanding performance was achieved by applying the design flow method and the noise modeling proposed in this work.

V. Conclusion

A complete design flow and modeling procedure for low-noise CMOS transimpedance amplifiers were proposed in this work. The proposed circuit is based on a conventional

cascode topology and the shunt-shunt feedback topology. The experimental results show that the proposed architecture has the lowest input referred current noise when compared with other state of art designs. The pro-posed circuit was manufactured and tested onto a RF PCB. The circuit was manufactured in 130 nm CMOS technology and the obtained transimpedance bandwidth ensure a 10 Gbps data rate operation.

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