

# Bias Stress Effects in Low Temperature Amorphous Hf-In-ZnO TFTs Using RF-sputtering HfO<sub>2</sub> as High-k Gate Dielectric.

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**Abstract** — In this work we analyze the electrical performance, contact resistance and the effects of positive and negative gate-bias stress of Hf-In-ZnO/HfO<sub>2</sub> thin film transistors. Devices were fabricated using RF-magnetron sputtering at room temperature and fully patterned, with operation voltage below 6 V. Devices with drain-currents up to 2x10<sup>-6</sup> A and threshold voltages of ~2 V were analyzed under negative and positive gate bias stress. Devices under negative gate-bias stress showed a slightly threshold voltage shift due to the transistor channel is depleted of electrons at the channel/dielectric interface. Devices under positive gate-bias stress, showed threshold voltage shifts in the negative direction due to the reversible charge/discharge effect of the electrons in pre-existing high-k HfO<sub>2</sub> bulk traps. Positive gate-bias stress does not cause any degeneration, since stressed devices tend to recover after 5 mins.

**Keywords** — AOSTFTs, stability, contact resistance, hump, bias stressing.

## I. INTRODUCTION

In recent years, amorphous oxide semiconductor thin film transistors (AOSTFTs) have attracted the interest of researchers due to their applications in flexible substrates, high mobility, and low-cost and low temperature fabrication process<sup>[1]</sup>. Within AOSTFTs, ZnO-based TFTs have had more enhancements in performance adding materials such as Hf, In, and Ga like Indium-Gallium-Zinc-Oxide (a-IGZO), Indium-Zinc-Oxide (IZO) and Hafnium-Indium-Zinc-Oxide (HIZO). HIZO TFTs have shown a better stability due to a better threshold voltage ( $V_T$ ) stability, lowering the conductivity of the active layer, and thus lowering the carrier concentration from 10<sup>19</sup> to 10<sup>16</sup><sup>[2]</sup>. Looking for alternative dielectrics to SiO<sub>2</sub> and SiN<sub>x</sub>, high-k dielectrics, such as AlO<sub>x</sub>, HfO<sub>2</sub> and TiO<sub>2</sub> have been used in AOSTFTs with deposition techniques such as atomic layer deposition (ALD)<sup>[3]</sup>, pulsed layer deposition (PLD)<sup>[4]</sup> and RF magnetron sputtering<sup>[5]</sup>.

Nevertheless, AOSTFTs still present several instabilities caused by illumination<sup>[6]</sup>, positive and negative bias stress<sup>[7]</sup>, ambient/surface interaction<sup>[8,9]</sup>, simultaneous light exposure/bias stressing [10], surface non-passivated<sup>[11]</sup> and interfacial defects<sup>[12]</sup>. Device performance and stability will depend on the device structure, on the material and thickness of the dielectric and semiconductor, as well as on the fabrication process. The device performance can also be affected by other factors, such as metal contact and contact resistance should be also considered. As it is known, oxide semiconductors are prone to instabilities during the process due to deposition and patterning processes during the formation of source-drain

(S/D) electrodes, therefore, it is critical to analyze the contact resistance, as this analysis is key for the implementation of the TFTs in circuit design.

Researchers have reported<sup>[7,10,13,14]</sup> that negative gate bias stress (NGBS) results in negligible changes in  $V_T$ , sub-threshold swing (S) and mobility ( $\mu_{\text{FET}}$ ) when the devices, with dielectrics such as thermal SiO<sub>2</sub> and ALD AlO<sub>3</sub>, are stressed in the dark, at room temperature and without surface passivation. Nevertheless, during the fabrication process, final annealing and deposition processes at temperatures > 200°C are performed. Some others, have reported a negative  $V_T$  shift and S degradation in ZTO<sup>[6]</sup>, IZO<sup>[15]</sup> and IGZO<sup>[16]</sup> TFTs.

Devices carried out with positive gate bias stress (PGBS), have showed a hump effect<sup>[17]</sup> and positive  $V_T$  shift<sup>[14]</sup> due to trap densities and with little or no change in S and  $\mu$ . Nevertheless, it has been exceptions, reporting an increase in mobility<sup>[18]</sup> attributed to trapping/detrapping and negative  $V_T$  shifts in the case of HfO<sub>2</sub><sup>[19]</sup>.

In a previous work<sup>[20]</sup>, we reported all RF magnetron sputtering at room temperature HIZO TFTs with HfO<sub>2</sub> as gate dielectric and metal-insulator-semiconductor (MIS) structures, with low operation voltage range. Since these devices are suitable to work at low operation voltages, in this work we analyze the stability in NGBS and PGBS, as well as the contact resistance with Al as metal contact. As far as we know, this is the first time this study is presented for devices with HfO<sub>2</sub>/HIZO layers, both deposited by RF sputtering at room temperature.

## II. EXPERIMENTAL PART

AOSTFTs were fabricated using a corning glass as substrate, cleaned by RCA. Then, 100 nm of Al were deposited by thermal evaporation as bottom gate contact. Then, 140 nm of HfO<sub>2</sub> and 40 nm of HIZO (Hf:In:Zn = 0.3:1:1 mol%) were deposited by RF sputtering at room temperature. HIZO and HfO<sub>2</sub> films were patterned by standard photolithography and wet and dry etching, respectively. Finally, 200 nm of Al were deposited and patterned by lift-off technique for the S/D top contacts. Cross section and top view of the devices are shown in Fig.1.

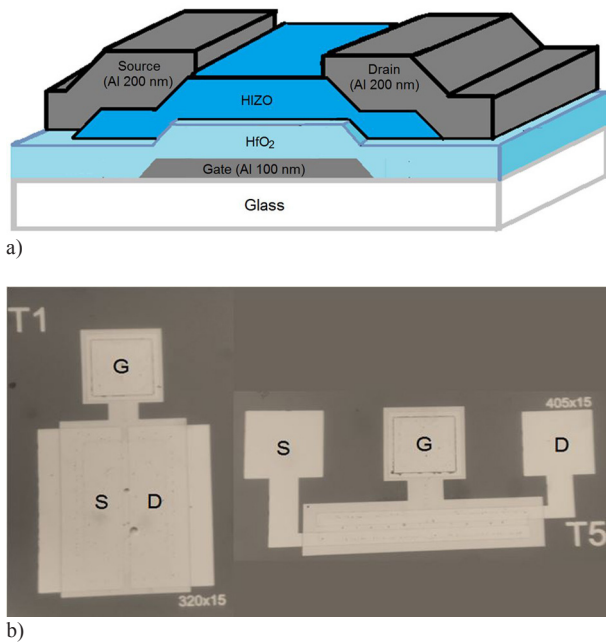
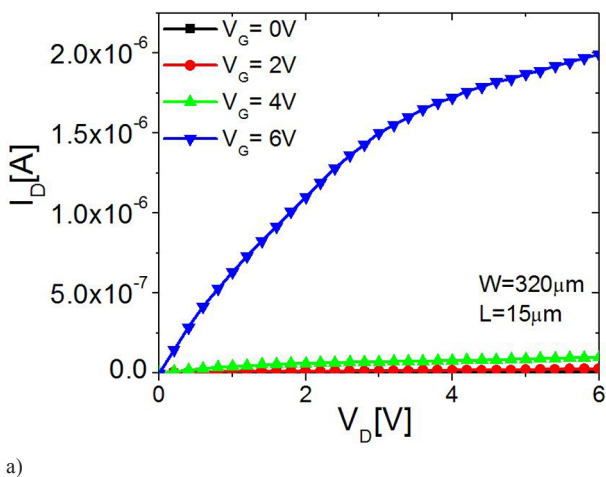


Fig. 1 a) Cross-section of HIZO TFTs. b) Top overview of two different fabricated transistors showing the two different layouts with  $W=320\ \mu\text{m}$  (left) and  $W=405\ \mu\text{m}$  (right).

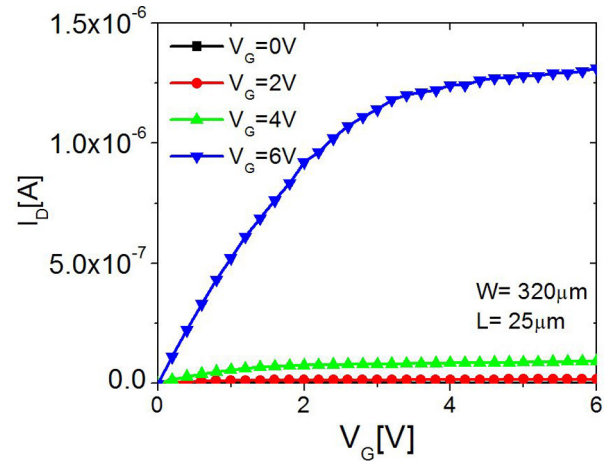
Gate bias stress was performed for 5 minutes at  $V_G = \pm 6\text{V}$ . The transfer characteristics were measured before and after applying the stress. Hysteresis was also measured and analyzed with hysteresis. The I-V measurements were performed using a Keithley 4200 semiconductor characterization system at room temperature in the dark.

### III. ANALYSIS AND DISCUSSION

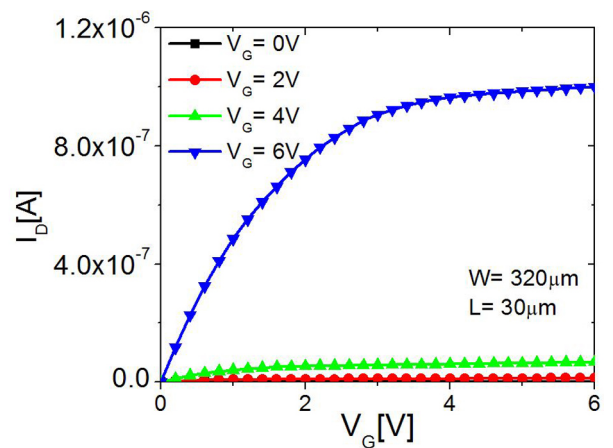
Figure 2 shows the output characteristics of three devices with different channel length (L): 15, 20, 25 and 30  $\mu\text{m}$ . As can be observed, there is significant increase in drain current when the gate voltage changes from 4 to 6 V. A similar behavior was found for IGZO-TFTs, which was attributed to the formation of oxide at the interfacial layer between Mg doped IGZO and Ti electrodes<sup>[21]</sup>.



a)



b)



c)

Fig. 2 Output characteristics of HIZO TFTs with  $W=320\ \mu\text{m}$  and a)  $L=15\ \mu\text{m}$  b)  $L=25\ \mu\text{m}$  c)  $L=30\ \mu\text{m}$ .

As ZnO-based materials are oxide semiconductors and both, Al and Ti, are highly sensitive to oxygen<sup>[22,23]</sup>, a dielectric interlayer can be formed at the S-D/active layer interface affecting the performance of the devices. Therefore, it is important to be analyze the presence of a contact resistance ( $R_c$ ). This effect was analyzed in our structures using the transmission-line method (TLM)<sup>[24]</sup> for the two different layouts (Fig 1b). As can be seen in Fig. 3 that, devices with  $W=405\ \mu\text{m}$  have a higher channel resistance ( $R_{ch}$ ) and  $R_c$  than devices with  $W=320\ \mu\text{m}$ , which can be explained due to the lower contact area for the first case. This contact effect is observed also in the output characteristics in Figure 4. Also, it is observed a drain current of  $10^{-7}\ \text{A}$ , an order of magnitude lower than devices with  $W=320\ \mu\text{m}$ .

Devices with the lowest  $R_c$  were analyzed in PGBS and NGBS. In Fig. 5, after PGBS it is observed a hump-effect, as well as,  $V_T$  shift to the left in the transfer curves. This  $V_T$  shift has been previously attributed to the increase of the trapped charge density at the dielectric/active layer interface<sup>[10, 25]</sup>. A similar behavior was found also for devices with HfO<sub>2</sub> deposited by ALD<sup>[26]</sup>.

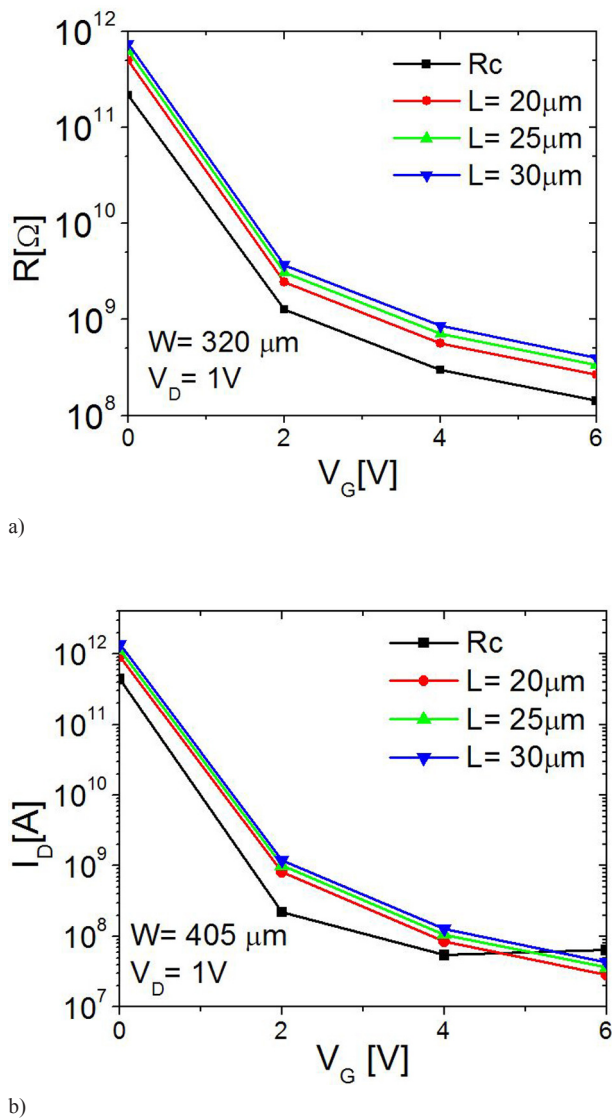


Fig. 3 Rc and Rch of devices with a)  $W=320 \mu\text{m}$  and b)  $450 \mu\text{m}$ .

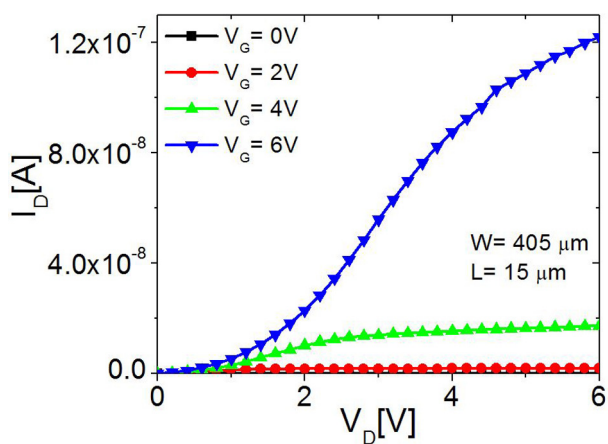


Fig. 4 Output characteristic of HIZO TFTs with  $W=405 \mu\text{m}$ .

It has been found that  $V_T$  shifts in the negative direction after PGBS due to the reversible charge/discharge effect of the electrons in pre-existing high-k HfO<sub>2</sub> bulk traps<sup>[26]</sup> and do not cause any degeneration as it can be observed in Fig. 5, that stressed devices tend to recover after 5 mins.

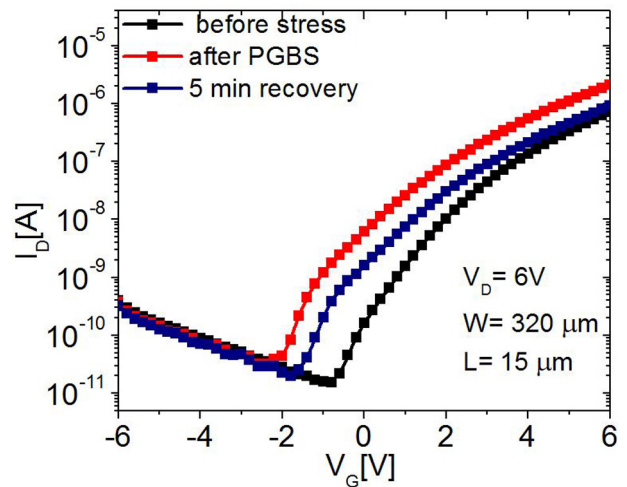
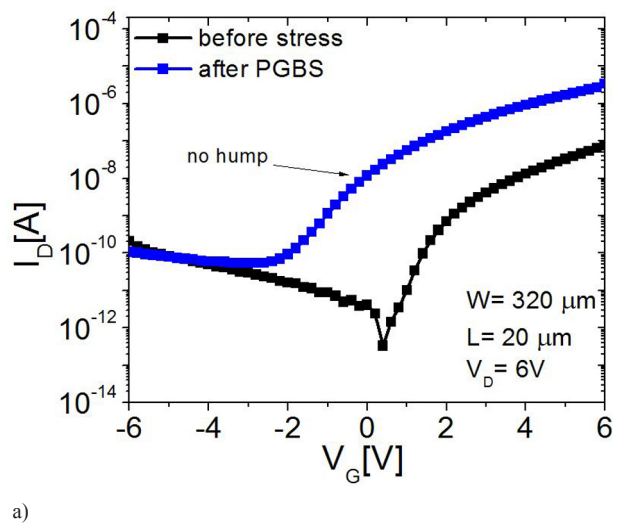


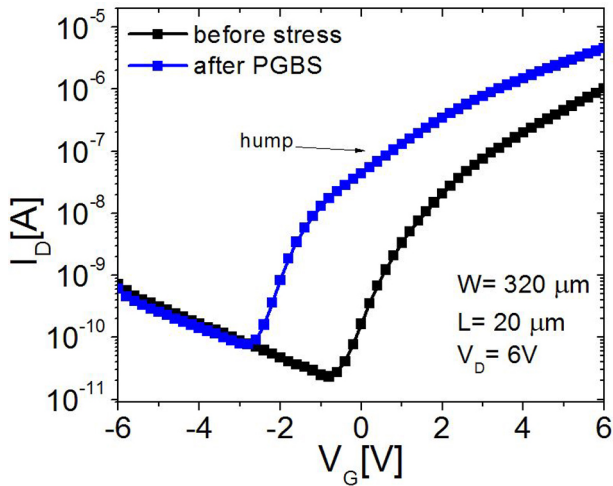
Fig. 5 Transfer characteristics of HIZO TFTs with PGBS and recovery after 5 min.

Trap density at the interface after PGBS was found to increase up to  $3.1 \times 10^{11} \text{ cm}^{-2}$  while mobility varies from  $6 \times 10^{-2}$  to  $1.3 \times 10^{-1} \text{ cm}^2/\text{V}\cdot\text{s}$ . Estimated  $V_T$  shifting ( $\Delta V_T$ ) was  $0.5 \text{ V}$ .

In Fig. 6a and 6b,  $V_G$  was swept from 6 to  $-6 \text{ V}$  and vice versa, respectively, after PGBS, where both presented a negative  $V_T$  shift and a "hump" appeared for the latter. This "hump" could be explained by when a negative  $V_G$  is applied, the density of states  $N$  at the back of the active layer is sufficiently high and the electron concentration near the back interface remains high enough to provide a current path in parallel to the TFT channel requiring more negative gate voltage to be applied to finally turn off the device, which gives rise to this hump<sup>[27]</sup>.



a)



b)

Fig. 6 Transfer characteristics of HIZO TFTs with PGBS with VG sweep: (a) VG=6 to -6 V and (b) VG=-6 to 6 V.

NGBS did not seem to affect the behavior of the devices in the linear regime, neither a  $V_T$  shift nor a hump was observed (Fig 7).

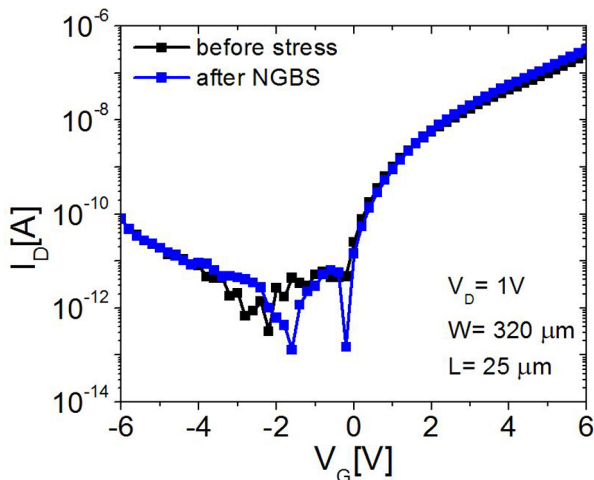
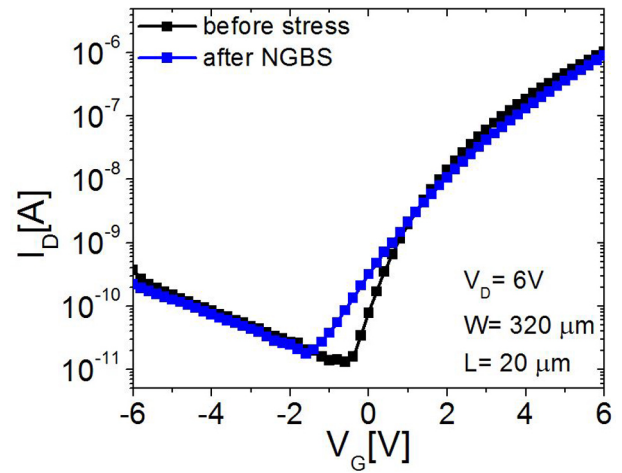
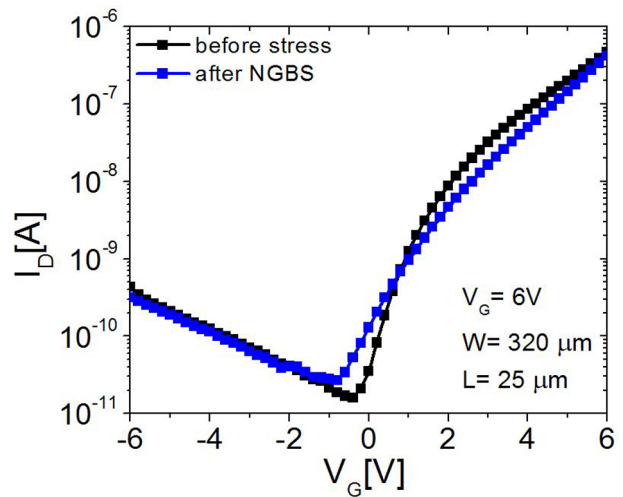


Fig. 7 Transfer characteristic of HIZO TFTs with NGBS in the linear regime.

In the transfer curves in saturation (Fig.8), the  $V_T$  shift is not observed, but shape of the transfer curve is slightly modified indicating the presence of interface traps. When NGBS is applied, the transistor channel is depleted of electrons at the channel/dielectric interface and no mobile negative charges are available for the charge trapping and tunneling process<sup>[7]</sup>. Despite oxide fixed charge centers are immobile, the deformation of the curve can be due to mobile ions that alter the centroid of the mobile ion distribution<sup>[28]</sup>.



a)



b)

Fig. 8 Transfer characteristics of HIZO TFTs with NGBS in saturation regime.

Figure 9 shows the hysteresis behavior of two HIZO TFTs with different L.  $V_H$  shift of  $V_G$  in hysteresis loops is commonly attributed to the polarization of the dielectric or to the interface trap density and/or bulk trap density<sup>[29]</sup>. Hysteresis loop here is quite small and since HfO<sub>2</sub> is a high-k dielectric, the shift is expected to be caused by the orientation of the dielectric dipoles when bias is applied.

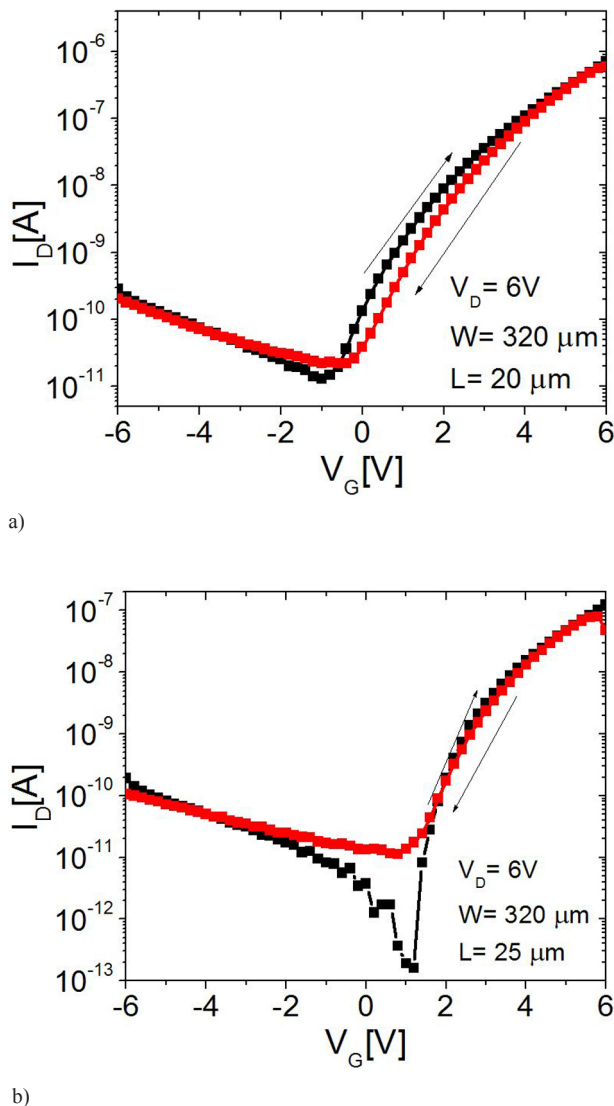


Fig. 8 Hysteresis characteristics of HIZO TFTs.

#### IV. CONCLUSION

The effects of gate-bias stress on the characteristics of HfO<sub>2</sub>/HIZO-TFTs, with both layers deposited by room temperature RF sputtering, were analyzed for the first time.

Devices show bias stress-induced instability as the  $V_T$  shifts toward negative values which be related to properties of the HfO<sub>2</sub> and/or its interface to the HIZO channel layer or to the reversible charge/discharge effect of the electrons in pre-existing high-k HfO<sub>2</sub> bulk traps. PGBS do not cause any degeneration, since stressed devices tend to recover after 5 mins. However, further work is required to a better understanding of the specific mechanisms involved. The charge/discharge effect can be reduced with a decrease in pre-existing high-k bulk traps and reducing the interlayer thickness.

Devices under NGBS showed a slight shift since the transistor channel is depleted of electrons at the channel/dielectric interface and no mobile charges are available for the charge trapping and tunneling process when a negative

bias is applied to the gate.

Hysteresis loop was small in spite of using a high-k dielectric. Despite a high parasitic resistance, due to the interlayer formed Al used as S-D contacts interlayer formed, the HIZO devices work at voltage lower than 6 V.

#### ACKNOWLEDGEMENTS

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