Boosting the MOSFETs Matching by Using Diamond Layout Style

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***Abstract*—This manuscript presents an experimental comparative study between the Metal-Oxide-Semiconductor (MOS) Silicon-On-Insulator (SOI) Field Effect Transistors, n-type, (nMOSFETs) matching, which are implemented with the hexagonal gate shape (Diamond) and standard rectangular ones. The main analog parameters and figures of merit of 360 devices are investigated. The results establish that the Diamond SOI MOSFETs with α angles equal to 90o can boost in more than in average -45.8% with a standard deviation of 20.1% the devices matching in comparison to those found with the typical rectangular SOI MOSFETs, concerning the same gate area and bias conditions. Consequently, the Diamond layout style is an alternative technique to reduce the nMOSFETs' mismatching, considering the analog SOI Complementary MOS (CMOS) integrated circuits (ICs) applications.**

***Index Terms*—** Devices Matching, SOI nMOSFET and analog SOI CMOS ICs.

I. Introduction

The electrical performance of analog Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs) is absolutely affected by the layouts of semiconductor devices (dimensions, geometric shape and how they are realized along the silicon wafer) [1-9]. Analog electrical performance of CMOS ICs may be also degraded when the devices dimensions are reduced due to the continued evolution of this manufacture process technologies [1-9]. The key analog building block used in these CMOS ICs is usually the operational transconductance amplifier (OTA), which is implemented with a differential circuit in its input stage [1-9]. The analog electrical performance of the differential circuit crucially depends on how identical or how matched are the devices that compose it, taking into account mainly their dimensions (aspect ratio, W/L, where W and L are respectively the channel width and length) and technological parameters, such as the gate oxide and silicon film thicknesses, and doping concentrations of the drain, channel and source regions, etc. [1-2]. Besides, the devices mismatching is straightforwardly correlated to the differences between their electrical behaviors, which they are implemented with the same geometries, dimensions, and also when they are operating in the same bias conditions, due to the CMOS ICs manufacturing processes variations [1-5].

Lately it was proposed an innovative layout technique to increase the electrical performance of Metal-Oxide-Semiconductor (MOS) Silicon-On-Insulator (SOI) Field Effect Transistors (MOSFETs) [10-13], without adding any extra cost to the CMOS ICs manufacturing processes. This happens because the Diamond MOSFETs have two additional effects entitled Longitudinal Corner Effect (LCE), which is responsible to boost the resultant longitudinal electric field along the channel length in relation to the one observed in the CSnM counterpart, regarding the same channel width, gate area (A_G), and bias conditions [10-13], and Parallel Association of MOSFETs with Different Channel Lengths Effect (PAMDLE) [10-13]. The hexagonal gate geometry (Diamond layout style) is an example of this layout approach [10-13]. In this circumstances, an experimental comparative study is significant to be done to explore the influence of the Diamond layout style (hexagonal gate shape) [10-13] in the n-type SOI MOSFETs (nMOSFETs) matching in comparison to the traditional rectangular layout style. Fig.1 shows a photograph of a n-type Diamond SOI MOSFET (DSnM).

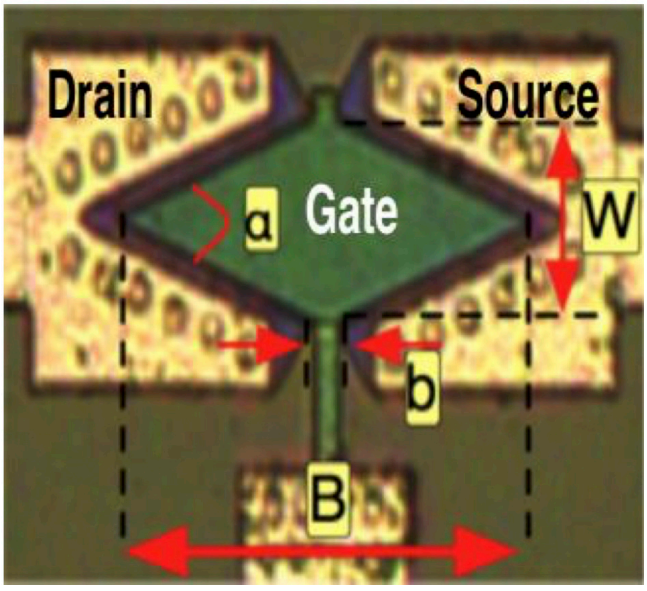

Fig. 22 Example of a picture of a DSnM.

In Fig. 1, b and B are the smallest and highest dimensions of the DSnM channel length, α is the angle between the metallurgical junctions composed by the drain-silicon film (channel)-source regions.

II. Devices Matching Quantification

The relative error (ε_r) in percentage of the devices matching between the DSnMs and typical rectangular SOI MOSFETs (CSnMs) counterparts, due to the variations of the CMOS ICs manufacturing process, is calculated by Equation (1) [14-15]. The ε_r states how much the DSnM can present a better (ε_r<0) or worse (ε_r >0) devices matching in comparison to their CSnM counterparts.

$$\varepsilon_r = \left(\frac{\left(\frac{s_{DSnM}}{x_{DSnM}}\right) - \left(\frac{s_{CSnM}}{x_{CSnM}}\right)}{\left(\frac{s_{CSnM}}{x_{CSnM}}\right)} \right) \cdot 100 \qquad (1)$$

where s_{DSnM} and s_{CSnM} and x_{DSnM} and x_{CSnM} are respectively the standard deviations, and the average values of a specific parameter of the DSnMs and CSnMs, considering a devices sample.

III. Device Description

The DSnM and their CSnM counterparts were manufactured by using 1 µm SOI CMOS manufacturing process from Université catholique de Louvain (ICTEAM/ELEN, UCL, Belgium). The Keithley 4200 was used to perform the electrical characterization of transistors. The key parameters of the fully depleted SOI nMOSFETs are as follows: the gate oxide thickness (t_{ox}), silicon film (t_{SI}), and buried oxide (t_{BOX}) are respectively 30 nm, and 80 nm, 390 nm, the doping concentrations of the drain/source and channel are equal to $4x10^{20}$ cm^{-3} and 6x1016 cm-3, respectively. The total data sample consists of 9 ICs. We studied 40 transistors per integrated circuit (IC), i.e. 20 pairs of SOI nMOSFETs with the same (A_G): 20 DSnM and 20 CSnM counterparts. From the 40 SOI nMOSFETs studied, there are 4 sets of 5 pairs of SOI nMOSFETs, which present the same W (12 µm, 24 µm, 30 µm, and 180 µm, respectively) with different values of the α angles (36.9˚, 53.1˚, 90˚, 126.9˚, and 143.1˚, respectively). These accounts a total of 360 transistors analyzed. The average threshold voltage (V_{TH}) of these devices is approximately 0.3 V. The average standard deviation of the V_{TH} of the analyzed samples for the DSnM devices, regarding the α angles equal to 36.9˚, 53.1˚, 90˚, 126.9˚ and 143.1˚ is equal to 0.17 V, respectively. The average standard deviation of the V_{TH} regarding the CSnM devices which are equivalent to the DSnM with α angles equal to 36.9˚, 53.1˚, 90˚, 126.9˚ and 143.1˚ is equal to 0.15V, respectively.

For comparison purposes, considering that the DSnMs and their CSnM counterparts present the same W, and AG, the CSnM L must present the average value of the smallest (b) and largest (B) values of the DSnM channel length, according to Equation (2).

$$L = \frac{B+b}{2} \qquad (2)$$

However, the SOI nMOSFET can be represented electrically as the parallel connection of N (integer number) SOI nMOSFETs with trapezoidal (rectangular, if N tends to infinite) gate shapes interconnected in parallel, with a channel width equal to W/N and different channel lengths (L_1, L_2, ..., L_N), which vary approximately from b a B. Fig. 2 shows how a Diamond SOI nMOSFET can be partitioned into N different SOI nMOSFETs with trapezoidal gate geometries.

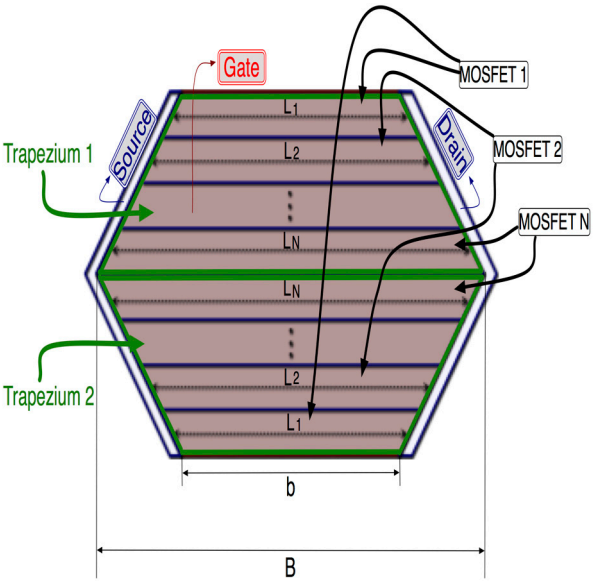

Fig. 2 Example of a DSnM partitioned in N SOI nMOSFETs with trapezoidal gate formats.

Fig. 3 illustrates the electrical representation of the Diamond SOI nMOSFET (Fig.3a), where W/L_{eff} is its effective aspect ratio and L_{eff} is its effective channel length; and its corresponding equivalent electrical circuit, considering that this device is subdivided in N SOI nMOSFETs with trapezoidal (rectangular, if N tends to infinite) gate shapes, which present the same channel widths (W/N) and different channel lengths (L_1, L_2, ..., L_N) (Fig.3b).

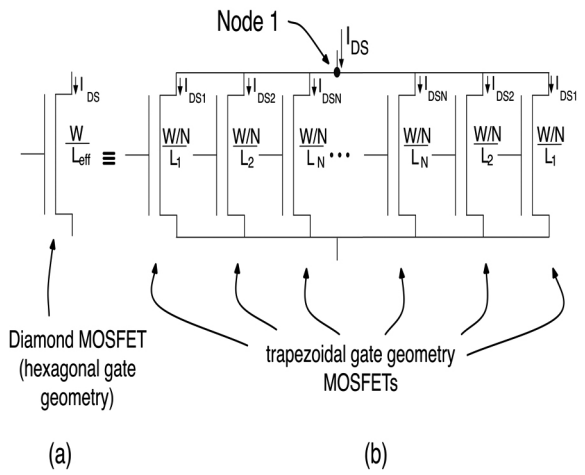

Fig. 3 Diamond SOI nMOSFET with its aspect ratio (W/L_{eff}) (Fig.3.a), and its equivalent electric circuit considering that this device can be partitioned in N SOI nMOSFETs of trapezoidal format, with channel width W/N and different lengths (L_1, L_2, ..., L_N) (Fig.3.b).

In Fig. 3, IDS is the drain current of the Diamond SOI nMOSFET, and I_{DS1}, I_{DS2} and I_{DSN}, are the I_{DS} of each SOI nMOSFET with trapezoidal gate geometry.

To obtain a simple first-order model of the DSnM L_{eff}, consider Fig. 4, which illustrates a Diamond SOI nMOSFET partitioned into 8 equal parts (N = 8).

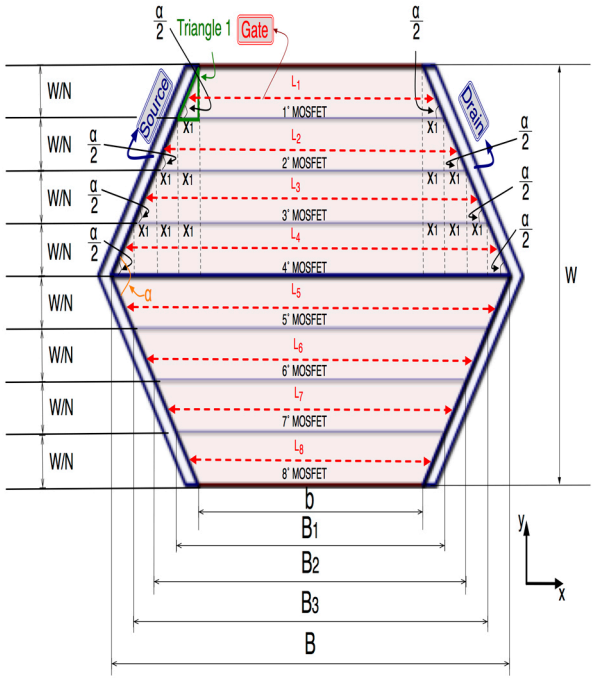

Fig. 4 Example of a Diamond SOI nMOSFET segmented into 8 equal parts, representing 8 SOI nMOSFETs with trapezoidal gate geometries, with different channel lengths and with the same channel width (W/N).

In Fig.4, L1, …, L8 are the average values of channel lengths of the 8 SOI nMOSFETs which are interconnected in parallel respectively, X1 is the projection in the x-direction of the base of the triangle 1, which belongs to the gate region of each one of the SOI nMOSFETs with trapezoidal shape, and b, B1, B2, B3 and B are the dimensions of the trapezoidal bases of SOI nMOSFETs that are connected in parallel.

By analyzing the equivalent electrical circuit of Fig. 3, the DSnM I_{DS} is given by the sum of the I_{DS} of each SOI nMOSFET with trapezoidal gate shape (Kirchhoff's Law of Nodes), according to Equation (3), considering N equal to 8.

$$I_{DS} = I_{DS1} + I_{DS2} + I_{DS3} + I_{DS4} + I_{DS5} + I_{DS6} + I_{DS7} + I_{DS8} \quad (3)$$

Thus, the Diamond SOI nMOSFET L_{eff} of the Diamond type considering 8 SOI nMOSFETs interconnected in parallel is given by Equation (4).

$$L_{eff} = \frac{8}{2\cdot\left[\frac{1}{b+\frac{W/8}{tg(\alpha/2)}} + \frac{1}{b+\frac{3\cdot W/8}{tg(\alpha/2)}} + \frac{1}{b+\frac{5\cdot W/8}{tg(\alpha/2)}} + \frac{1}{b+\frac{7\cdot W/8}{tg(\alpha/2)}}\right]} \quad (4)$$

Equation (4) can be generalized according to Equation (5), considering N as an even number and higher than 6.

$$L_{eff} = \frac{N}{\left[\frac{1}{b+\frac{W/N}{tg(\alpha/2)}} + \frac{1}{b+\frac{3\cdot W/N}{tg(\alpha/2)}} + \frac{1}{b+\frac{5\cdot W/N}{tg(\alpha/2)}} + \cdots + \frac{1}{b+\frac{(N-1)\cdot W/N}{tg(\alpha/2)}} + \frac{1}{b+\frac{(N-1)\cdot W/N}{tg(\alpha/2)}} + \cdots + \frac{1}{b+\frac{5\cdot W/N}{tg(\alpha/2)}} + \frac{1}{b+\frac{3\cdot W/N}{tg(\alpha/2)}} + \frac{1}{b+\frac{W/N}{tg(\alpha/2)}}\right]} \quad (5)$$

To understand numerically what Equation (5) means, Table I illustrates the values of the DSnM L_{eff}, considering different values of N.

Table I. Dimensions of DSnMs, their L_{eff} [Equation (5)] regarding different N, and the CSnM's Ls, which present the same A_G of DSnM counterparts.

Diamond SOI nMOSFETS dimensions (μm)				Effective lenghts of the Diamond SOI nMOSFETs considering the PAMDLE (μm)		CSnM L that presents the same Ag of a DSnM (μm)
W	b	N	α (*)	L_{eff}(N=10)	L_{eff}(N=50)	L=(b+B)/2
12	2	38	36.9*	13.4	12.3	20
12	2	26	53.1*	9.95	9.39	14
12	2	14	90*	6.33	6.17	8
12	2	8	126.9*	4.37	4.33	5
12	2	6	143.1*	3.66	3.64	4
24	4	76	36.9*	26.8	24.6	40
24	4	52	53.1*	19.9	18.8	28
24	4	28	90*	12.7	12.3	16
24	4	16	126.9*	8.74	8.66	10
24	4	12	143.1*	7.32	7.29	8
30	5	95	36.9*	33.5	30.8	50
30	5	65	53.1*	24.9	23.5	35
30	5	35	90*	15.8	15.4	20
30	5	20	126.9*	10.9	10.8	12.5
30	5	15	143.1*	9.15	9.11	10
180	30	570	36.9*	201.2	184.5	300
180	30	390	53.1*	149.2	140.9	210
180	30	210	90*	94.9	92.6	120
180	30	120	126.9*	65.5	64.9	75
180	30	90	143.1*	54.9	54.6	60

Observing the results obtained of the values of DSnM L_{eff}, we conclude that the hexagonal layout style for SOI nMOSFETs has the capacity to reduce its channel length (L) in relation to a standard SOI nMOSFET (rectangular gate geometry) counterpart, considering that they present the same W, and A_G. This effect is entitled "Parallel connection of MOSFETs with Different Channel Lengths Effect, PAMDLE") [13].

When N in Equation (5) tends to infinite, the DSnM L_{eff} is given by the Equation (6). Besides, the incorporation of the PAMDLE makes the first-order model of the DSnM L_{eff} more accurate with maximum error of 9.5% for micrometre scale [13].

$$L_{eff} = \frac{B-b}{ln\left(\frac{B}{b}\right)} \quad (6)$$

IV. Experimental Results

Table II presents the dimensional characteristics of four pairs of equivalent MOSFETs (rectangular and hexagonal gate geometries), regarding five different α angles. For instance, considering the first row of Table II, there are four equivalent MOSFETs with rectangular and hexagonal gate geometries with the same W (12, 24, 30 and 180 μm) and A_G (240, 960, 1500, and 54000 μm^2). Besides, we have four different L for the four CSMs (20, 40, 50, and 300 μm) and four b (2, 4, 5, and 30μm), B (38, 76, 95, and 570 μm) and L_{eff} (12.3, 24.6, 30.8, and 184.5μm) for the four DSM counterparts. As we study five different α angles, the total number of devices investigated were 40 per CMOS IC studied.

Table II. The dimensional characteristics of the devices used for this study.

CSnM and DSnM parameters								CSnM				DSnM											
W (μm)				A_G (μm^2)				L (μm)				α (°)	b (μm)			B (μm)				L_{eff} (μm)			
12	24	30	180	240	960	1500	54000	20	40	50	300	36.9	2	4	5	30	38	76	95	570	12.3	24.6	30.8	184.5
12	24	30	180	168	672	1050	3700	14	28	25	210	53.1	2	4	5	30	26	52	65	390	9.39	18.8	23.5	140.9
12	24	30	180	96	384	600	21600	8	16	20	120	90.0	2	4	5	30	14	28	35	210	6.17	12.3	15.4	92.6
12	24	30	180	60	240	375	13500	5	10	12.5	75	126.9	2	4	5	30	8	16	20	120	4.33	8.66	10.8	64.9
12	24	30	180	48	192	300	10800	4	8	10	60	143.1	2	4	5	30	6	12	15	90	3.64	7.29	9.11	54.6

Regarding Table II, placing the Diamond MOSFET layout over the Rectangular MOSFET one (overlap), it is possible to analyze if their total areas are similar, as illustrated in Fig. 5.

Fig. 5 Overlapping of the layouts of the Diamond and Rectangular MOSFETs in order to verify if their total die areas are similar.

Therefore, according to Fig. 5, it is possible to verify that the area of region 3 is basically the same as the sum of the area of regions 1 and 2. Therefore, one can conclude that their total die areas are practically the same. Additionally, it is also possible to affirm that the same behavior happens concerning region 6, that is, the sum of the areas of regions 4 and 5 are practically the same as the area of region 6.

By analyzing the IDS as a function of the drain voltage (V_{DS}) of 360 SOI nMOSFETs indicated in Table II, in the moderate inversion regime, the devices matching of DSnMs in relation to the CSnM counterparts, concerning the saturation drain current (I_{DSsat}) normalized as a function of the aspect ratio (AR) [$\varepsilon_{r\_IDSsat/(AR)}$], taking into account only the LCE effect (W/L_{eff}), and also considering the two effects (LCE and PAMDLE) working simultaneously (W/L), where L corresponds to the channel length of a standard (rectangular gate geometry) SOI nMOSFET, which presents the same W,

and A_G of a DSnM (real condition of operation), is presented in Fig. 6, regarding V_{GS} equal to 0.4 V. The method used to obtain the I_{DSsat} is described in the references [16-18].

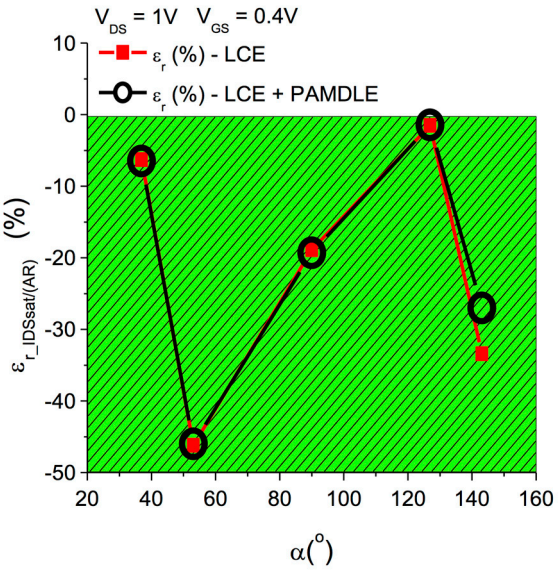

Fig. 6 The [$\varepsilon_{r\_IDSsat/(AR)}$] in relation to the α angles of DSnMs, regarding V_{DS} and VGS equal to 1 V and 0.4 V, respectively.

Based on Fig. 6, taking into account the I_{DSsat}/AR, we can see that the DSnMs, considering all α angles studied, are able to present better devices matching in relation to those found with the CSnM counterparts (-6.3% for the α equals to 36.9˚, -46.2% for the α equals to 53.1˚, -18.9% for the α equals to 90˚, -1.5% for the α equals to 126.9˚ and around -33.4% for the α equals to 143.1˚). This happens because the DSnMs always present higher I_{DSsat}/AR values than those found considering the CSnM counterparts, regarding the same W, AG, and bias conditions, as a result of the LCE and PAMDLE effects. Additionally, in this case, the devices matching related to the I_{DSsat}/AR, considering the AR with the presence of both effects (LCE and PAMDLE), which is the real condition of DSnM operation, is similar to that concerning only the LCE effect. This can be justified because both the average values and standard deviations depend on the AR values, which they are changing at the same time, and therefore, the relative error ($\varepsilon_{r\_IDSsat/AR}$) tends to present similar results.

Fig. 7 illustrates the ε_r of the maximum transconductance normalized by the aspect ratio [$\varepsilon_{r\_gmSAT/(AR)}$], considering the LCE and PAMDLE effects and only the LCE effect, of the DSnMs in relation to the CSnM counterparts as a function of the α angles of the DSnMs, regarding V_{GS} equal to 0.4V (saturation region). Therefore, these values correspond to the maximum values of the parameter gm when the MOSFETs are operating in the saturation region. The method used to get the gm_{SAT} is defined in the references [16-18].

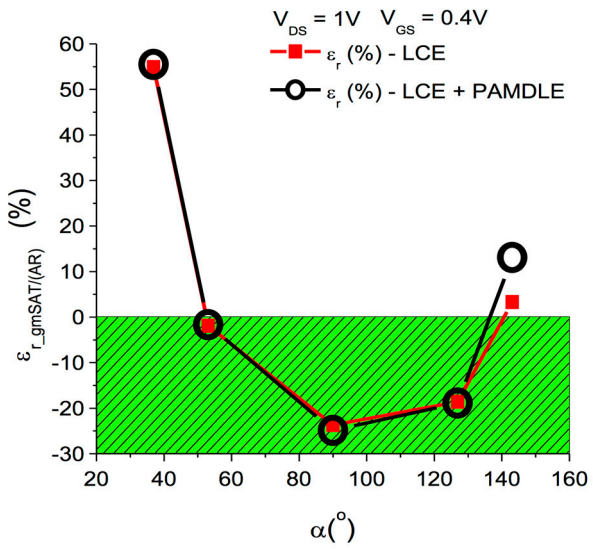

Fig. 7 The [$\varepsilon_{r\_gmSAT/(AR)}$], considering the LCE and PAMDLE effects and only the LCE effect, in relation to the α angles of DSnMs, regarding V_{DS} and V_{GS} equal to 1V and 0.4V, respectively.

By analyzing Fig. 7, we can see that the DSnMs with α angles equal to 90˚ and 126.9˚, respectively, are able to present better devices matching than those obtained with the CSnM counterparts (-23.7% for the α equals to 90˚ and -18.6% for the α equals to 126.1˚). This can be explained because the LCE and PAMDLE effects, which are responsible to boost the DSnMs' gm_{SAT}/AR in relation to those found in the CSnMs counterparts, and consequently the average value of the DSnMs' gm_{SAT}/AR is higher than the one observed of the CSnM counterparts, considering the Equation (5). Besides, for the α equal to 53.1o and 143.1˚, they present similar devices matching in comparison to their CSnM counterparts (-1.9% for the α equals to 53.1˚, and +3.3% for α equals to 143.1o). Regarding the DSnM with α equal to 53.1o, although they have greater gm_{SAT}/AR values than those found in the CSnM counterparts, a possible explanation for this effect is due to their geometric shapes (hexagonal) be pointed, and therefore these transistors tend to be more affected by CMOS ICs manufacturing processes variations. Considering the DSnMs with α equal to 143.1˚, this can be justified because the DSnMs tend to present an electrical behavior similar to those found in the CSnM counterparts, because the LCE and PAMDLE effects are not so intense and therefore their average values must be similar. Finally, the worst devices matching observed (around +54.9%) in relation to the CSnM counterparts, is related to the DSnMs with α angle equal to 36.9˚. This can be justified due to their gate geometries are very pointed, and consequently their gm_{SAT}/AR are strongly affected by the manufacturing processes variations (round corners, etc.) [3-5], as illustrated in Fig. 8, although they present higher gm_{SAT}/AR than those found in the CSnM counterparts, as a consequence of the LCE and PAMDLE effects.

Furthermore, the behavior of the devices matching related

to the DSnMs gm_{SAT}/AR in comparison to those presented with the CSnM counterparts, taking into account the LCE and PAMDLE effects together, and only considering the LCE effect, are the same presented to the DSnMs' I_{DSsat}/AR.

Fig. 8 illustrates the pointed region of the interface between the source and channel regions of the DSnM with an α angle equal to 36.9˚.

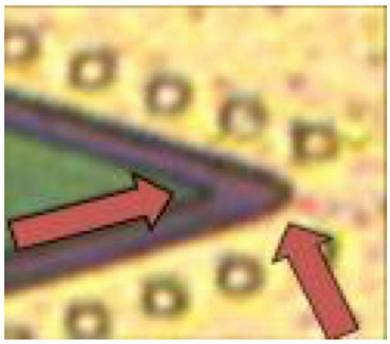

Fig. 8 Pointed region of the interface between the source and channel regions of the DSnM with an α angle equals to 36.9˚, which presents rounded corner and consequently can be strongly affected by the manufacturing process variations.

The ε_r of the unit voltage gain frequency [f_T=gm/(2πC$_L$, where C_L is the load capacitance adopted equal to 10 pF] of the DSnMs in relation to the one found with the CSnM counterparts [$\varepsilon_{r\_ft/(AR)}$] as a function of the α angles, considering VDS and VGS equal to 1 V, and 0.4 V respectively (Saturation region and moderate inversion regime), concerning both AR normalizations (LCE and PAMDLE effects working together, and considering only the LCE effect acting in the DSnMs) presents the same behavior than the one observed in the εr of the maximum transconductance normalized by the aspect ratio [$\varepsilon_{r\_gmSAT/(AR)}$]. This can be justified because f_T is directly proportional to gm [19].

Fig. 9 illustrates the ε_r of the ratio between the transconductance and drain current [$\varepsilon_{r\_gm/IDS}$] of the DSnMs in relation to those with the CSnM counterparts, considering LCE and PAMDLE effects working together and also considering only the LCE effect , as a function of the α angles, regarding V_{GS} equal to 0.4V (saturation region). The method applied to acquire the gm/IDS is described in the references [16-19].

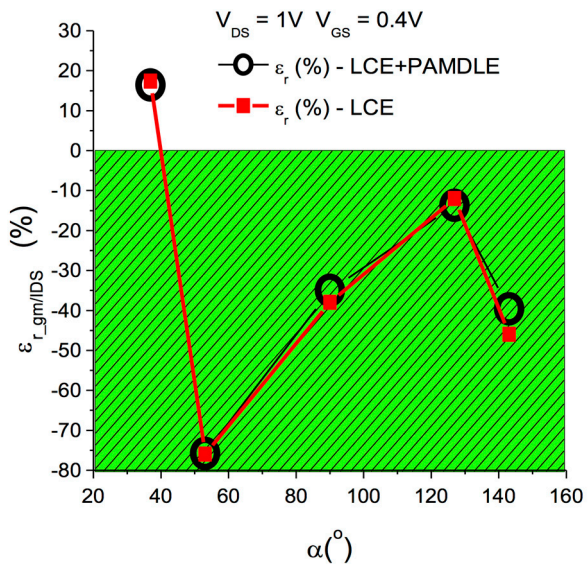

Fig. 9 The [$\varepsilon_{r\_gm/IDS}$] of the DSnMs in relation to the CSnM counterparts as a function of the α angles, regarding V_{GS} equal to 0.4V and V_{DS} equal to 1V (Saturation region and moderate inversion regime).

Analyzing Fig.9, we observe that the DSnM with the α angle equal to 53.1˚, 90˚, 126.9˚ and 143.1˚, respectively, are capable of presenting a better devices matching (-75.8% for the α equal to 53.1˚, -35.0% for the α equal to 90˚, -13.7% for the α equals to 126.9˚ and -39.6% for the α equals to 143.1˚) when compared to those obtained to their CSnM counterparts. This can be justified because the DSnMs present the LCE and PAMDLE effects, which are capable of boosting this figure of merit in relation to those observed with the CSnMs counterparts. Finally, to a α angle equal to 36.9˚, one can observe a very different behavior in comparison to the other α angles, that is, the DSnM present a worst matching between devices (+16.4%) in relation to those obtained to their CSnM counterparts. This can be justified due to the strong influence of the manufacturing process in the gate hexagonal geometries of the DSnMs (rounding corners, doping concentration variation, mobility variations of the charge mobile carriers in this region, etc.) [3-5]. In this case both gm and IDS depends on AR, consequently there are no differences between the relative errors taking into account the LCE and PAMDLE effects working together (real condition) and the εr that considers only the LCE effect.

Another important analog figure of merit is the Early voltage (V_{EA}), as the intrinsic voltage gain [A_V=(gm/I_{DS}).V_{EA}] of SOI nMOSFETs is directly proportional to the V_{EA} [19-20]. Fig. 10 presents the ε_r of the Early voltages [$\varepsilon_{r—VEA/(AR)}$] of the DSnMs in relation to the CSnM counterparts, taking into account the LCE and PAMDLE effects acting together and only considering the influence of the LCE effect [$\varepsilon_{r—VEA/(L)}$] as a function of the α angles, regarding V_{DS} equal to 1 V and V_{GS} of 0.4 V (Saturation region and moderate inversion regime). The method used to obtain the V_{EA} is explained in the references [16-19].

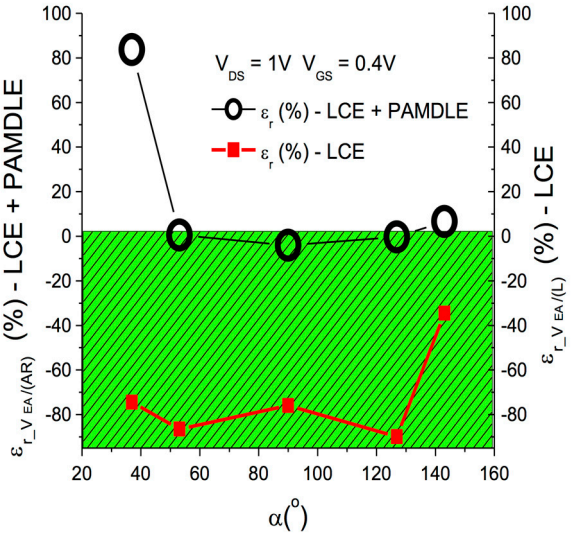

Fig. 10 The [$\varepsilon_{r\_VEA/(AR)}$] and [$\varepsilon_{r\_VEA/(L)}$] of the DSnM V_{EA} in relation to that found with the CSnM counterparts as a function of α angles, regarding V_{DS} and V_{GS} equal to 1V and 0.4V, respectively (Saturation region and moderate inversion regime).

By analyzing Fig.10, we can observe that the devices matching regarding the V_{EA}/AR of the DSnMs in relation to the one found with the CSnMs counterparts are regarding α angles equal to 53.1o (maximum relative error of +0.5%), 90˚ (-4.0%), 126.9˚ (-0.4%), and 143,1o (maximum relative error of +6.6%), respectively, as regarding the LCE and PAMDLE effects. This can be explained because as the relative error of DSnMs V_{EA}/(AR) increases (standard deviation increases and the average value reduces), and in the same time, the relative error of CSnMs V_{EA}/(AR) reduces (standard deviation reduces and the average value increases) as the α angle reduces. However, for the DSnM with α angle equal to 36.9o (+83.7%), the standard deviation of the V_{EA}/AR is very higher than the one found with the CSnM counterpart. Furthermore, we can observe that the devices matching regarding the V_{EA}/ L of the DSnMs in relation to the one found with the CSnMs counterparts are, regarding α angles equal to 36.9o (maximum relative error of -74.4%), 53.1o (-86.5%), 90˚ (-75.9%), 126.9˚ (-89.9%), and 143,1o (-34.5%), respectively, as regarding the LCE effects. This can be explained because V_{EA} is only dependent of L, and as the relative error of DSnMs V_{EA}/(L) decreases (standard deviation decreases and the average value increases), and in the same time, the relative error of CSnMs V_{EA}/(AR) reduces (standard deviation reduces and the average value increases) as the α angle reduces, due to mainly the LCE effect.

Fig. 11 illustrates the [$\varepsilon r_{\_AV/(AR)}$] of the DSnMs in relation to the CSnM counterparts as a function of the DSnM α angle, regarding V_{DS} equal to 1 V and V_{GS} equal to 0.4 V (Saturation region and moderate inversion regime) [17]. This figure shows the $\varepsilon r_{\_AV/(AR}$), which takes into account the LCE and PAMDLE effects working together (real condition) and also the $\varepsilon r_{\_AV/(L)}$ which considers only the LCE effect.

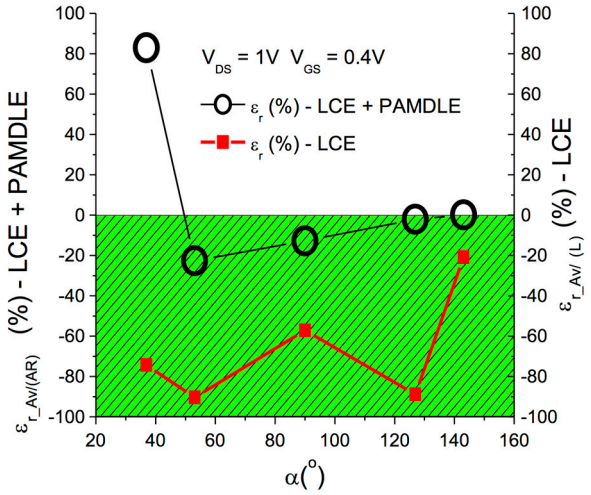

Fig. 11. The [$\varepsilon_{r\_AV/(AR)}$] and [$\varepsilon_{r\_VEA/(L)}$] in relation to the DSnM α angle, regarding V_{DS} and V_{GS} equal to 1V and 0.4V, respectively (Saturation region and moderate inversion regime).

Analyzing Fig.11, we observe that the devices matching of DSnMs with α angles equal to 53.1o, and 90o, respectively, taking into account the A_V/AR, is better (-22.6% for α of 53.1˚, and -12.8% for α of 90˚) than those observed with the CSnMs counterparts. However, the DSnMs with α angles equal to 126.9˚, and 143.1˚, respectively, present practically the same devices matching for the A_V/(AR) than those verified with the CSnM counterparts (-2.13 for α of 126.9˚, and +0.1% for α of 143.1˚). This happens due to the influence of the both devices matching taking into account the gm/IDS and V_{EA}/(AR), respectively, according the previous results indicated in Figs. 9 and 10, respectively. Besides, we observe that the devices matching of DSnMs with α angles equal to 36.9 o, 53.1o, 90o, 126.9 o and 143.1 o respectively, taking into account the A_V/L, is better (-74.3% for α of 36.9˚, -90.4% for α of 53.1˚, -57.2% for α of 90.0˚, -88.8% for α of 126.9˚ and -20.9% for α of 143.1˚) than those observed with the CSnMs counterparts. This can be explained due to the influence of the both devices matching taking into account the gm/I_{DS} and V_{EA}/(L), respectively, according the previous results indicated in Figs. 9 and 10, respectively.

Fig. 12 illustrates the ε_r of the on-state drain current (I_{on}) normalized by the aspect ratio (I_{on}/AR) as a function of the α angles of the DSnM, regarding V_{GS} and V_{DS} equal to 0.4 V and 50 mV, respectively. This figure shows both AR normalizations (LCE and PAMDLE effects working together, and considering only the LCE effect acting in the DSnMs) of the DSnMs in relation to the one found with the CSnM counterparts [$\varepsilon_{r\_Ion/(AR)}$]. The method utilized to get the I_{on} is described in the references [16-18].

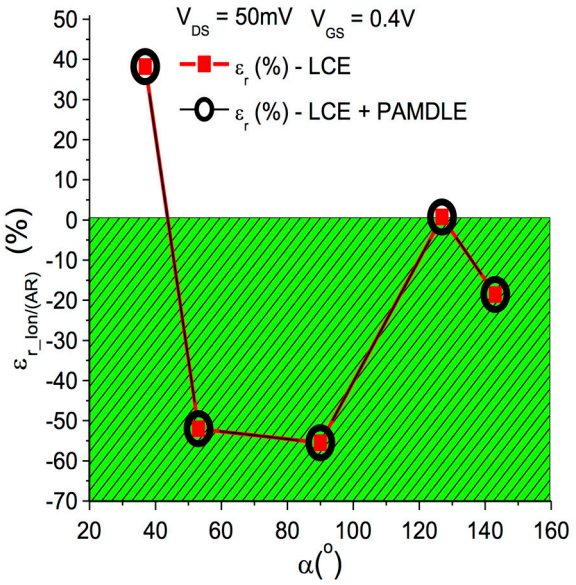

Fig. 12 The [$\varepsilon_{r\_Ion/(AR)}$] in relation to the DSnM α angle, regarding V_{GS} and V_{DS} equal to 0.4 V and 50 mV, respectively.

From Fig.12, we observe that the DSnM with α equals to 53.1˚, 90˚ and 143.1˚ are capable of presenting a better devices matching as compared to the one found with the CSnM counterparts (-52.0% for the α equals to 53.1˚, -55.5% for the α equals to 90˚ and -18.6% for the α equals to 143.1˚). For the α equals to 126.9˚, it is possible to verify that there is a similar matching between devices behavior in relation to its CSnM counterparts (around +0.7%). Finally, for the α equals to 36.9˚ it is possible to affirm that the DSnM have a worst matching between devices when compared to its CSnM counterparts for an α equals to 36.9˚ (around +38.2%). This behavior of the devices matching taking into account of ION/AR is the same of the I_{DSsat}/AR, as reported earlier.

Fig.13 illustrates the εr of the on-state resistance (R_{on}) normalized in relation to the inverse of the AR [$\varepsilon_{r\_Ron/(1/AR)}$] of the DSnMs in relation to the CSnM counterparts, for both 1/AR normalizations, as a function of the α angles, regarding VGS equal to 0.4 V. The technique used to achieve the R_{on} is described in the references [16-18].

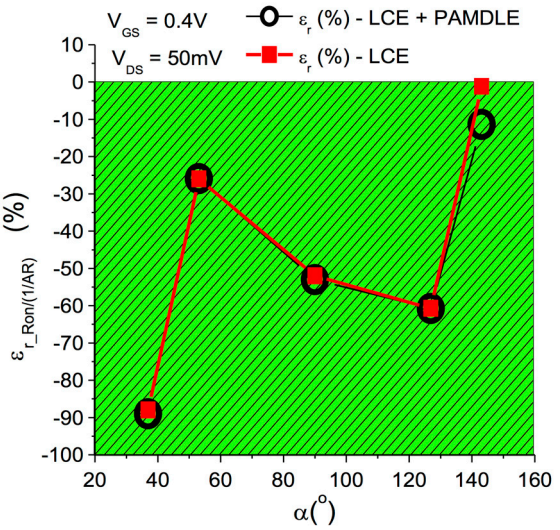

Fig. 13 The [$\varepsilon_{r\_RDSon/(1/AR)}$] in relation to the DSnM α angles, regarding VGS equal to 0.4 V, respectively.

By analyzing Fig.13, it is possible to observe that the DSnM with all the α angles are capable of producing a better matching between devices when compared to those found with the CSnM counterparts (-89% for the α equals to 36.9˚, -25.9% for the α equals to 53.1˚, -53% for the α equals to 90˚, -60.8% for the α equals to 126.9˚ and -11.36% for the α equals to 143.1˚). This occurs due to LCE and PAMDLE effects in the DSnMs. Furthermore, in this case, the devices matching related to the R_{on}/(1/AR), considering the AR with the presence of both effects (LCE and PAMDLE), which is the real condition of DSnM operation, is similar to that concerning only the LCE effect. This happens due to both the average values and standard deviations depend on the AR values, which they are changing at the same time, and therefore, the relative error [$\varepsilon_{r\_IDSsat/(AR)}$] tends to have similar values.

V. General Comparative Table of the Studied Electrical Parameters and Figures of Merit

Table III presents the relative errors of the devices matching, regarding all electrical parameters and the figures of merit of the DSnMs in relation to their CSnMs counterparts studied on this work, taking into account different AR normalizations (LCE and the PAMDLE effects, and only considering the LCE effect).

Table III. General comparative Table of the devices matching of the DSnMs in relation to those obtained with the CSnM counterparts, regarding the different AR normalizations (LCE and the PAMDLE effects and only considering the LCE effect).

ε_r (%) - LCE + PAMDLE					
α (°)	36.9	53.1	90.0	126.9	143.1
I_{DSsat}/AR	-6.5	-46.0	-19.3	-1.4	-27.0
gm_{SAT}/AR	+55.5	-1.7	-24.9	-18.9	+13.1
gm/I_{DS}	+16.4	-75.8	-35.0	-13.7	-39.6
V_{EA}/AR	+83.7	+0.5	-4.0	-0.36	+6.6
A_V/AR	+82.9	-22.6	-12.8	-2.1	+0.1
I_{on}/AR	+38.2	-52.0	-55.5	+0.7	-18.6
R_{on}/(1/AR)	-89.0	-25.9	-53.0	-60.8	-11.4
Average Value	25.89	-31.93	-29.21	-13.79	-10.97
Standard Deviation	60.50	27.73	19.63	22.05	18.91
ε_r (%) - LCE					
α (°)	36.9	53.1	90.0	126.9	143.1
I_{DSsat}/AR	-6.3	-46.2	-18.9	-1.5	-33.4
gm_{SAT}/AR	+54.9	-1.9	-23.7	-18.6	+3.3
gm/I_{DS}	+17.4	-76.0	-38.0	-12.0	-46.0
V_{EA}/L	-74.4	-86.5	-75.9	-89.9	-34.5
A_V/L	-74.3	-90.4	-57.2	-88.8	-20.9
I_{on}/AR	+38.0	-52.2	-55.1	+2.6	-23.3
R_{on}/(1/AR)	-88.0	-26.0	-52.0	-60.7	-1.1
Average Value	-41.00	-54.17	-45.83	-38.41	-22.27
Standard Deviation	54.49	32.73	20.14	40.46	17.99

Based on Table III, we conclude that the DSnM with α equal to 90 □ can always produce the best devices matching devices (in average -45.8% with a standard deviation of 20.1%), as compared to those obtained with the CSnM counterparts, for all main electrical parameters and figures of merit considered in this study. Therefore, Diamond layout style can be considered an alternative layout technique to boost the accuracy of the analog and digital SOI CMOS ICs applications.

VI. Conclusions

This study performed an experimental comparative study of the devices matching among the DSnMs and the CSnM counterparts, regarding the same W, AG and bias conditions. The results demonstrated that the DSnM with α angles equal to 90o are capable of boosting in more than 45% in average, with a standard deviation of 20.1%, the devices matching in comparison to those observed with the CSnM counterparts.

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