Advantageous Sampling of Correlated Current Signals to Supress Fixed-Pattern Noise in CMOS Imagers

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Abstract — **The Active Pixel Sensor (APS) has been a vastly used integrated circuit topology in CMOS imagers. Mismatch of physical parameters among pixels, caused by process variations, introduces Fixed-Pattern Noise (FPN) at the array output. Correlated Double Sampling (CDS) in voltage mode is a commonly used method to suppress the offset caused FPN. However, it increases the complexity as well as the demanded silicon area of either the pixel or the external circuitry, besides having its signal swing restricted by the supply voltage. An alternative CDS circuit operating in current mode to reduce FPN is presented in this paper. The correlated current signals are sampled and subtracted using a simpler circuitry, leading to a more efficient relation of FPN reduction for the required silicon area. Furthermore, this technique does not change the APS topology or basic operation cycle. A simulated and tested CDS alternative is presented, and a simulated further improved version is proposed. Simulation and experiments showed a 40% FPN reduction with the fabricated CDS, whereas the improved simulated version ensures 90% FPN reduction.**

Keywords — Image Sensor, APS, FPN, CDS, Mismatch.

I. Introduction

CMOS based image sensors have numerous advantages, such as being cost effective in mass production, featuring low power consumption, large integration level and random access to pixels in the array, besides low operational voltage. Furthermore, they are sensitive to both visible and near-infrared spectral ranges, making them versatile to several new applications and technology demands [1].

The preferred choice for CMOS image sensor topology nowadays is the Active Pixel Sensor (APS). However, it introduces issues like the Fixed Pattern Noise (FPN), which is defined as the pixel-to-pixel output variation for flat-field illumination across the image plane. During the fabrication process, unavoidable transistor and photodiode parameter mismatches arise, such as threshold voltage and quantum efficiency. The pixels, therefore, render signals that deviate from the expected reference values. Design techniques such as Correlated Double Sampling (CDS) operating in voltage mode are used to attenuate this noise [2]-[7]. This technique uses a circuit that samples a voltage output at two specific instants, one during the fixed reset level and another at the measured signal level. Since FPN is mostly an offset and present in both, it can be cancelled by means of differential read-out [7].

This work proposes a new CDS circuit approach, which operates in current mode. As in the voltage-mode version, the APS output is sampled twice, but now, the current subtraction operation can be performed with a fairly simpler circuit than that of a voltage-mode CDS, reducing also the necessary silicon area and being compliant with the lower supply voltages in smaller technology nodes.

II. FPN Simulation in APS

The noise present in CMOS image sensors is typically divided into two categories: Temporal noise and spatial noise. The temporal noise is what we can call real noise, since it behaves randomly through the time and changes from frame to frame. One way to reduce it is by averaging a frame sequence [8]. The spatial noise is effectively a pattern noise, which does not change significantly from frame to frame and cannot be reduced by means of consecutive frames. The pattern noise is divided into two components: Fixed-Pattern Noise (FPN) and Photo-Response Non-Uniformity (PRNU) [11]. The FPN is the pattern-noise component, which does not depend on the light and is generally measured without incidence of light, although it is also present under incident light. In relation to the pixel output response, the FPN can be observed as a gain factor and offset variation. The FPN caused by gain factor variations is difficult to correct and there are no widely used methods for reducing it. Unlike the gain factor FPN, the offset FPN – i.e., the FPN caused by offset variations – can be significantly reduced by the implementation of a CDS [12].

Although there are other FPN sources, the transistor mismatch is the main cause discussed in recent reports [13]-[19]. The mismatch affects electrical parameters of the transistor, which in turn differ between two identically drawn devices; consequently, the operating point and other circuit characteristics differ from their desired values [14]. Some possible reasons for the systematic component are non-uniform thermal distribution during the fabrication process, lens aberration during the photolithographic process, foreign material contaminations during the fabrication, dimension variations of the photo-sensitive region, variations in the doping concentrations and variations in the oxide thickness [8].

Among different pixel architectures, the APS has become the preferred choice of designers due to its simplicity and functionality [4]. Architecture alternatives in APS-circuit topologies are discussed in the literature like reported by L. C. Costa et al. and P. F. L. Retes et al. [9][10]. Advantages and disadvantages of each APS variation and its applications is not the focus of this work, but the FPN problem is common to all of them. Here a variation of a APS on the Fig.

1 is chosen for analysis of the FPN caused by fabrication parameters variation in the transistors T_{RESET}, T_{BUFFER} and T_{LOAD}. The basic operation of an active pixel depends on the reset signal, which will charge the photodiode intrinsic capacitance when it turned on. When the transistor reset is turned off, the integration period starts, which consists of the I_{ph} discharging the intrinsic capacitance of the photodiode [8]. In the specialized literature [14]–[19] transistor mismatch is usually characterized by providing the standard deviation of the mismatch in a set of transistor electrical parameters such as the threshold voltage V_{T0}, the current gain factor β, gate oxide capacitance density, transistor width, transistor length, mobility degradation parameter, and the bulk threshold parameter. Often it is possible to simulate properly the precision limits that can be achieved by a certain circuit topology in a given fabrication process because VLSI circuit manufacturers provide transistor mismatch information. Regarding the technology with which this work was developed, the factory provides information on the standard deviation of a normal distribution of the parameters V_{T0} and β of transistors build directly side by side. The circuitry was implemented in a standard 350 nm CMOS technology. Electrical circuit simulations using HSPICE have been performed using the Bsim3v3 MOSFET Model where only the parameter V_{T0} can be directly modified to simulate FPN noise in the APS on the Fig. 1.

The following Pelgrom model describes the dependency of parameter V_{T0} standard deviation on their active channel area (*W.L*).

$$\sigma(V_{T0}) = \frac{9.5\ mV.\mu m}{\sqrt{W.L}}(\text{NMOS}) \quad (1)$$

$$\sigma(V_{T0}) = \frac{14.5\ mV.\mu m}{\sqrt{W.L}}(\text{PMOS}) \quad (2)$$

Considering (1) and (2) and the dimensions of the transistors T_{RESET}, T_{BUFFER} and T_{LOAD}, Fig. 1, the mean (μ) and standard deviation (σ) of the distribution are calculated for the parameter V_{T0} of the transistors. This result and the Monte Carlo simulation specification are shown in table I.

For the FPN simulation in the APS, a current source, Fig. 1, simulates the photodiode photo-current of I_{ph}=3.5 *nA*. This is the photocurrent value at the middle of the dynamic range corresponding to the APS output sensibility peak. The Tx analogue switch is always turned on and is not going to be part of the FPN analysis since it explores another functionality which is not covered in this work. Monte Carlo simulations of the APS were performed with 500 passes to verify the total FPN caused at the APS output due to the variations combined in the parameter V_{T0} of the T_{RESET}, T_{BUFFER} and T_{LOAD} APS transistors.

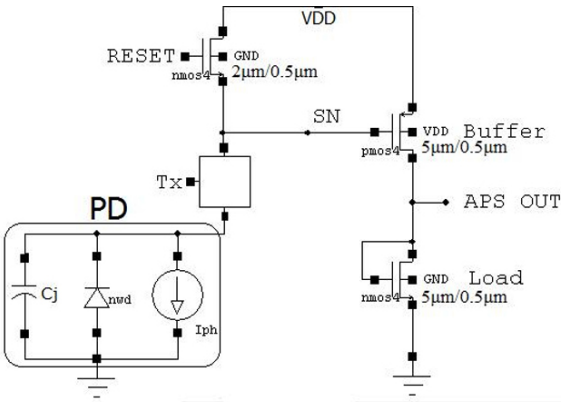

Fig.1 Implement APS topology.

Table I: Monte Carlo simulation specification

T_{RESET}	V_{T0} distribution	μ = 498 mV	σ = 9.50 mV
T_{BUFFER}	V_{T0} distribution	μ = −692 mV	σ = 9.17 mV
T_{LOAD}	V_{T0} distribution	μ = 498 mV	σ = 6.01 mV

The Fig. 2 shows the APS_{OUT} response curves to the 500 steps of the Monte Carlo simulation to a photodiode photo-current of I_{ph}=3.5 *nA* with variation of the parameter V_{T0} showed in the table I. The FPN reduction method proposed in this article stores the offset value at the end of the reset time to do the subtraction that removes this offset value during the integration time. Then it is important to characterise this APS output value variation immediately before the integration time. The statistical analysis of the 500 values has shown a normal distribution, which can be defined through its mean (μ) and standard deviation (σ).

The Fig. 3 shows seven APS response curves – the mean and 1, 2 and 3 standard deviations. The table II shows the mean (μ) and standard deviations (σ) of APS_{OUT} in the 5ms time, in the second column shows the standard deviations relative to the total APS_{OUT} signal swing, and in the third column the respective APS_{OUT} value at the end of τ_{RESET}. The FPN presented in the table II quantifies a realistic variation expected for a standard CMOS fabrication process.

Table II: Deviation results from Monte Carlo simulation

	Mean Deviation (mV)	Mean Deviation (%)	APS_{OUT}
Mean (μ)	0	0	589.7 mV
−σ	-14.7 mV	-1.16 %	575.0 mV
+σ	14.7 mV	1.16 %	604.5 mV
−2σ	-29.5 mV	-2.32 %	560.2 mV
+2σ	29.5 mV	2.32 %	619.2 mV
−3σ	-44.2 mV	-3.48 %	545.5 mV
+3σ	44.2 mV	3.48 %	634.0 mV

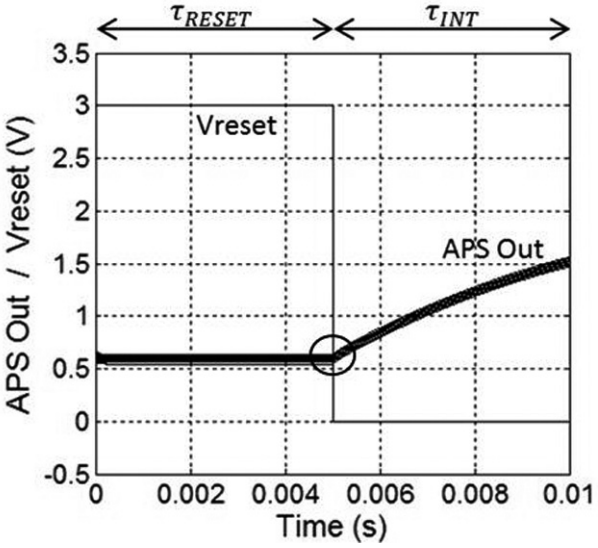

Fig.2 Monte Carlo simulation of APS_{OUT} showing 500 results.

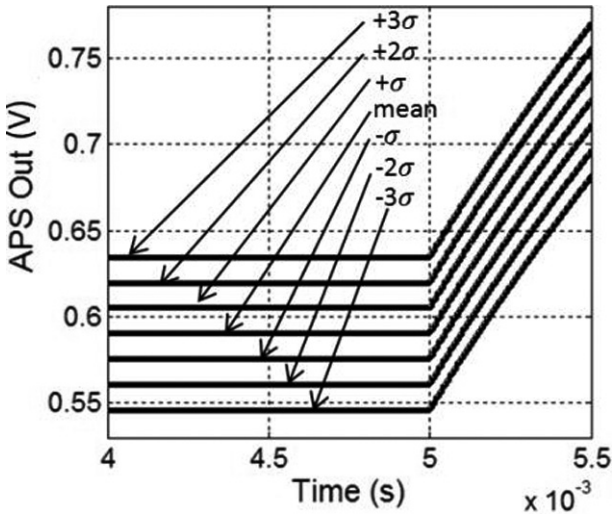

Fig.3 APS_{OUT} curve relative to the mean and 1, 2 and 3 standard deviations.

III. The CDS Circuit

Correlated double sampling (CDS) is a widely accepted technique aimed at reducing FPN noise. The CDS operation consists of storing an offset signal during the reset time and subtracting it during the subsequent integration time [15]. This operation virtually eliminates FPN at the output of a circuit like the APS, since this noise is mainly composed by offsets. Most of the reported CDS designs, however, include these on-chip image-processing functionalities at the expense of silicon area or increasing the complexity of the control signals, changing the basic operation cycle with additional read-out steps. This can limit the maximum spatial resolution achievable and the pixel matrix read-out speed. A common CDS design operating in linear (integrating) mode incorporates two sample-and-hold circuits and an operational amplifier using a correlated double sampling method to subtract the fixed pattern noise in voltage mode.

The CDS technique proposed in this work accomplishes this operation in current mode, which requires a simpler circuit for the subtraction operation reducing the necessary silicon area. Furthermore, no extra step is needed in the APS operation cycle, maintaining the read-out speed and the control signal complexity unaltered.

The CDS circuit on the Fig. 4 is shared between various pixels of a same array and, at each instant, one APS output signal is connected to the CDS_IN. During the τ_{RESET} period of the APS, Fig. 2, the analogue switch 2 is turned on and the APS output voltage level, containing different offsets, is transduced into a I_2 current. Note that the current I_2 is mirrored to the Out Node. At the end of the τ_{RESET} period, the switch 2 is turned off in order to store the τ_{RESET} information as a current, and the switch 1 is turned on to transform the APS voltage signal from the integration time τ_{INT}, Fig. 2, into a I_1 current, Fig 4. Applying the Kirchhoff's law on the Out Node, it results in (3) in which the subtraction operation is done during the τ_{INT}.

$$I_{out} = I_{pol} + (I_2 - I_1) \tag{3}$$

The current I_{pol} is a fixed current source and since I_1=I_2 at the τ_{RESET} period, $I_{out} \approx I_{pol}$ at the beginning of the integration time τ_{INT}. Along with the increase of I_1, I_{out} is gradually reduced and can reach a minimum of zero current. The Fig. 5–7 show the APS output waveforms and the respective currents I_1 and I_{out} simulating a photocurrent I_{ph} input, Fig. 1, of 100 pA, 1 nA, 2 nA and 3 nA. These photocurrent values are chosen as examples for the understanding of the CDS circuit and this behaviour shown in the curves is kept for other photocurrent values.

In the integrator circuit, Fig. 8, the CDS output current I_{out} is mirrored on a current mirror and integrated in an output capacitor. Note that the lower the APS output signal is, the lower is the current I_1 and the higher is the CDS output current I_{out}. So, the V_{OUT} voltage integrated in the integrator capacitor and read at the end of the integration time τ_{INT} is directly proportional to the input photo-generated current I_{ph}. The Fig. 9 illustrates this process for Iph = 100 pA; 1 nA; 2 nA; 3 nA. Characteristics of the Pixel read-out are listed in table III.

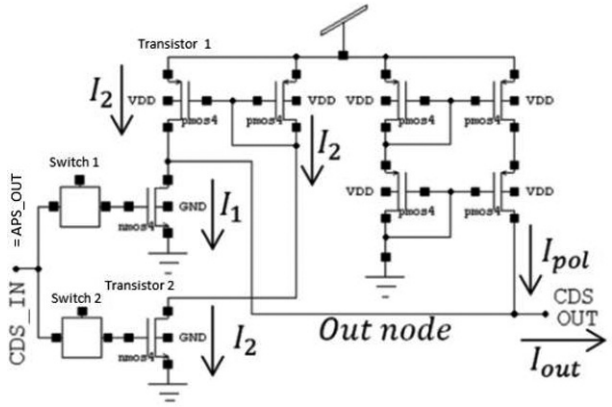

Fig.4 CDS circuit in current mode.

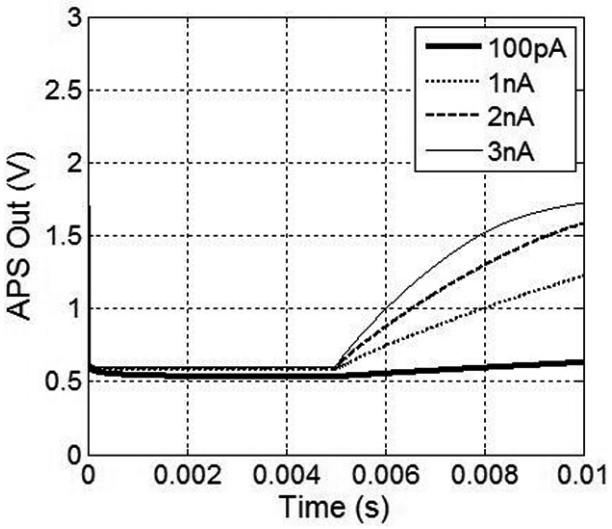

Fig.5 APS_{OUT} signal for photocurrent I_{ph} input of 100 pA, 1 nA, 2 nA and 3 nA.

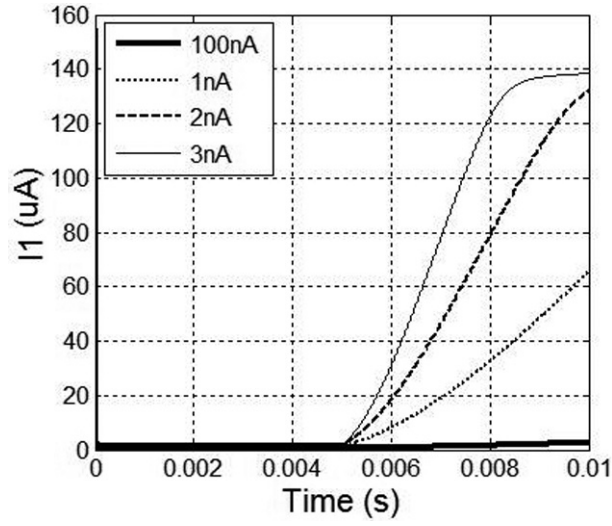

Fig.6 I_1 current signal for photocurrent I_{ph} input of 100 pA, 1 nA, 2 nA and 3 nA.

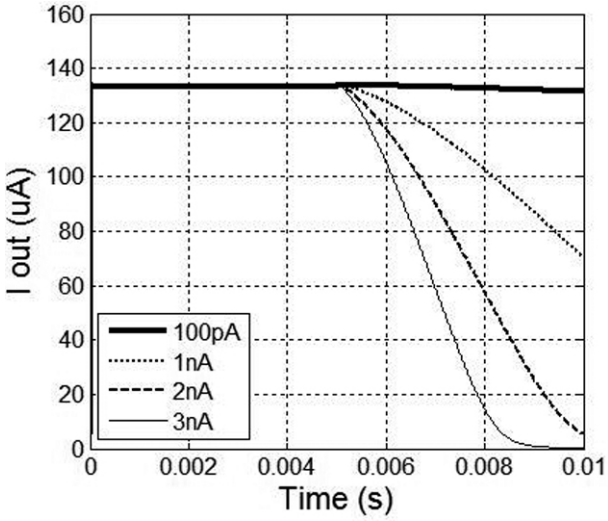

Fig.7 I_{OUT} current signal for photocurrent I_{ph} input of 100 pA, 1 nA, 2 nA and 3 nA.

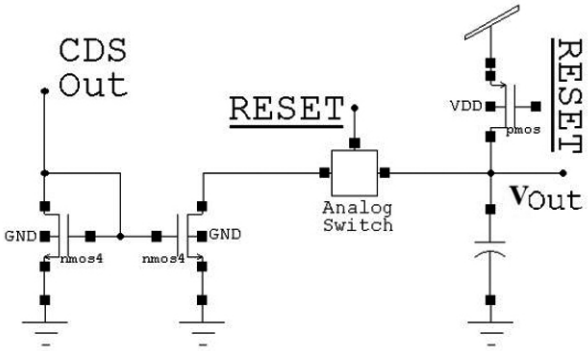

Fig.8 Current integrator circuit.

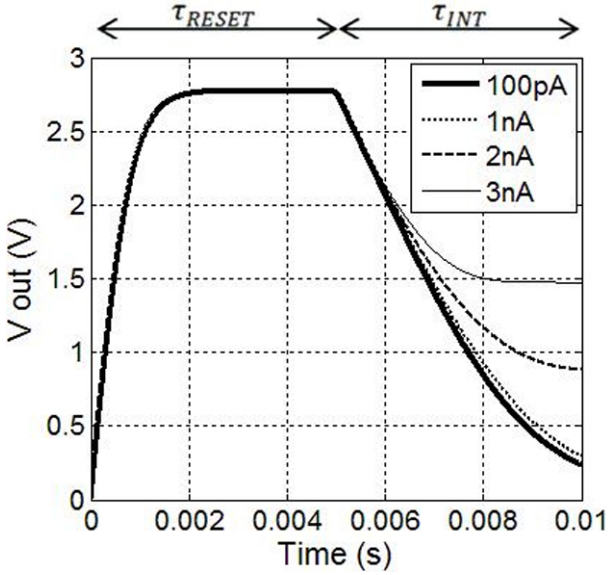

Fig.9 V_{OUT} signal.

Table III: Characteristics of the Pixel Read-Out

Technology	0.35 µm 2P4M CMOS
Supply Voltage "V_{DD}"	3.0 V
Reset Time "T_{RESET}"	5 ms
Integration Time "T_{INT}"	5 ms
Photodiode Size	85 µm X 85 µm
APS Size	25 µm X 25 µm
Fill Factor	78%
Dynamic Range	500 pA – 165 nA
Dynamic Range	50 dB
Signal Excursion	2.52 V

IV. Reducing Fixed Pattern Noise

In order to simulate a FPN noise, a variation in the parameter V_{T0} of the transistors T_{RESET}, T_{BUFFER} and T_{LOAD} is applied according to table I. The Monte Carlo simulation shows the expected APS output variation in the Fig. 2. The seven APS response curves in relation to the mean and variation of 1, 2 and 3 standard deviations, Fig. 3, are simulated to evaluate the FPN reduction at the response V_{OUT} of the complete circuit formed by the APS, the CDS and the integrator. The seven curves are generated at the APS output through the voltage source FD, Fig. 10. This type of simulation was chosen to make the simulations compatible with the experimental tests.

To compare the CDS performance, two simulations are performed with these seven curves – one using the CDS circuit and the other one bypassing it. The FPN noise is translated into an offset variation on the APS_{OUT} signal. The offset information is stored within the current I_2, performing a subtraction in the CDS circuit during the τ_{INT}. So as to bypass the CDS operation, it is necessary to keep the current I_2 null during the whole operation cycle. To eliminate the current I_2 in the simulation, the GND shall be connected to the transistor 2 gate in the CDS circuit, Fig. 4. Since this procedure is not performable in the subsequent experimental tests, another method is accomplished to cancel the current I_2. During 2.5 ms within the reset time τ_{RESET}, the voltage source FD is adjusted to the maximal applicable voltage, 3 V, letting the APS output to its lowest possible voltage value. Within this interval, the switch_2 is turned on to cancel the current I_2. The Fig. 11 displays control signals to perform this procedure and the seven V_{FD} waveforms to generate the outputs of the APS from the Fig. 3. Aiming to evaluate whether this method for bypassing the CDS circuit is satisfactory, a comparative simulation applying GND at the transistor 2, in Fig. 4, gate is performed and shows the same results, validating the adopted procedure. The switch_1 signal is continuously kept in V_{DD} for the purposes of this work. For the simulation using the CDS function, the signal P2 becomes the same signal as the RESET. This way, the offset information in APS_{OUT} is stored within the current I_2 and maintained during the τ_{INT}.

The Fig. 12: a) shows the response V_{OUT} concerning to the seven output curves of the APS depicted on the Fig. 3, with CDS actuation; b) the same without the CDS actuation for FPN reduction. The analysis on the Table IV shows the V_{OUT} values and the FPN reduction for each deviation associated to the deviation distribution observed at the APS output for the Monte Carlo simulations.

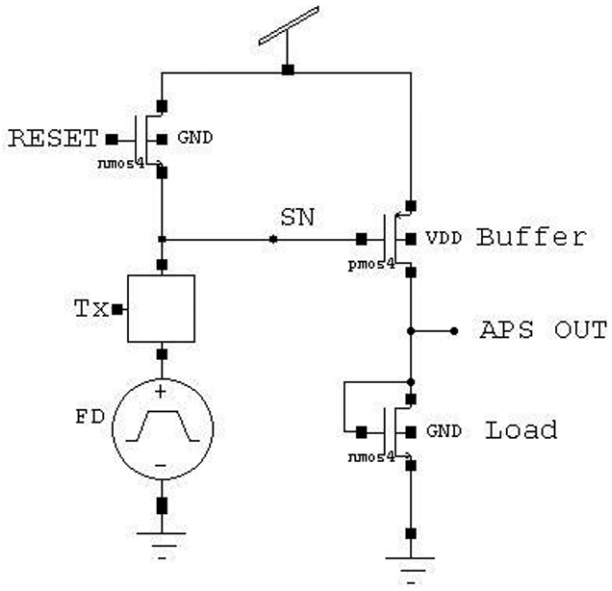

Fig.10 Simulated APS circuit.

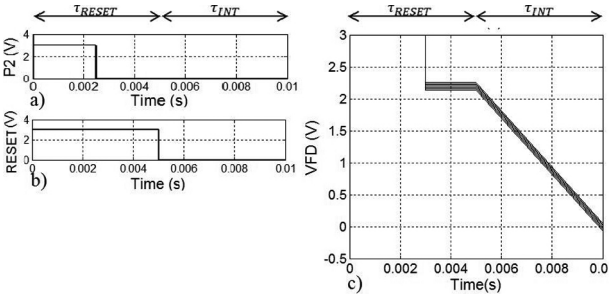

Fig.11 a) *P2* signal b) RESET signal c) V_{FD} signal..

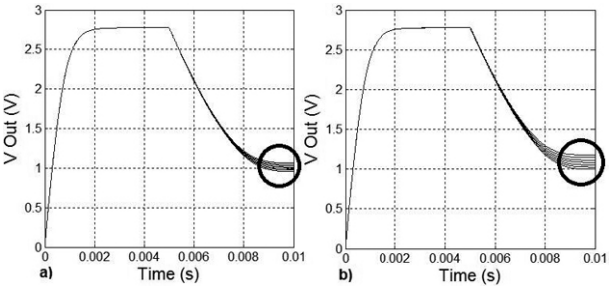

Fig.12 VOUT signal: a) with CDS operation, b) without CDS operation.

Table IV: Simulation results for the FPN reduction

	With CDS		Without CDS		FPN Reduction
	Mean Deviation	V_{out}	Mean Deviation	V_{out}	
Mean	0	1.010 V	0	1.083V	-
−σ	-18 mV	0.992 V	-31 mV	1.052V	42 %
+σ	17 mV	1.027 V	29 mV	1.112V	41 %
−2σ	-36 mV	0.974 V	-58 mV	1.025V	38 %
+2σ	35 mV	1.045 V	61 mV	1.144V	43 %
−3σ	-55 mV	0.955 V	-85 mV	0.998V	35 %
+3σ	53 mV	1.063 V	95 mV	1.178V	44 %

Observe that the deviations in V_{OUT} are not symmetric due to a non-linearity between APS_{OUT} and V_{OUT}. Statistically the results show that there is a 31.8% chance that the V_{OUT} variation is greater than 30 mV without the CDS actuation. Considering a 10-bit ADC converter, it means that the measure for equal light intensity between two adjacent pixels can be greater than 10 LSB in 31.8% of the cases. With the FPN reduction, this value drops to less than 6 LSB. The 40% FPN reduction is a significant result, even with the CDS circuit operating in an unfavourable condition. The APS with a PMOS-type BUFFER transistor makes the APS_{OUT} have its lowest value during τ_{RESET} as shown in the Fig. 2. At this voltage level, the transistor 2, Fig. 4, operates in a subthreshold regime of low transconductance gain, i.e., small offset variations of APS_{OUT} in τ_{RESET} imply in a small variation of the current I_2, responsible for subtracting the different offsets APS_{OUT} caused by the FPN noise.

It can be proven that the FPN noise is directly proportional to the sensitivity of V_{OUT} with a photocurrent I_{ph}, i.e., the response variation V_{OUT}, due to the transistors mismatch, is highlighted by the sensor sensitivity. The characterization of the results of the technique showed in this paper is performed with a photocurrent I_{ph}=3.5 *nA*, which was chosen for being at the peak sensitivity, and the FPN problem is directly proportional to sensor sensitivity. At this operation point, the technique gave a reduction of 40%. Extending the simulations to the complete possible current range for this circuit, the FPN reduction showed in the Fig. 13 is gotten.

In spite of the high efficiency of this technique for higher and lower photocurrents, for those regions the FPN issue is less significant due to the low sensitivity of the sensor for these operation regions. Within the photocurrent range responsible for 95% of the signal swing, the FPN reduction varies between 40% and 65%.

There are some aspects characteristic to this CDS circuit, which limit the efficiency in reducing the FPN. During the τ_{RESET} period, the APS output, APS_{OUT}, presentes a voltage value that varies within a voltage range, 569 mV through 630 mV, Fig. 14. This variation depends on the I_{ph} current level and on the offset variation due to the FPN. At the end of the τ_{RESET} period, the APS_{OU} voltage is sampled on the gate of the transistor 2, Fig. 4, and the offset information is stored by means of current I_2. The transconductance relation $I_D x V_G$ for this transistor is presented in the Fig. 15. It can be observed that the APS_{OUT} possible voltage range during the τ_{RESET} period elapses over a region of low transconductance gain $I_D \times V_g$ for the transistor 2, which shows a quadratic relation after V_{th}. While the current I_2 is limited to a range between 1.1 μA and 2.7 μA, the current I_1 can range values from 1.1 μA to 180 μA. This aspect reduces the relevance of the current I_2, responsible for sampling the offset from the APS_{OUT}, before the I_1 current levels, making the subtraction operation less efficient.

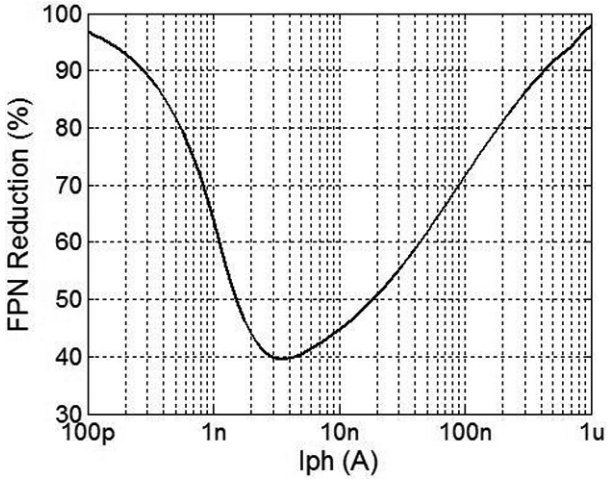

Fig.13 FPN reduction vs Photocurrent.

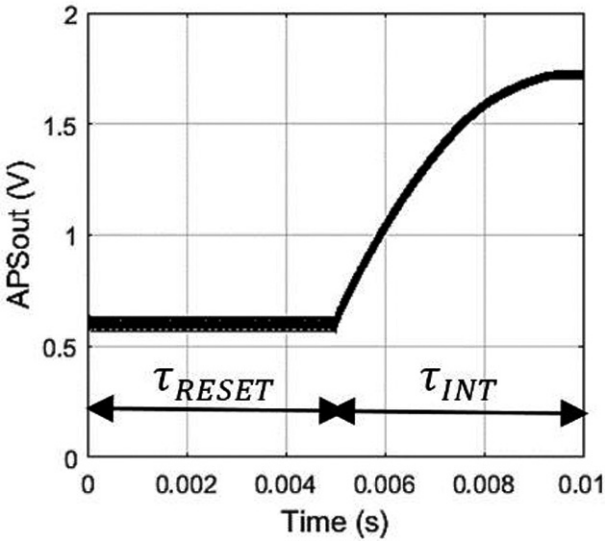

Fig.14 APS_{OUT} signal offset variations during a cycle.

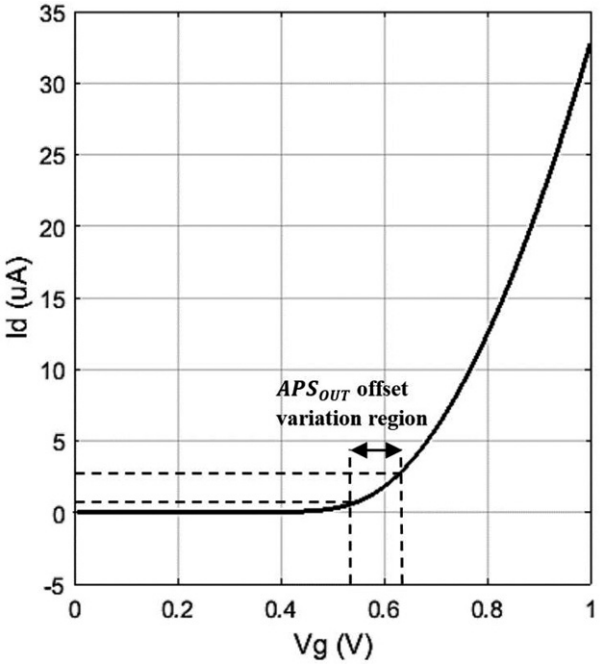

Fig.15 Drain current for the transistor 2 and APS_{OUT} signal offset variation region in the $I_d \times V_g$ curve.

A new improvement is proposed here – referred to as CDS v.2, not yet implemented in a manufactured device – to improve the CDS operation without changing the circuit topology but rather only by readjusting the CDS transistors channel dimensions W and L, which changes their transconductance gain. Once the CDS operates by reducing the offset from the APS output, adjusting the CDS gain is one of the most direct ways to improve its performance on subtracting the FPN. However, due to the transistor non-linearity, this is not enough to make the resulting FPN independent of the current and consequently to allow finding the best parameters to globally reduce FPN within the full expected current range. Under this simple topology there is always going to be a non-linear relation between FPN and photo-current and the FPN cannot be cancelled for the entire region but only for some specific points.

In order to find more compliant values for the CDS transistors W and L, there were chosen a series of values for them and the total FPN was determined by simulation. However, the voltage deviation at the output, which represents the FPN, varies through the entire current domain and there is only a specific current range of interest, in which the light variation is able to cause a measurable voltage output variation. This range is called dynamic range and is depicted in Fig. 16 and Fig. 17 as bottom and upper limits. So, the total mean squared FPN was estimated as the mean error energy, as shown in 4, using the voltage deviation at the output, V_{dev}, which depends on the photocurrent, the current range within the region of interest from I_0 to I_f, and the total number of measured currents in this same region:

$$FPN_{total} = \frac{\sum_{I_0}^{I_f} V_{dev}^2}{n} \quad (4)$$

The current axis is logarithmic so as the human eye response to light is [20]. So, the formula for computing the mean FPN also respects it since the density of current values reduces logarithmically from I_0 to I_f. The FPN for the previously implemented CDS circuit [8] as well as the FPN without CDS and the best curve obtained from the circuit improvement are highlighted in the Fig. 16, as shown in the legend. Other curves for other values of L and W were also obtained, but they are not shown on this graph.

The best curve was obtained with a width change from 10 µm to 18 µm of the transistor 2, Fig. 4, and a width change from 2 µm to 3 µm of the transistor 1. Table V shows the FPN obtained by this formula for the three main curves.

Fig. 17 shows the percentual FPN reduction for both CDS versions. The FPN reduction for the central I_{ph}=3.5 *nA* was by 40% with the implemented CDS circuit. Its new version, CDS v.2, led to a reduction of about 90% for this photocurrent. Considering the whole photocurrent range of interest, the squared mean FPN reduction was by 60% with the previous version and by 96% with the new improved version. Howeve ∓ one can notice that the improvement was not in this entire photocurrent range, but mainly in the surroundings of 3.5 nA. For higher photocurrents, the FPN tends even to increase instead of reduce, as seen in Fig. 16, but since it is already very low at this area without the CDS operation, it will remain low even if it is being magnified.

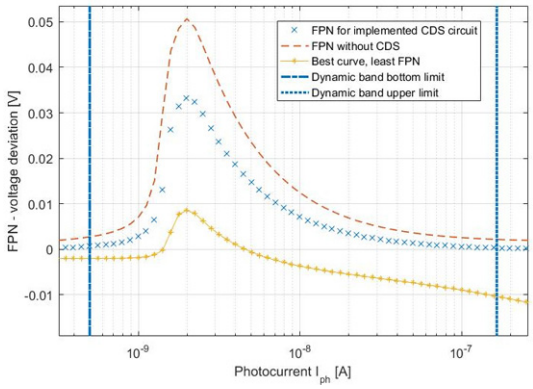

Fig.16 Output voltage deviation versus Photocurrent for the different value of W and L for the CDS transistors.

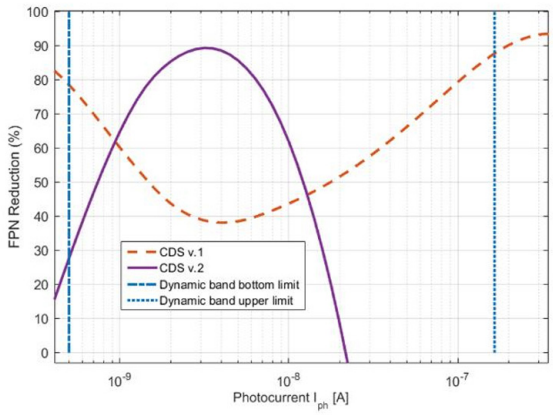

Fig.17 FPN reduction for the previously implemented CDS – CDS v.1 – and for the new improved CDS – CDS v.2.

TABLE V – Simulated results for the squared mean FPN

	Squared mean FPN [mV²]	Squared mean FPN Reduction
Without CDS	0.52398	-
Implemented CDS circuit	0.20630	60.6 %
Best curve	0.01867	96.5 %

Furthermore, the FPN from CDS v.1 cannot be set inside a voltage deviation boundary smaller than 0.3 V CDS v.2 has a voltage boundary of approximately 0.1 V, considering only absolute values, as in Fig. 16. Anyway, there is a trade-off, which should be taken into account according to the targets of the circuit.

V. Experimental Results

The measurement test setup consists of the chip, shown in Fig. 18, set up in the printed circuit board (*PCB*) for physical support, control signals conditioning and voltage regulation at 3.0 V. To generate the control signals (Reset and P2), an Arduino MEGA 2560 microcontroller was used to avoid glitches and delays due to the PC operational-system multitasking. Agilent 33522A Function / Arbitrary Waveform Generator is used as a FD source to generate the waveforms from the Fig. 11 c). For the output signal V_{OUT} measurement, Fig.8, were used the oscilloscope Tektronix TDS2024B and LabView software. All measurements were predicted at 22ºC 1ºC.

The experimental measurements use the same methodology used in the simulation presented in the topic IV. The seven APS response curves, APS_{OUT} concerning the mean and variation of 1, 2 and 3 standard deviations, Fig. 3, are simulated to evaluate the FPN reduction on the V_{OUT} response of the complete circuit consisting in APS, CDS and integrator. The measurement result is obtained by the V_{OUT} value at the end of the integration time τ_{INT} at the elapsed time of 10 ms. Fig. 19 a) shows the V_{OUT} curves for measurement with the CDS circuit activated and the Fig. 19 b) shows the output without CDS actuation.

The values for V_{OUT} in the experimental tests turn up to be very similar to the ones resulting from simulations, however with a slightly greater FPN reduction shown in table VI.

The circuit with the improved CDS version – CDS v.2, i.e. with the new L and W dimensions for certain transistors, was still not implemented. Nonetheless, the experimental results show that the entire circuit works on reducing the FPN as like as predicted by the simulations.

VI. Discussion and Conclusion

A FPN reduction technique was presented in this paper, using a CDS circuit in current mode. Considering the parameter variation, a Monte Carlo simulation was performed in the APS circuit, leading to an offset variation in its response curve with a normal distribution with 14.7 mV standard deviation for the peak sensitivity current, where the FPN is at its highest levels. Two versions of the CDS were developed. The first one, CDS v.1, was simulated, prototyped and tested while the following version, CDS v.2, with the same topology and some different transistor scales, was simulated and compared with the first version. The final output distribution presented a 30.0 mV standard deviation without the CDS actuation and 17.5 mV for the CDS v.1 operation. The match between simulation and experimental measurements validated the methodology. For the CDS v.2, this achieved standard deviation fell to 3 mV.

The presented results show that the proposed and tested solution, CDS v.1, based on a simple additional circuit, leads to more than 40% FPN reduction, with a low additional cost of silicon area, resulting in an improved CMOS image sensor. The new proposed and simulated version, CDS v.2, although not yet implemented on chip, indicates even better results without any additional fabrication costs, with up to 90% FPN reduction, according to the simulation.

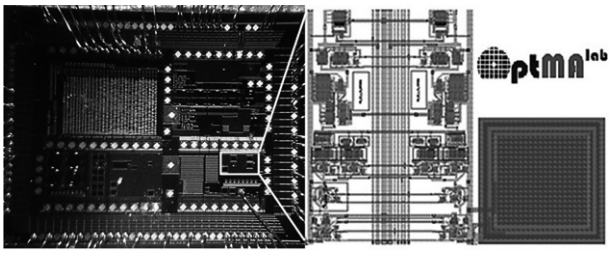

Fig.18 Chip developed and circuit layout of APS, CDS v.1 and Integrator

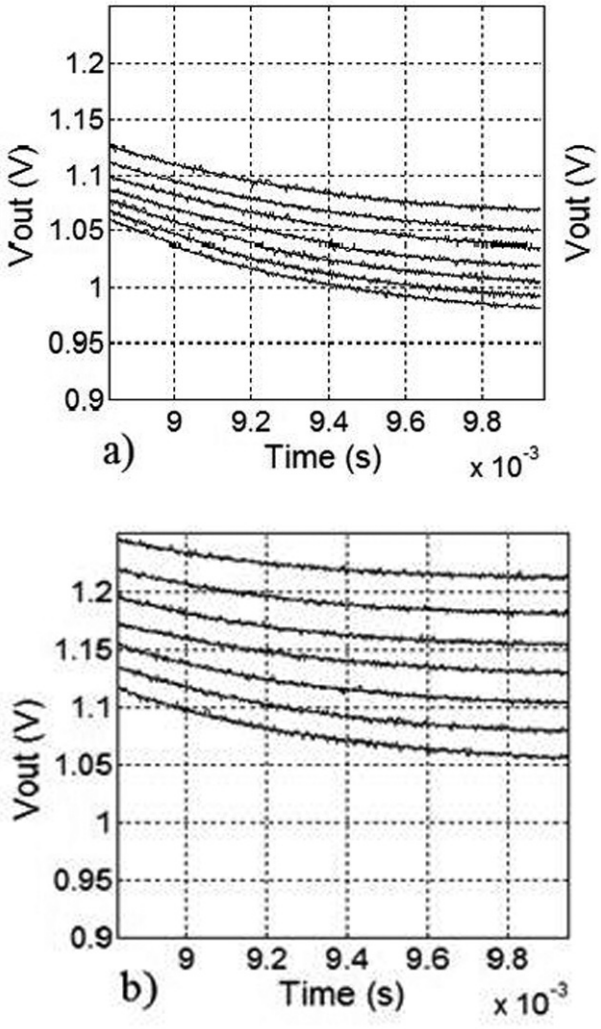

Fig.19 V_{OUT} signal at end of τ_{INT} a) with CDS operation, b) without CDS operation.

Table VI: Experimental results for FPN reduction

	With CDS		Without CDS		FPN Reduction
	Mean Deviation	V_{out}	Mean Deviation	V_{out}	
Mean	0	1.010 V	0	1.083V	-
−σ	-18 mV	0.992 V	-31 mV	1.052V	42 %
+σ	17 mV	1.027 V	29 mV	1.112V	41 %
−2σ	-36 mV	0.974 V	-58 mV	1.025V	38 %
+2σ	35 mV	1.045 V	61 mV	1.144V	43 %
−3σ	-55 mV	0.955 V	-85 mV	0.998V	35 %
+3σ	53 mV	1.063 V	95 mV	1.178V	44 %

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