Power Constrained Design Optimization of Analog Circuits Based on Physical gm/I_D Characteristics

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ABSTRACT

This paper presents a transistor optimization methodology for low-power analog integrated CMOS circuits, relying on the physics-based gm/I_D characteristics as a design optimization guide. Our custom layout tool LIT implements and uses the ACM MOS compact model in the optimization loop. The methodology is implemented for automation within LIT and exploits all design space through the simulated annealing optimization process, providing solutions close to optimum with a single technology-dependent curve and accurate expressions for transconductance and current valid in all operation regions. The compact model itself contributes to convergence and to optimized implementations, since it has analytic expressions which are continuous in all current regimes, including weak and moderate inversion. The advantage of constraining the optimization within a power budget is of great importance for low-power CMOS. As examples we show the optimization results obtained with LIT, resulting in significant power savings, for the design of a folded-cascode and a two-stage Miller operational amplifier.

Index Terms: Analog Design, Sizing, Computer-Aided Design, Simulated Annealing

1. INTRODUCTION

The design of CMOS analog integrated circuits is demanding due to the complex relations between the design objectives (multiple and complex performance specifications to be met, like bandwidth, gain, power, maximum offset voltage, power supply rejection ratio, etc.) and the large number of design variables (transistor sizes and bias currents) to be set. Previous work has been done in the field of analog design automation to enable fast design at the block level. Different strategies and approaches have been used, such as symbolic simulation [8], artificial intelligence [6], fuzzy logic [5], hierarchy and topology selection [10] and geometric programming [11]. The main difficulty encountered for widespread use of these tools is that they require appropriate modeling of both the devices (technology dependence) and of the circuit in order to achieve the design objectives in a reasonable processing time. The choice of different circuit topologies to support in a method or tool is also a problem, since most approaches work with topology-based equations, which limits the application range. The addition of new block topologies has to be supported, and requires again expert analog designer knowledge. The use of optimization algorithms combined with physical models seems to be a good solution when applied to specific applications, since a general solution most often proves to have shortcomings for fully exploiting the capabilities of the analog CMOS technology. The main requirements of an analog synthesis tool are: user interactivity, flexibility for multiple topologies, connection to automatic layout generation, and reasonable response time. The interface with an electrical simulator is also convenient. This paper describes a methodology for analog CMOS design automation that combines the simulated annealing optimization technique, a physics-based transconductance-to-current ratio characteristics and the electrical simulation integrated in the module LIT-S of the LIT tool [9], providing even to a non-expert user a very flexible tool that is able to size analog circuits, including a broad range of analog constraints, including total power dissipation. The paper is organized as follows: section 2 describes the proposed methodology and explains how the simulated annealing algorithm, the gm/I_D characteristics and the ACM MOSFET model are used to search opti-

mized designs; section 3 shows the synthesis of a two-stage Miller operational amplifier in order to demonstrate the capabilities of the methodology; section 4 presents the automatic synthesis of a folded-cascode operational amplifier and a comparison with traditional hand-made design; and section 5 summarizes main contributions.

2. ANALOG DESIGN METHODOLOGY

The design of analog CMOS integrated circuits requires extensive design practice with a given technology to correctly size MOS transistors in order to achieve the required performance. Analytical knowledge-based equations describe the relations between the transistors (design parameters), design specifications (e.g. slew-rate more than 10V/μs) and design objectives (such as minimum power, area, noise, etc, or a combination thereof). These equations are topology-specific and can be used within an automatic synthesis methodology, which must perform the resolution of a system of non-linear equations. This system usually has more independent variables than independent equations, returning a wide solution space. The search for an optimum design, however, is often made by extensive simulation practice, by expert heuristics and, to a much lesser extent, by optimization algorithms. The simulated annealing (SA) algorithm was implemented as a good alternative to optimize the design, since it exploits the entire design space, including different transistor lengths. In most devices these are kept fixed by the tools or the designer. SA is a well known random-search technique which exploits an analogy between the way in which a metal cools and freezes into a minimum energy crystalline structure (the annealing process) and the search for a minimum of a cost function in a more general system. It forms the basis of an optimization technique for combinatorial and other problems [12]. The use of simulated annealing in the synthesis of analog circuits was reported in previous works [7, 15]. SA's major advantage over other methods is the ability to avoid becoming trapped in local minima in the parameter space. The algorithm employs a random search which does not only accept solutions that decrease the objective cost function f_c (assuming a minimization problem), but also some changes that increase it. In the design procedure herein proposed, a methodology called gm/I_D is used for the circuit performance evaluation. This methodology considers the relationship between the ratio of the gate transconductance gm over DC drain current I_D and the normalized drain current $I_n = I_D/(W/L)$ as a fundamental design parameter [13], such as the measured curve shown in figure 1. The gm/I_D characteristic is directly related to the performance of the transistors, gives a clear indication of the device operation region (weak, moderate or strong inversion) and provides a way for straightforward estimation of transistors dimensions. The main advantage of this method is that the gm/I_D x I_n curve is unique for a given technology, reducing the number of electrical parameters related to the fabrication process. Additionally, its analytical form covers continuously all transistor operation regimes, from weak to moderate to strong inversion. In the LIT tool, the gm/I_D x I_n curve is automatically evaluated by electrical simulation using the ACM compact MOSFET model [3], which is also implemented in the commercial simulator SMASH. An automatic parameter conversion procedure from BSIM3 to ACM is reported [2], warranting the compatibility with most technology kits provided by silicon foundries. The analog circuit modeling for simulated annealing is straightforward. The design objective, or its cost function, has to be formulated appropriately and then minimized. In this work we propose and use the following cost function:

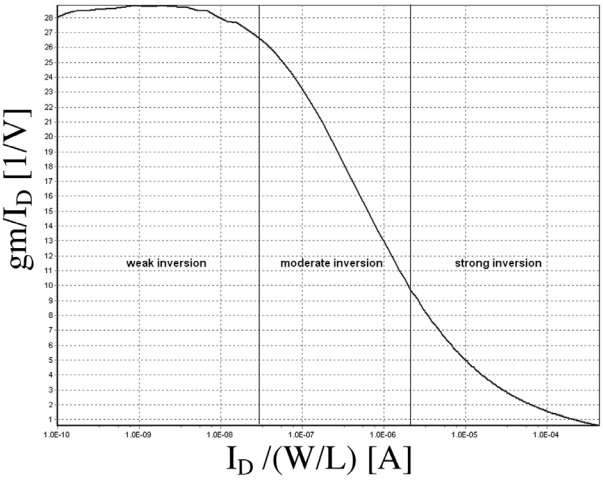

Figure1. Measured *gm/I*$_D$ x I_n curve for NMOS 0.35μ*m* CMOS technology.

$$f_c = \sum_{i=1}^{n} \alpha_i \hat{p}_i(X) + \sum_{j=1}^{m} \beta_j \hat{c}_j(X) \qquad (1)$$

where n is the number of design objectives and α_i is the weighting coefficient for performance parameter $\hat{p}_i(X)$, which is a normalized function of the vector of independent design parameters X. This function allows the designer to set the relative importance of competing performance parameters, such as, for example, a weighted relation between power and area. The parameter $\hat{c}_j(X)$ is a constraint normalized function, which shrinks the design space to feasible solutions of m design specifications. The coefficient β_j

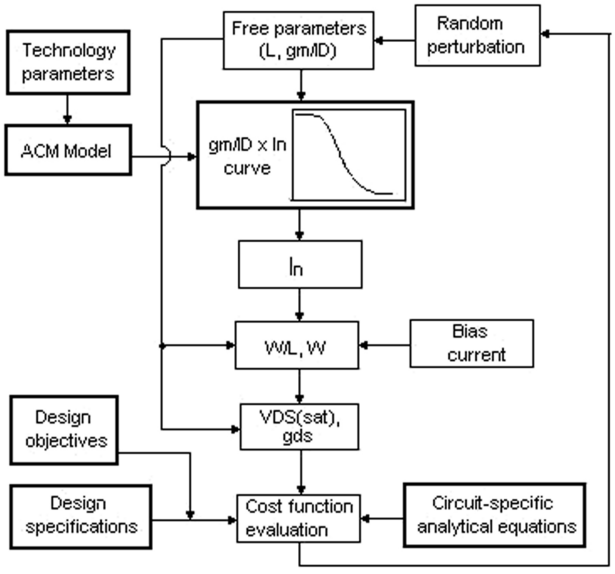

Figure 2. Proposed design flow.

indicates how closely the specification must be pursued. If $\hat{c}_j(X)$ is inside a given specification, it is set to zero. The correct design space exploration is directly related to the cost function formulation [4]. Figure 2 shows the proposed sizing procedure design flow. The user enters the design variables, technology parameters and configures the cost function according to the required design objectives and specifications. The optimization loop performs a random perturbation on design variables, whose amplitude is defined by the system "temperature" (which is initially high and cools down as the process evolves). These variables are defined by the user, and are always related to transistor geometry, large and small-signal parameters, such as W, L, I_D, gm and gm/I_D. Following, the design properties evaluation is performed by the calculation of the circuit characteristics such as gain, cut-off frequency, phase margin, DC power, common-mode range, etc. This is done using circuit-specific analytical equations, the gm/I_D versus I_n curve and the ACM model for the calculation of transconductances, drain-source saturation voltages and currents. If the circuit is feasible, i.e., transistor sizes are within an allowed range, the cost function can be evaluated and the solution is accepted if the cost decreased or else if the cost increased to avoid trapping in a local minimum - in the last case with a given probability inversely related to the system temperature. Next iteration starts with a new temperature calculated by the following equation:

$$T_{k+1} = \alpha \cdot T_k \qquad (2)$$

Here, α is a constant close to 1 (but smaller)

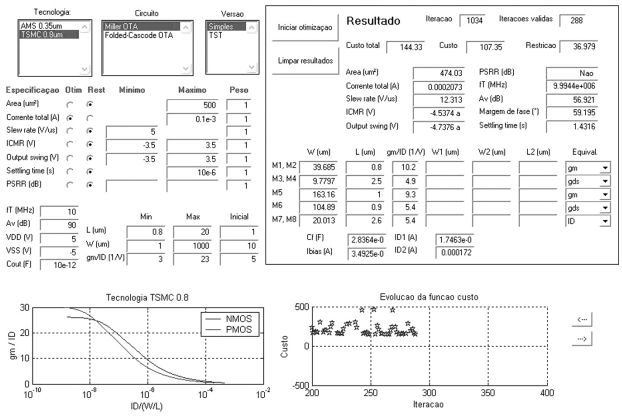

Figure 3. Main screen of the LIT-S module for transistor sizing embedded in LIT tool.

and k is an index that indicates the iteration step. This relation results in an exponential decay. The process finishes when temperature reaches some determined value or the cost function variation does not suffer relevant changes with perturbations of the variables. A trade-off between response time and refinement of final solution can be achieved setting the value of α parameter. The final solution returns the devices dimensions W and L. The entire automatic optimization flow is implemented as a module in the LIT tool using an optimization routine called *Adaptative Simulated Annealing* [14] through ASAMIN interface [15]. A graphical interface was developed in order to provide faster and intuitive data entry, system configuration and visualization of results, and integrated as a module of LIT tool called LIT-S. The main screen of LIT-S module is shown in figure 3. The tool returns a spice-like description of the sized circuit and the evaluated performance. External electrical simulations are then evaluated at this stage, in order to verify the solution integrity. The physical synthesis can also be performed in the LIT tool, which generates the layout according to specific criteria of transistor pair matching, transistor folding/splitting, and even more complex associations of transistors.

3. AUTOMATIC DESIGN OF A TWO-STAGE OPERATIONAL AMPLIFIER

The proposed algorithm and design methodology were implemented and applied to the synthesis of a two-stage operational amplifier, shown in figure 4. This amplifier is composed by an input differential pair with active load in the first stage, an inverter amplifier in the second stage, and a compensation capacitor for stability, connecting nodes 4 and 5 between 1st and 2nd stages. The analytical equations that describe the behavior of this circuit are well-known [1]. In this

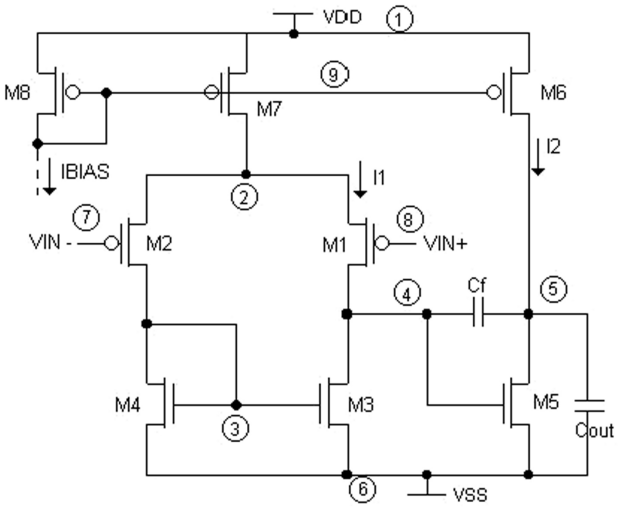

Figure 4. Schematics of a two-stage Miller operational amplifier.

Table 1. Specifications and simulated results for the Two-Stage Miller Amplifier.

Specification	Required	Simulated
Total current (μA)	≤ 200	102
Phase margin (°)	≥ 60	60
Low-frequency gain (dB)	≥ 90	95
GBW (MHz)	≥ 15	15
Slew-rate (V/μs)	≥ 15	15
ICMR$^-$ (V)	≤ -1	-0.8
ICMR$^+$ (V)	≥ 1	1.4
Total area (μm^2)	minimize	9064
Offset (μV)	≤ 200	160
Cost function	minimize	1.62

example, we want to size the transistors in order to achieve the design specifications given in Table 1. The design objective (f_c) is to minimize the relative area and total DC current, and to maximize the low-frequency gain *Av*, in the following way:

$$f_c = \frac{A}{A_0} + \frac{I_{DD}}{I_{DD0}} + \frac{A_{v0}}{A_v} \tag{3}$$

Here, A is the silicon area occupied by all transistors, including drain and source regions (estimated), A_0 is a reference area for normalization, I_{DD} is the total supply current, I_{DD0} is a reference current, A_v is the low-frequency gain, and A_{v0} is a reference gain. The gate transconductance of the input differential pair is set by the GBW and Miller cap, as:

$$gm_1 = GBW \cdot C_f \tag{4}$$

The drain current for these transistors can be calculated with the information about the transconductance-to-current ratio, which is treated as an independent variable:

$$I_{D1} = \frac{gm_1}{\left(\frac{gm}{I_D}\right)_1} \tag{5}$$

So, the aspect ratio for the input transistors is:

$$\left(\frac{W}{L}\right)_1 = \frac{I_{D1}}{I_{n1}} \tag{6}$$

$$W_1 = \left(\frac{W}{L}\right)_1 \cdot L_1 \tag{7}$$

where I_{n1} is the normalized current given directly by the gm/I_D x I_n curve. The transistor widths W are determined after the optimization of L, which is an independent variable as well as gm/I_D. The same approach is done for the remaining transistors. For example, the dimensions of the transistors in the current mirror load are determined by:

$$\left(\frac{W}{L}\right)_3 = \frac{I_{D1}}{I_{n3}} \tag{8}$$

$$W_3 = \left(\frac{W}{L}\right)_3 \cdot L_3 \tag{9}$$

The design characteristics calculation is straightforward. The low-frequency gain, for example, is given by

$$A_v = \left(\frac{gm}{I_D}\right)_1 \cdot \left(\frac{1}{\frac{1}{VA_1} + \frac{1}{VA_3}}\right) \cdot \left(\frac{gm}{I_D}\right)_5 \cdot \left(\frac{1}{\frac{1}{VA_5} + \frac{1}{VA_6}}\right) \tag{10}$$

Our LIT tool implements the ACM model source code and can estimate the Early voltage (VA) according to the transistor length. In this example, the technology used is CMOS $0.35\mu m$, the power supply voltage rails are $\pm 1.65\,V$ and the load capacitance is $10pF$. The independent variables subjected to perturbations by the simulated annealing algorithm are: $L_1 = L_2$, $L_3 = L_4$, L_5, L_6, $L_7 = L_8$, $(gm/I_D)_1 = (gm/I_D)_2$, $(gm/I_D)_3 = (gm/ID)_4$, $(gm/I_D)_5$, $(gm/I_D)_6$, $(gm/I_D)_7$, and the dependent parameters are $W_1 = W_2$, $W_3 = W_4$, W_5, W_6, $W_7 = W_8$, C_f and bias current. The constraints $L \geq L_{min}$, $W \geq W_{min}$ and $(gm/I_D)_{min} \leq (gm/I_D) \leq (gm/I_D)_{max}$ avoid infeasible solutions, with $L_{min} = 0.3\mu m$, $W_{min} = 0.6\mu m$, $(gm/I_D)_{min} = 0.1$ and $(gm/I_D)_{max} = 25$ in our technology. The range of gm/I_D is well known from device physics and behaves

smoothly over a range of several decades of transistor bias currents, which is advantageous for the search robustness. Moreover, the design space is limited by values of gm/I_D less than about $28\,V^{-1}$, which is the theoretical maximum gm/I_D of bulk MOS transistors. Design objectives and design specifications are evaluated in terms of free variables $(gm/I_D)_i$ and L_i. The same occurs with the dependent variables such as W_i and I_{Di}. The optimization process for the example took 158 iterations and mere 91 million floating point operations. The final transistors sizes obtained by the iterations with analytical models are shown in table 2. The effective exploration of the design space is evident with the solution for gm/I_D ranging from $0.7V^{-1}$ (strong inversion) to $16.5V^{-1}$ (moderate inversion). The third column of table 1 shows the performance of the optimized solution obtained by electrical simulations of the sized circuit with SMASH. Figure 5 shows the evolution of the cost function after each iteration, converging to a minimum value, reaching stability as the cool-down proceeds.

AUTOMATIC DESIGN OF A FOLDED-CASCODE OPERATIONAL AMPLIFIER

In order to exemplify the proposed optimization methodology for different topologies, we show how the synthesis of a folded-cascode operational amplifier is performed using the module LIT-S. The schematic of the amplifier is shown in figure 6. Some equations that describe the circuit behavior are the following:

$$SR = I_{D3} / C_L \tag{11}$$

$$V_{out(\max)} = V_{DD} - 2\left|V_{DS4(sat)}\right| \tag{12}$$

$$V_{out(\min)} = 2 \cdot V_{DS8(sat)} + V_{SS} \tag{13}$$

$$R_1 = V_{DS4(sat)} / I_{D4} \tag{14}$$

$$R_2 = V_{DS8(sat)} / I_{D8} \tag{15}$$

$$GBW = gm_1 / C_L \tag{16}$$

$$V_{in(\min)} = V_{SS} + V_{DS3(sat)} + V_{GS1} \tag{17}$$

$$V_{in(\max)} = V_{DD} - \left|V_{DS4(sat)}\right| + V_{T1} \tag{18}$$

$$P_{diss} = (V_{DD} - V_{SS}) \cdot (2 \cdot I_{D3} + 3 \cdot I_{D4}) \tag{19}$$

For matching purposes, some transistors have to be identical (same width W and same length L). Table 3 shows the matching constraints. The free variables for the optimization procedure are the

Table 2. Transistors sizes obtained by the optimization method for the Miller amplifier.

Transistor	*W* (μm)	*L* (μm)	*gm*/*I*$_D$ (V^{-1})
M_1, M_2	74.8	1.2	16.5
M_3, M_4	15	6.6	4.7
M_5	147.0	0.6	15.7
M_6	10.7	6.0	0.7
M_7, M_8	5.5	0.8	3.1

Table 3. Matching constraints and free variables for the folded-cascode amplifier.

Matching requirement	Free parameters
$M_1 = M_2$	L_1, $(gm/I_D)_1$
$M_3 = M_{15}$	L_3, $(gm/I_D)_3$
$M_4 = M_5 = M_{14}$	L_4, $(gm/I_D)_4$
$M_6 = M_7$	L_6, $(gm/I_D)_6$
$M_8 = M_9 = M_{10} = M_{11}$	L_8, $(gm/I_D)_8$
M_{12}	L_{12}, $(gm/I_D)_{12}$

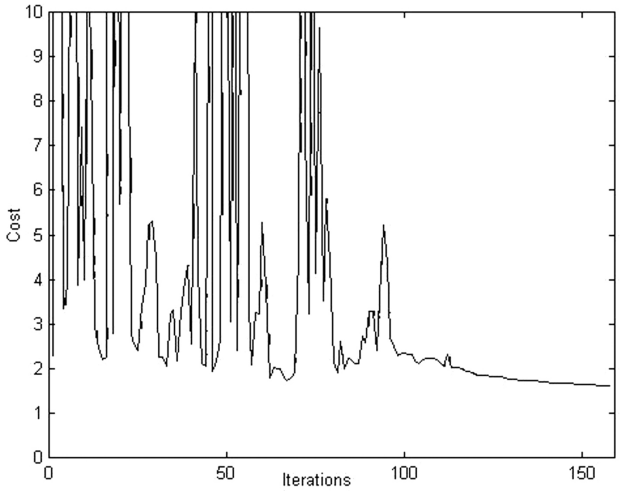

Figure 5. Cost function evolution.

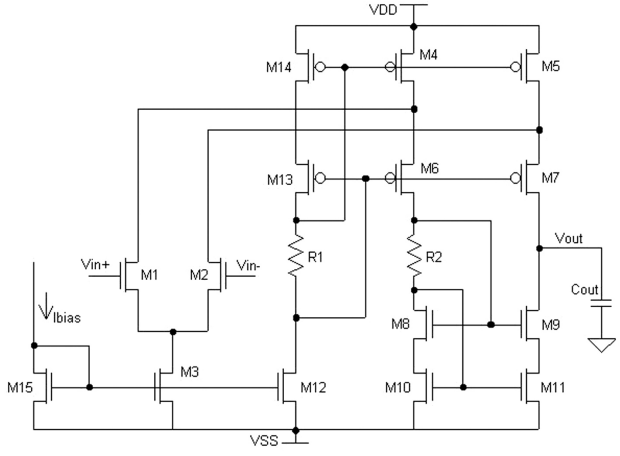

Figure 6. Schematics of a folded-cascode operational amplifier.

corresponding channel length and transconductance-to-current ratio. The input gate transconductance gm_1 is given by the gain-bandwidth and slew-rate requirements. The current I_{D1} that flows in these transistors can be easily evaluated by the same approach of eq. 5, using the gm/I_D x I_n curve for the determination of I_{n1} and the given gm_1 for the estimation of I_{D1}. So, the bias current is given by $I_{D3} = 2 \cdot I_{D1}$. As the next step, the normalized current for the input transistors is calculated based on the gm/I_D curve and the corresponding transconductance. In order to avoid zero current in the active load, we consider $I_{D4} = I_{D6} = I_{D8} = 1.25 \cdot I_{D3}$. At this point, as we have the gm and I_D of all transistors, we can estimate the remaining normalized currents using the curve gm/I_D x I_n. The aspect ratio of all transistors is now calculated by eq. 6. At this point, the dimensions of all transistors in the circuit are evaluated. The dependent variables $V_{D(sat)i}$, gm_i and gds_i are calculated straightforward with the ACM model. The cost function is evaluated according to design specifications given by equations 11 to 19. Table 4 shows an example for low-power design, with the required specifications and the simulated results obtained by the optimization procedure. The design objective is to minimize the dissipated power, maintaining the remaining specifications inside an allowed range. The optimization process took about 1 minute running on a PC with Intel Celeron 1.3 GHz. The resulting transistor sizes are shown in table 5, for a 0.35μm technology.

Table 4. Specifications and simulated results for the folded-cascode amplifier.

Specification	Required	Automatic synthesis	Manual synthesis
Low-frequency gain (dB)	≥ 65	74	67
GBW (MHz)	≥ 15	15	15
Phase margin (°)	≥ 60	70	84
Slew-rate (V/μs)	≥ 10	11	17
$V_{in(min)}$ (V)	≤ -1	-1	-1.2
$V_{in(max)}$ (V)	≥ 1	1	1.3
$V_{out(min)}$ (V)	≤ -1	-1	-1.1
$V_{out(max)}$ (V)	≥ 1	1.5	1.1
Dissipated power (mW)	minimize	1.9	2.5
Total area (μm²)	minimize	927	1391

Table 5. Transistors sizes obtained by automatic optimization and by manual synthesis for the folded-cascode amplifier.

Transistor	Automatic synthesis		Manual synthesis	
	W (μm)	L (μm)	W (μm)	L (μm)
M_1, M_2	142.0	0.8	140.0	2.0
M_3, M_{15}	23.6	0.7	21.2	2.0
M_4, M_5, M_{14}	23.3	4.2	47.6	2.0
M_6, M_7	10.0	4.1	47.6	2.0
M_8, M_9, M_{10}, M_{11}	94.0	0.6	15.3	2.0
M_{12}	29.5	0.7	26.6	2.0

A. Comparison with conventional manual design

In the hand-made design, the channel length of all transistors is usually kept fixed in order to decrease the number of free variables. The designer has to choose a determined size for L that minimizes the influence of short-channel effects. Also, all transistors are considered to be in saturation and strong inversion region, simplifying the current and transconductance equations. The MOS model used usually is a simplified Spice Level 3, which turns the design very imprecise. Several electrical simulations must be made in order to refine the solution. A manual design methodology of the folded-cascode operational amplifier is related in [1]. The basic considerations are that all transistors have the same channel length, operate in strong inversion and saturation region. The transistor sizes are calculated based on the design specifications, according to the equations 11 to 19. The design procedure is linear and fixed and there is no place for exploration of the design space. The optimization is a difficult task, since usually the designer feeling is the only strategy. The design time is also a factor to be considered. Even expert designers can take some hours to complete a design that meets the specifications. For comparison purposes, we have designed a folded-cascode using the manual methodology. The transistor dimensions achieved are shown in table 5 and the resulting performance parameters are shown in last column of table 4. We can see that the automatic design achieves better results in terms of DC power and area, with advantages on total design time.

5. CONCLUSION

The proposed methodology combines the SA algorithm, the gm/I_D characteristics and the ACM MOSFET model in the same environment in order to optimize the design of analog integrated circuits based on the transistor inversion coefficient. The main advantage of using the SA over the crude gm/I_D technique is that the design space is explored in a more effective way, combining operation in weak, moderate and strong inversion to achieve optimum low-power design. The methodology is implemented in the LIT tool and provides a reasonable solution in a short CPU time. The main advantage is the simple sizing method based on the transistor inversion coefficient, which is calculated by a single technology-specific characteristic curve gm/I_D versus I_n. The design space is not limited to strong inversion region, but also to moderate and weak inversion, allowing low-power optimum design. Comparing with a typical human-made design procedure, the advantages of using an automated design methodology are the reduced

design time, better performance and the possibility, even for non-expert analog designers, to achieve good solutions for non-critical applications with full exploration of the design space.

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