Journal of Integrated Circuits and Systems

Volume 2 • Number 1 • March 2007 • ISSN 1807-1953

Measuring the Efficiency of Cache Memory on Java Processors for Embedded Systems
A. C. S. Beck, M. B. Rutzig, and L. Carro

A Cryptography Core Tolerant to DFA Fault Attacks
C. R. Moratelli, É. Cota and M. S. Lubaszewski

Power Constrained Design Optimization of Analog Circuits Based on Physical g_m/I_D characteristics
A. Girardi and S. Bampi

Communication Aware Optimization of the Task Binding in Hardware/Software Reconfigurable Networks
T. Streichert, C. Strengert, D. Koch, C. Haubelt, and J. Teich

Hardware Support in a Middleware for Distributed and Real-Time Embedded Applications
E. T. Silva Jr, F. R. Wagner, E. P. Freitas, L. Kunz and C. E. Pereira

Mapping of Massive Data Processing Systems to FPGA Computers Based on Temporal Partitioning and Design Space Exploration
P. S. B. do Nascimento, S. M. da Silva, J. L. Seixas, R. E. Sant'Anna, and M. E. de Lima

The **Journal of Integrated Circuits and Systems** (**JICS**) is a publication from SBMicro – Brazilian Microelectronics Society and SBC – Brazilian Computer Society whose are non-profit scientific societies aiming to foster the microelectronics and computer science teaching, research and development.

***Editor-in-chief*:**

João Antonio Martino, University of Sao Paulo, Brazil

***Co-Editor*:**

Luigi Carro, Federal University of Rio Grande do Sul, Brazil

***Associate Editors*:**

Process and Materials

Jacobus Swart, State University of Campinas, Brazil
Olivier Bonnaud, University of Rennes, France

Devices and Characterization

Marcelo Antonio Pavanello, FEI University, Brazil
Cor Claeys, IMEC, Belgium

Design

Armando Gomes, Motorola, Brazil
Franco Maloberti, Texas A&M, USA

Test

Vladimir Castro Alves, Morphotec, USA
Yervant Zorian, Logic Vision, USA

CAD

Reinaldo Bergamaschi, IBM, USA
Ahmed Jerraya, TIMA, France

Sponsored by:

Brazilian Computer Society
Av. Bento Gonçalves, 9500
Porto Alegre, Brazil
Caixa Postal 15012 – CEP 91501-970

Brazilian Microelectronics Society
Av. Prof. Luciano Gualberto, trav. 3 n. 158
CEP 05508-900, Sao Paulo, Brazil

Journal of Integrated Circuits and Systems

Volume 2 • Number 1 • March 2007 • ISSN 1807-1953

CONTENTS

Foreword 5

Measuring the Efficiency of Cache Memory on Java Processors for Embedded Systems
A. C. S. Beck, M. B. Rutzig and L. Carro 7

A Cryptography Core Tolerant to DFA Fault Attacks
C. R. Moratelli, E. Cota and M. S. Lubaszewski 14

Power Constrained Design Optimization of Analog Circuits Based on Physical g_m/I_D characteristics
A. Girardi and S. Bampi 22

Communication Aware Optimization of the Task Binding in Hardware/Software Reconfigurable Networks
T. Streichert, C. Strengert, D. Koch, C. Haubelt and J. Teich 29

Hardware Support in a Middleware for Distributed and Real-Time Embedded Applications
E. T. Silva Jr, F. R. Wagner, E. P. Freitas, L. Kunz and C. E. Pereira 38

Mapping of Massive Data Processing Systems to FPGA Computers Based on Temporal Partitioning and Design Space Exploration
P. S. B. do Nascimento, S. M. da Silva, J. L. Seixas, R. E. Sant'Anna, and M. E. de Lima 45

FOREWORD

This issue of Journal of Integrated Circuits and Systems (JICS) includes 6 papers on design, test and CAD. These papers have been selected from the presentations given at SBCCI2006 (Symposium on Integrated Circuits and Systems Design), which was organized in Ouro Preto, Brazil in 2006. Among the contributions presented at SBCCI2006 conference, only a few were selected by the Technical Committee for this issue. These papers have been submitted to usual reviewing process with the help of external experts.

We would like to thank the authors for their effort in preparing these high quality papers, as well as the reviewers for their help on paper selection which guarantees the scientic level of this issue. We sincerely hope that JICS readers will enjoy these contributions, as we have enjoyed listening to them at the SBCCI2006 conference.

The Editors.

www.sbc.org.br/jics
www.sbmicro.org.br/jics

ISSN 1807-1953