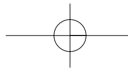

A Review of SOI Technology and its Applications

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ABSTRACT

Classical scaling is no longer possible to follow Moore's law. In addition to the material innovations such as high K/metal gate and stressors, a transition to SOI is essential to meet scaling and performance requirements alike. The advances in SOI for fully depleted devices and some key SOI applications are described.

INTRODUCTION

Substrate engineering [1] has enabled the industry to overcome many of the limitations encountered by traditional scaling. As a result, device architecture and engineered substrates have become strongly coupled, a coupling that is growing stronger as the IC industry moves to the 32 nm technology node and beyond. Substrate engineering started in earnest with the industry transition to SOI wafers in the late '90s. SOI substrates made possible increasing the drive current while simultaneously reducing parasitic leakage and capacitance, thus improving IC performance and reducing power consumption. SOI has allowed the IC industry to develop superb solutions for high performance logic [2].

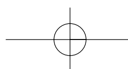
A review of applications driving high performance devices is presented here. The SOI architecture for low power application is also discussed.

Ultra-Thin Body (UTB) device architecture is extensively investigated to suppress the short channel effects (SCE) for scaling gate length beyond 30 nm and to lower the sub-threshold leakage as projected by the International Technology Roadmap for Semiconductors (ITRS). The combination of high mobility channels and UTB SOI devices is most appealing for high density, high performance and low power applications. The future nodes are driving numerous substrate solutions.

Today's partially depleted (PD) transistor architecture implemented for high performance processors may evolve into a fully depleted (FD) approach with planar single gate transistors or with multiple gate (FinFET, TriGate) structures. SOI substrates are also essential to RF circuits, Si-based Optoelectronic devices, MEMS, high voltage and Smart Power circuits, back-side illuminated image sensors, and to other emerging applications [3].

SMART CUT™ TECHNOLOGY FOR SEMICONDUCTOR ON INSULATOR SUBSTRATES

Smart Cut™ technology relies on transfer of a high quality single crystal layer from one wafer to another [4]. In typical applications, a thin layer of Si that is coated with thermal oxide is bonded and transferred from its original "donor" wafer to another Si "handle" wafer that is coated with only native oxide [5]. The process sequence starts with oxidizing the donor wafer, followed by implanting ions, typically hydrogen, through the oxide and into silicon. Hydrogen doses $>5\times10^{16}$ cm^{-2} are typically used for splitting of silicon. Then the donor wafers and the handle wafers are very carefully cleaned to remove any particles and to provide surface chemistry that is most favorable to wafer bonding. Wafer pairs are properly positioned with respect to each other and lightly pressed together to initiate a fusion wave that makes the wafers stick together. In the following step, wafer pairs are split along the hydrogen-weakened zone that was previously produced within the donor wafers. Typically thermal energy is sufficient to induce splitting, but mechanical force can be used in some cases instead of heating. After the split, finishing procedures are used to make the surface of the newly made SOI wafers smooth, and an annealing step strengthens the bonded interface. The donor substrates, which were split off the SOI wafers and are now thinner by a



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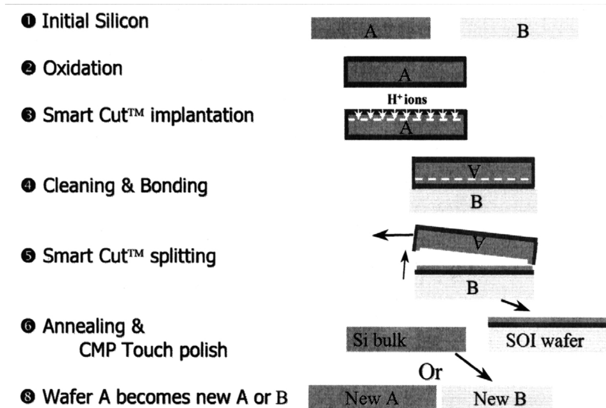

Figure 1. Smart Cut™ technology process flow.

micron or less, are repolished in preparation for making another batch of SOI wafers. A typical Smart Cut™ process sequence is shown in Fig. 1.

The thickness of the silicon or another semiconductor film and/or buried oxide or other insulator can be adjusted in a wide range in the Smart Cut™ technology by tuning the implant energy and oxidation or deposition time. The thickness of the silicon film in current applications typically runs from about 5 nm to 1.5µm. The thickness of the silicon dioxide is typically set at 10 nm to 5 µm. SOI wafers are thus adaptable to most device architectures, from ultra-thin CMOS to thick-film power transistors and sensors as shown in Fig. 2. It also should be mentioned that only conventional equipment is needed for mass production of 8” and 12” SOI wafers [6]

Since the Smart Cut™ technology is a layer transfer technique, it allows producing a variety of engineered wafers, with a layer of one material placed on a substrate of a different material. For example, biaxially strained Si layers or relaxed layers of SiGe alloys can be bonded to Si handle wafers with SiO_2 in between [3], germanium films on insulator (GeOI) can be formed [7], and compound semiconductor layers on oxidized Si handle wafers can be produced. Multilayer structures such as SOLES wafers that combine SOI and GeOI hold promise for monolithic integration of CMOS and III-V RF devices [8]. The dielectric film can be SiN or a composite film of SiO_2 and SiN, and in principle the handle wafer can be glass, fused silica, SiC or another flat and smooth substrate. This flexibility in combining dissimilar materials with specific properties facilitates fabrication of devices with improved performance or better matched to the unique need.

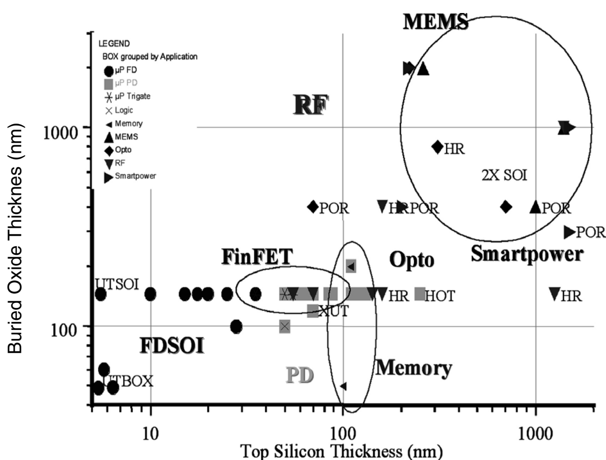

Figure 2. Smart Cut™ addresses various SOI applications

CURRENT SOI APPLICATIONS

High Performance microprocessors

The single largest application of SOI is in high performance microprocessors that are used in a broad spectrum of applications, from desktop PCs and game systems to servers, specialized scientific computers and the largest supercomputers. The use of SOI leads to higher performance, lower dynamic and static power and better immunity to soft errors.

Microprocessors in x86 architecture from AMD:

Manufactured on SOI since 2003. Initially introduced as a single-core Opteron™ built in 130 nm technology, it has evolved to a multi-core architecture in production in 65 nm design rules and moving to 45nm technology.

Microprocessors in POWER architecture:

Built by IBM and Freescale, and their foundry partners for use in some PCs, a variety of servers and blades, and customized mainframe computers. POWER6™ is the latest IBM version in production, with 65 nm design rules, and a clock frequency >4GHz [9]. An integrated communications processor MPC 8569E PowerQUICC™ III from Freescale is built in 45 nm design rules, and it combines an e500 processor core built on Power Architecture™ technology with system logic required for networking, wireless infrastructure, and telecommunications applications.

Cell architecture microprocessors:

Initially designed by IBM, Sony and Toshiba for game systems (Sony PlayStation 3), but also used or planned for HD TVs and a variety of other graphics intensive and multitasking applications. Cell is a heterogeneous chip multiprocessor that consists of an IBM 64-bit Power Architecture™ core, augmented with eight specialized co-processors based on a novel single-instruction multiple-data (SIMD) architecture called Synergistic Processor Unit (SPU), which is for

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data-intensive processing, like that found in cryptography, media and scientific applications.

Gaming processors:

XBOX 360, Play Station 3 and Wii

Supercomputers:

Four out of the top five most powerful supercomputers on the www.top500.org list are based on SOI microprocessor chips. First on the list is Roadrunner, which can operate at 1 petaflops (1E15 floating point operations/sec). This system contains 6,948 dual-core Opteron™ processors and 12,960 PowerXCell™ 8i processors that are interconnected with about 57 miles of optical fiber. The Opteron processors handle standard processing such as file system I/O. The PowerXCell 8i processors accelerate mathematical and CPU-intensive processing. PowerXCell 8i is an HPC-specific modification of IBM's first-generation Cell Broadband Engine (Cell/B.E.) processor designed for the computer gaming market and the Sony PlayStation.

Low Power Applications

Performance and power are inversely related – operating a very high performance microprocessor at a reduced supply voltage Vdd cuts down on performance while greatly reducing power consumption during operation.

True low power circuits require that both the dynamic power Pdyn and the standby or static power Pstat are minimized:

$$P = P_{stat} + P_{dyn} = I_{off}(V_{dd})V_{dd} + a f C_{load} V_{dd}^2$$

where f is the switching frequency and a is a proportionality coefficient.

The leakage current Ioff should be as low as 10 pA/mm in low standby power (LSTP) devices, and a few nA/mm in low operating power (LOP) devices. Fully depleted (FD) SOI transistors with undoped channels are ideally suited for low power applications [10]. Substrates for FD devices require very thin Si films, of the order of 20 nm with the uniformity range of <1 nm. After processing, transistor channel regions are as thin as 4-5 nm, which makes the S/D junction area and its contribution to Cload very small.

FD SOI devices combined to ultra thin buried oxide SOI have very steep subthreshold slopes, with values close to the theoretical minimum. This allows setting Vt and Vdd very low, and assures that both Pstat and Pdyn are low.

Oki has specialized for many years in applications that are less demanding in performance but require ultra-low power. They have been building FD SOI system-on-a- chip (SOC) circuits for several popular lines of solar-powered radio-controlled Casio watches [11].

UTB-SOI DEVICES FOR ELECTROSTATIC CONTROL

Planar Ultra-Thin-Body (UTB) SOI devices are considered among the best candidates to increase the control of SCE. Extremely thin, 4-6 nm films, are widely recognized for their potential for the end-of-the-roadmap transistors as projected by ITRS. The SOI substrate fabrication based on the Smart Cut™ technology has been developed to provide commercial availability of high quality substrates. Development is ongoing to fabricate the active Si or strained Si and buried oxide (BOX) films as thin as 10 nm with good uniformity and low defectivity. Even though planar single gate UTB devices do not have as good scalability as double-gate devices, they offer the major advantage of full compatibility with planar CMOS processing. Undoped channels are desired in order to reduce random dopant fluctuation effects for improving Vt variation as shown in Fig. 3 [10] and to improve low-field mobility. While vertical isolation from the substrate is provided by the BOX, various lateral isolation schemes for ultra thin films may provide additional density benefits. The applicability of existing techniques for mobility enhancement used in planar bulk or PDSOI technologies can provide additional boost in thin film devices. Currently, most of these techniques are based on process-induced strain obtained from a contact etch stop layer (CESL), raised SiGe in the S/D regions, or Stress Memorization Technique (SMT). Substrate-induced strain techniques, not yet widely used in today's technologies, can also provide additional boost in thin film devices.

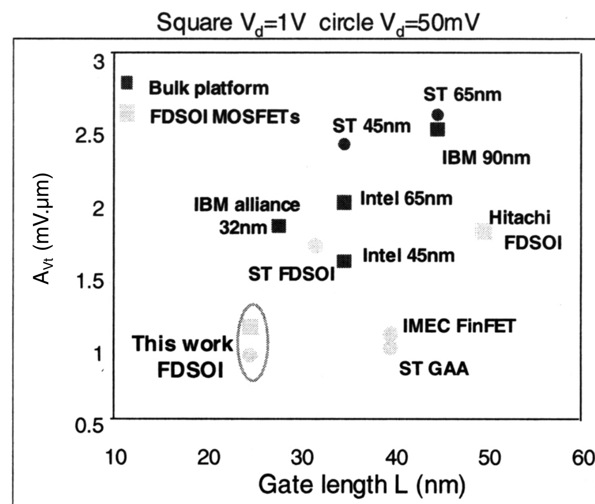

Figure. 3: Published Avt comparison of the FDSOI vs. Bulk transistors [10]

CONCLUSIONS

To meet high performance (HP) and low power (LP) circuit requirements, increased channel mobility is required to boost the transistor drive current and/or reduce Vdd for lower power dissipation without performance penalty. SOI and more advanced engineered substrates developed on the SOI platform provide solutions for technology nodes of 32 nm and beyond. The options include process-induced strain, biaxial strain virtual substrates, modification of surface and channel orientation, or selection of channel materials with high mobility and high saturation velocities such as Ge, SiGe alloys, and III/V compound semiconductors.

The ultra-thin-body SOI devices with undoped and strained channels can be used to control the SCE and reduce the sub-threshold leakage for scaling and low power dissipation. Such fully depleted devices promise excellent performance at very low power, a critically important attribute for the rapidly growing realm of portable consumer electronics.

This brief overview of SOI applications has focused on "more Moore" applications. In fact the SOI substrates enable a broad spectrum of technologies that are used in many conventional areas of electronics, beyond microprocessors, like smart power, and high voltage because they offer better performance. In addition, SOI enables some unique applications that would be very difficult if not impossible in bulk Si, such as RF devices in high resistivity substrates, ultra-thin RFID chips, backside imagers, MEMS, photonic integrated circuits, and flexible electronics. For a recent review see [12].

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