Waferlevel Vacuum Packaged Microscanners: A High Yield Fabrication Process for Mobile Applications

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ABSTRACT

Packaging of MEMS is an important expense factor within the production costs and, to ensure mass producibility, the packaging has to be performed on a waferlevel. While for inertial MEMS this is state of the art, it has not yet been reported for scanning micromirrors. Therefore, Fraunhofer ISIT has developed a process technology based on two 30 µm thick epitaxially deposited polysilicon layers for the manufacturing of waferlevel vacuum packaged MEMS scanning mirrors. It allows the fabrication of vertically stacked combdrives for out-of-plane mirror operation and a low damping environment for the reduction of needed driving signals. An anodically bonded structured glass wafer seals the devices at the front side, while an Au-Si eutectically bonded silicon wafer with an integrated 400 nm thick Ti getter layer is used to seal the devices from the backside. The measurement of the quality factor allows the estimation of the internal cavity pressure of sealed devices, which is in the range of 10^{-3} mbar. Waferlevel measurements showed that the fabrication process reaches a high mechanical yield of Y_m = 95%. Vacuum packaged devices needed 6V driving voltage to reach a total optical scan angle of above 50°.

Index Terms: microscanner, vacuum, waferbonding, quality factor, laserdisplay.

1. INTRODUCTION

Scanning micromirrors are promising candidates for a broad range of different mobile projection and imaging applications, such as compact laser based microdisplays for the integration in mobile phones and PDA's, or miniaturized LIDAR devices for object detection in cars.

As to the fact that these MOEMS (Micro Optical Electro-Mechanical Systems) devices are made for mobile use, they have to withstand even harsh environmental conditions, such as dust and change in temperature as well as humidity while power consumption must be kept low to guarantee an acceptable battery lifetime. For inertial MEMS, like gyroscopes and accelerometers, this is established by hermetic encapsulation on waferlevel [1, 2]. Therefore, a silicon wafer with several microns deep cavities is bonded on top of a MEMS wafer by standard waferbonding technologies (anodic, eutectic, or glass frit bonding). Subsequent to the waferbonding a dicing process separates the dies [2]. Waferlevel packaging not only protects sensitive MEMS devices, it also gives the ability to guarantee a vacuum environment, which reduces air damping and thus increases the amplitude of resonating MEMS actuators.

However, in the case of MOEMS devices, specifically microscanners, a waferlevel vacuum encapsulation is a big challenge. In this case, light has to be transmitted through the package onto the mirror plate. Due to reflection on the mirror it passes the package a second time before it reaches the projection area. Thus, the package must possess perfect optical quality to minimize image errors due to light beam distortion.

Besides the optical requirement, the scanners must meet extraordinary high mechanical requirements. For example, the optical resolution of laser projection systems based on scanning micromirrors mainly depends on the mirror plate diameter D, the mechanical scan angle of the mirror plate _ and the scan frequencies f_{res} (see Table I) [3, 4].

For example, to project images with a standard display format (e.g. VGA), a scanner with a typical mirror plate diameter of D = 1mm must be operated at a frequency of at least f_{res} = 15.7 kHz and at the same time must reach a mechanical scan angle of Θ = 7.5 deg.

Table I. Mechanical scanner requirements for different video resolutions [3,4].

Display Format	**VGA**	**SVGA**	**SXGA**
Horizontal Pixel Number	640	800	1280
Vertical Pixel Number	400	600	1024
Horizontal Scan Frequency (Hz) at 60 Hz Refresh Rate	15700	19200	32000
∪D (°mm)	7.5	9.37	15

Especially with respect to the product ΘD a further requirement regarding the waferlevel MOEMS package can be made. The distance from the surface of the glass wafer to the moving structure must be large enough to allow the desired mirror scan angle. Hence, for a maximum mechanical scan angle of +15° and a length of the moving mirror structure (containing mirror plate, driving fingers and an optional mounting frame) of 2 mm related to the axis of rotation, a distance between the surface of the MEMS wafer and optical window of 480 µm is needed.

2. FABRICATION TECHNOLOGY

The use of the scanners in mass markets requires that the fabrication technology for the scanner and the hermetic vacuum package is mass producible. This can only be ensured by waferbonding processes. The successful implementation of a waferlevel package for scanning micromirrors does not only comprise wafer-bonding technologies. Even more important is that the implementation has to dedicate the whole process integration of the MOEMS wafer to this goal as well.

Standard waferbonding processes only work with a few combinations of materials, which are optimized for the case that one wafer provides a silicon surface [5]. For instance, gold-silicon eutectic bonding needs a silicon and a gold interface provided by different wafers to form a low melting eutectic alloy [6]. Anodic bonding joins a silicon and a glass wafer [7, 8]. Hence, to have access to most of the waferbonding technologies the fabrication technology has to provide silicon sealing surfaces. Moreover, these silicon surfaces should have little to no topography in order to maintain hermeticity.

The fabrication of the scanner devices can be divided into two parts. The first part is the fabrication technology of the MOEMS devices itself while in subsequent processing sequences wafers for the waferlevel package are fabricated.

A. Scanner Fabrication

The scanner fabrication technology for electrostatically driven scanning micromirrors is bridging the gap between bulk and surface micromachining while being loosely based on state of the art MEMS technologies which use thick epitaxially deposited polysilicon layers and high rate aniso-tropic dry etch processes to structure these layers [8].

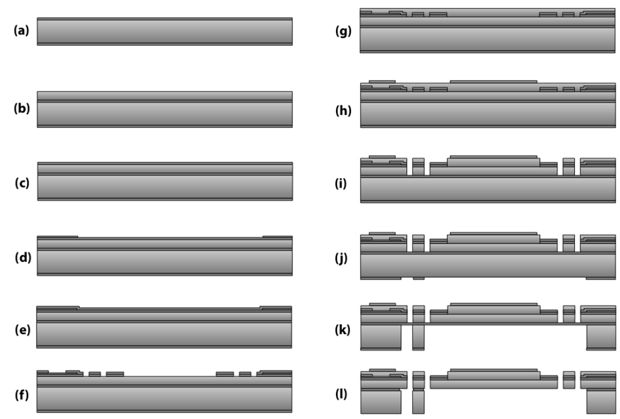

Figure 1. Schematic of the processflow for the wafer containing the mirror devices.

Featuring two 30 µm thick epitaxially deposited polysilicon layers, the main processing takes place on the wafer front side while this completely defines the mirror structure. The processing of the backside of the wafer mainly consists of a DRIE step excavating the mirrors from the back.

Figure 1 shows a schematic of the fabrication process flow for the device wafer in a cross-sectional view. A 6” n-type silicon wafer polished on front and back side serves as substrate material. In a first process step the wafers are cleaned and thermally oxidized (a). On top of this 1 µm thick oxide, a 190 nm thin polysilicon layer is deposited by a LPCVD process. This film serves as a starting layer for the subsequent deposition of the first epitaxial polysilicon layer (b) with a thickness of about 35 µm. Due to the inherent high roughness of epitaxially grown layers the wafers are polished in a chemical-mechanical planarization (CMP) process resulting in a 30 µm thick silicon layer with minimum topography. The next step is the deposition of a 1.2 µm thick LPCVD silicon oxide layer (c) and, on top of it, a 500 nm thin polysilicon layer, which serves later on as a buried interconnection layer. A lithography and a dry etch step structure the silicon layer (d). Next, a second 1.2 µm thick silicon oxide layer is deposited (e) and structured together with the previous oxide layer (f). This opens contact holes to the interconnection layer and the epi-polysilicon layer beneath. A second 35 µm epitaxial polysilicon layer with a previously deposited 190 nm thick starting layer is placed on top of this stack. Like the previous one, this layer has to be polished via CMP (g). Subsequently, a 100 nm thin metal layer, such as aluminum or silver, is deposited on top of the silicon surface, which enhances the reflectivity of the mirror plate and serves as metallization of the contact pads used for wire bonding (h). Thereafter, a DRIE process defines the outline of the structure while the buried oxide layers serve as a hardmask for the first thick silicon layer (i). This marks the end of the processing of the wafer's front side. After turning the wafers, a DRIE step exposes the backside of the mirror devices (j,k). The remaining thermal oxide layer generated at the process beginning is removed by a HF vapor phase etch process, which finally allows the free movement of the devices (l).

By the use of two 30 μm thick epitaxial polysilicon layers from which the lower one can be nearly independently structured via the buried hard mask, it becomes possible to generate two-level silicon planes. Thus, the height of the combdrives used for electrostatic actuation can be fabricated in a staggered manner (Fig. 2). These staggered combdrives not only allow resonant operation of the mirror plate, but also quasistatic out-of-plane movements, which broaden the range of applications. Additionally, staggered planes open up the ability to design suspension beams with two different thicknesses expanding the range of possible resonance frequencies.

The deformation of the mirror plate has a great impact on the laser beam distortion and thus on the image quality. By structuring the buried oxide and silicon layers it is possible to fabricate a mirror plate consisting of 60 microns of polysilicon without any intermediate layers, which could induce stress and would lead to undesired static deformation of the mirror plate. Interferometric measurements showed that the radius of curvature r of a scanner with a mirror diameter of D = 1mm is r ≈ 7m. Lateral feedthroughs formed by the buried interconnection layer made of LPCVD silicon in between the two thick silicon layers conduct electrical potentials into the cavity, which are used for driving and position detection of the scanner without losing hermeticity.

B. Wafer-Level Package

The surface of the front and back side of the wafer containing the micromirrors consists of silicon and thus provides the possibility to apply a variety of wafer bonding processes. The sealing area at the front side possesses a flat and topography less bond frame of epitaxially grown and polished silicon under which lateral feedthroughs conduct the electrical potentials. After removing the thermal oxide by HF vapor phase etching the polished substrate material of mono crystalline silicon is laid open.

As the fragile microstructure is exposed from the front and back side, it must be sealed from both sides in order to form a hermetic cavity. Hence, the front side has to be joined with a transparent cover wafer with a suitable wafer bonding process while another wafer seals the back side. It must be pointed out, that the wafer bonding processes must not influence one another. For example, if both wafers are successively joined by eutectic bonding, the bond of the first wafer could loosen during the joining process of the second wafer. For this reason, the transparent cover wafer is joined with the front side of the mirror wafer by anodic bonding. This bonding technology joins a thermally matched glass wafer (e.g. Pyrex) with a silicon wafer resulting in a chemical bond, which does not break even at elevated temperature. The wafer bonding is performed in SÜSS SB6 anodic waferbonder. Typical bonding parameters (temperature T, voltage V) during anodic bonding were T=500°C and V=600V.

After this, a second wafer with a gold metallization reinforced by electroplating is eutectically bonded on the backside of the mirror wafer. This waferbond is also performed in a SÜSS SB6 waferbonder. During waferbonding, the wafers are heated above the eutectic temperature T_{eut} = 363°C of the

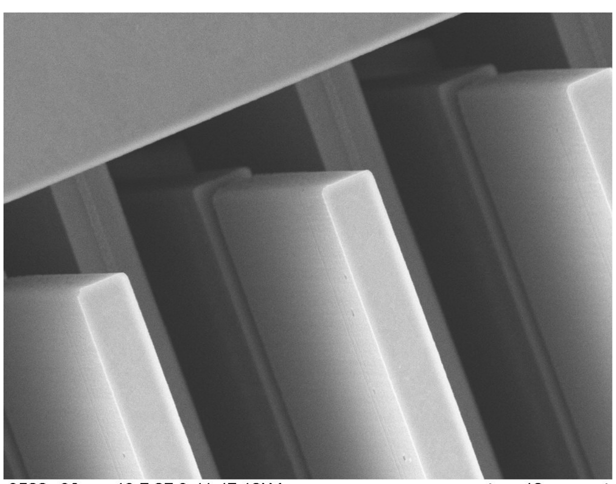

Figure 2: SEM image of a stacked combdrive used for electrostatic actuation of the scanner.

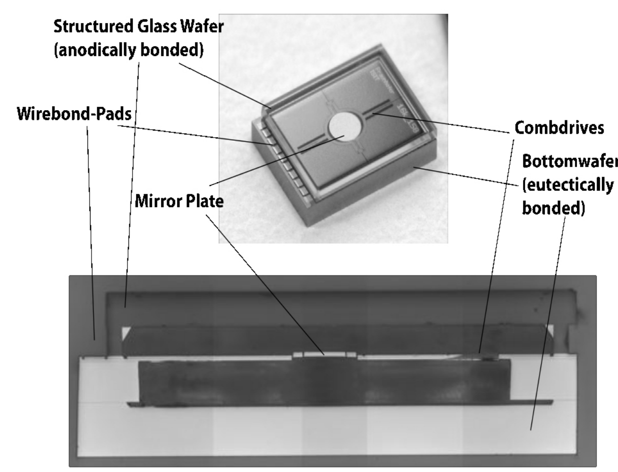

Figure 3. Cross section and photo of the final MEMS scanner package.

Au-Si eutectic alloy (typically T_{Bond} = 400°C) and are pressed together with a typical pressure of P_{Bond} = 5 bar. This second wafer also incorporates a 400 nm thick titanium getter layer, which is needed to guarantee a vacuum environment within the package. The elevated process temperature during the eutectic waferbonding activates the getter layer, which will absorb desorbed gas atoms during the eutectic bonding process by chemisorption. A first dicing step exposes the metalized contact pads for waferlevel testing and a second dicing step separates the dies. A complete microscanner can be seen in Fig. 3.

C. Fabrication of the structured Glass Cover Wafer

The fabrication of the glass cover wafer is carried out by casting a silicon wafer mold (Fig. 4)[9]. At first, trenches are etched into a bare silicon wafer by deep reactive ion etching (a, b). This structured silicon wafer is then joined by anodic bonding in a vacuum environment with a glass wafer (c).

Subsequently, the wafer stack is heated above the glass transition temperature (T_G = 530° for Borofloat glass). The glass wafer starts to flow into the trenches of the silicon wafer until they are completely filled with glass (d) and in this manner casting the negative pattern of the silicon wafer. After this glass flow process the remaining glass surface is deformed particularly in the surroundings of the trenches and at the wafer edge. A following grinding and polishing step smoothens the glass surface and removes the silicon wafer until the casted glass area is uncovered and polished (f). During a wet etch step the silicon in the cavities is removed (f) resulting in the final structured glass wafer.

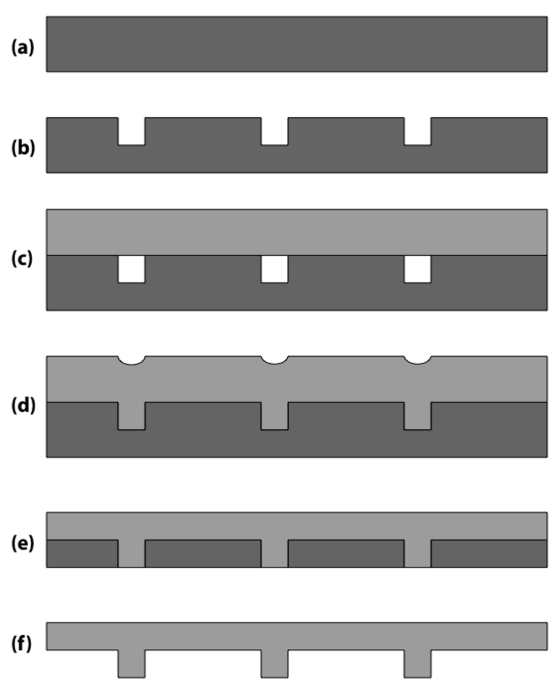

Figure 4. Schematic of the process flow of the structured glass wafer.

3. MEASUREMENTS ON VACUUM PACKAGED DEVICES

A resonantly driven microscanner can be regarded as a damped harmonic oscillator. The quality factor Q of this oscillator can be defined by [10]:

$$Q = \frac{\omega_0}{2\delta} \tag{1}$$

where ω_0 is the angular resonance frequency of the device and δ is the damping coefficient, which describes the exponential decay of the oscillation's amplitude in case of the absence of any external driving force. The quality factor also describes the increase in oscillation amplitude of a resonantly driven oscillator compared to the amplitude at static deflection.

The following measurements have been performed with two different types of 2D scanners with a mirror diameter of D = 1 mm and with different resonance frequencies (f_{res1} = 16.8 kHz, f_{res2} = 23 kHz). A more detailed description of the scanners can be found in [11].

A. Reference Curve

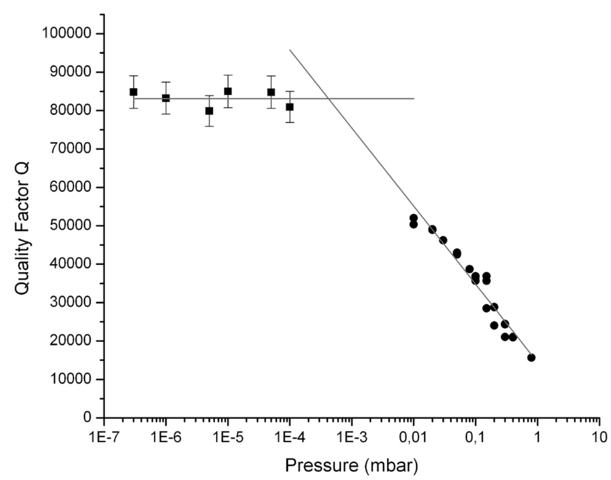

Figure 5. Reference curve (Q vs. pressure) used for estimation of the internal cavity pressure of the package.

Measuring the quality factor of unpackaged scanner devices at varied pressures delivers a reference curve (Fig. 5), which can be used to estimate the internal cavity pressure of sealed devices. For this, a single unpackaged scanner with a resonance frequency of f_{res} = 16.8 kHz has been placed in a vacuum chamber. The movement of the scanner was measured by directing laser light onto the actuated mirror plate and detecting the scanned beam with a PSD (Position Sensitive Device). The pressure of the vacuum chamber was varied from 1 mbar to $3*10^{-7}$ mbar.

Two parts determine the damping of the structure. Over a wide pressure range, the damping depends on the gas friction of the ambient atmosphere. Internal friction due to the deformation of the suspension beams generates an additional intrinsic damping. The quality factor increases with decreasing ambient pressure in case the extrinsic damping exceeds the intrinsic damping. If the ambient pressure is low enough so that the extrinsic damping no longer overweighs the intrinsic damping, a further decrease of the pressure does not increase the quality factor.

By extrapolation of the different data sets of the measurement it can be seen, that the transition region between extrinsic and intrinsic damping must be in the range of 10^{-3} mbar and 10^{-4} mbar. Below this pressure region, the device shows a constant quality factor of approximately $Q \approx 80.000$, while above this region the quality factor exponentially decreases with increasing pressure.

B. Measurements on Wafer Scale

Sealed MEMS wafers have been tested with a wafer prober. For this, a dicing step removes the glass above the metalized contact pads to contact the devices with the needles of a probe card. The probe card (Fig. 6) holds an optical fiber, which guides laser light over a beam splitter onto the mirror plate of the measured device. A PSD detects the scanned beam. The output voltage of the PSD correlates directly with deflection angle of the scanner.

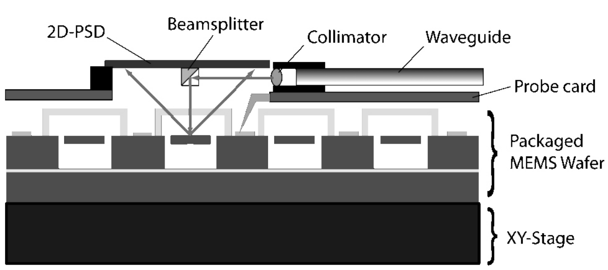

Figure 6. Schematic of the probe card for waferlevel testing of the packaged MEMS devices.

Figure 7 shows a histogram of quality factors of the measured devices. Approximately 75% of the measured devices exhibit a quality factor in the range of $Q \approx 80.000$. By comparing the measured values with the reference curve shows that the quality factor of the devices is not determined by gas friction but by intrinsic damping generated by the deformed suspension beams. Based on these measurements the corresponding internal cavity pressure is in the range of 10^{-3} mbar.

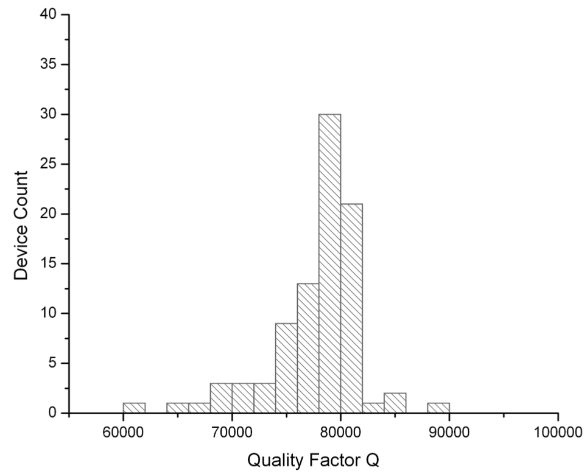

Figure 7. Histogram of the quality factor distribution of the packaged Wafer. Approx. 75% of the devices showed a quality factor of $Q \approx 80.000$.

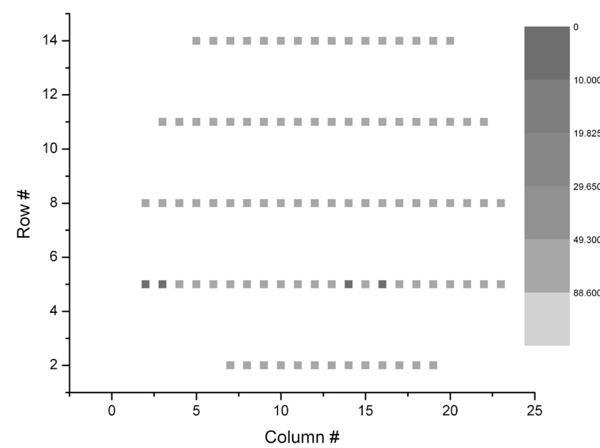

Figure 8. Wafermap of the quality factor of a waferlevel tested wafer. The process features a high mechanical yield of Y_m = 95%.

The wafer map of the quality factor (Fig. 8) allows the estimation of the mechanical yield of the process. A total of 93 devices have been measured and thereof only 4 devices showed a quality factor below $Q < 60.000$. This corresponds to a wafer yield of roughly $Y_m = 95\%$.

C. Driving Voltage

Further measurements have been carried out to evaluate the needed driving voltage for mirror actuation. Fig. 9 shows the dependence between total optical scan angle and driving voltage of a vacuum packaged scanner with a resonance frequency of 14 kHz. Due to the absence of gas damping, a total optical scan angle of above 50° can be reached even at a low driving voltage of about 6 V.

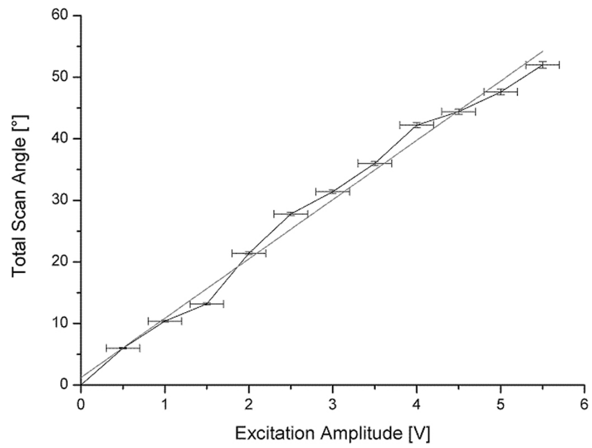

Figure 9. Dependence of the total optical scan angle with the excitation amplitude of a 14 kHz scanner.

4. CONCLUSIONS

A novel fabrication technology for waferlevel vacuum packaged scanning micromirrors has been developed and tested successfully. The technology is based on two epitaxially deposited polysilicon layers each with a thickness of 30 µm. Both sides of the fabricated MEMS wafer exhibit polished and flat silicon surfaces with no trenches, which enable the use of standard wafer bonding processes, such as anodic and Au-Si eutectic bonding. To allow a large mirror scan angle the wafer's front side must be sealed by a transparent glass wafer featuring deep cavities. Therefore, a process flow for the fabrication of glass cover wafers based on casting a silicon wafer mold has been presented. This glass wafer is joined with the MEMS wafer by anodic bonding. Subsequent Au-Si eutectic bonding of a second wafer with an integrated Ti getter layer seals the MEMS devices at the back side. The measured quality factor of $Q \approx 80.000$ of packaged scanners corresponding to a internal cavity pressure of approximately 10^{-3} mbar shows that the damping is not determined by gas damping but by intrinsic damping. Sealed devices reach total optical scan angles of above 50° at a very low driving voltage of about 6V. Measurements on wafer scale revealed the high mechanical yield of $Y_m = 95\%$.

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