Influence of Fin Shape and Temperature on Conventional and Strained MuGFETs' Analog Parameters

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ABSTRACT

This work evaluates two important technological variations of Triple-Gate FETs: the use of strained silicon and the occurrence of non-rectangular body cross-section. The anaysis is focused on the electrical parameters for analog applications, and covers a temperature range from 150 K to 400 K. The comparison of the intrinsic voltage gain between the different trapezoidal fin shapes showed that the fin shape can have a major role in some analog parameters than the use of the strained silicon technology, helping to improve those parameters under certain circumstances. The highest intrinsic voltage gains were obtained for strained devices with top fin width larger than bottom at low temperature. Besides the intrinsic voltage gain, were also studied: the threshold voltage, subthreshold swing, drain induced barrier lowering, channel resistance, total harmonic distortion, transconductance, transconductance to drain current ratio, output conductance, Early voltage, drain voltage saturation and unity gain frequency.

Index Terms: Strain, Non-Rectangular Fin, SOI MuGFET, Low Temperature.

INTRODUCTION

Multiple-gate MOSFETs (MuGFETs) are being considered for the future technologic nodes, as they present some advantages over more conventional devices, considering the continuous increase in performance requirements [1,2]. Besides de transistor architecture, some material improvements, as the use of mechanical stress [4], and environmental conditions, like the reduction of temperature [3] can be used to boost even more the device performance. The fabrication process of MuGFETs includes some etching steps for the formation of silicon fins. Due to technological problems in these steps, it is very usual the occurrence of some fin width variations along the vertical direction, leading on most cases to nearly trapezoidal, non-rectangular, cross-sections [5]. Some previous works [6,7,8] showed some consequences of these shape variations at room temperature.

The triple-gate FET is a MuGFET structure that has a great potential for analog applications and there are some works dealing with numerical simulated MuGFETs at low temperature with concave fin shapes [9] and experimental measurements on strained MuGFETs at low temperature [10] but a more complete study of trapezoidal MuGFETs under uniaxial stress and variable temperatures is not available until now.

Two different channel shapes are compared in this work, through three-dimensional numeric simulation, with strained and non-strained devices, under temperatures ranging from 150 K to 400 K.

SIMULATION DETAILS

The studied devices are fully depleted triple-gate MuGFETs, as presented in figure 1. Two cross-section shapes are proposed to be studied, both trapezoidal, one with top fin width of W_{Top} = 10 nm and bottom fin width of W_{Bottom} = 30 nm (named here as *regular trapezium*) and the other with opposite dimensions, W_{Top} = 30 nm and W_{Bottom} = 10 nm (named here as *inverse trapezium*). The average fin width (i.e. the width at the half height of the fin) of both devices is exactly the same and equal to 20 nm, and also the cross-section areas are the same for both devices. The use of same area and average width simplify the comparison between them. Common to all

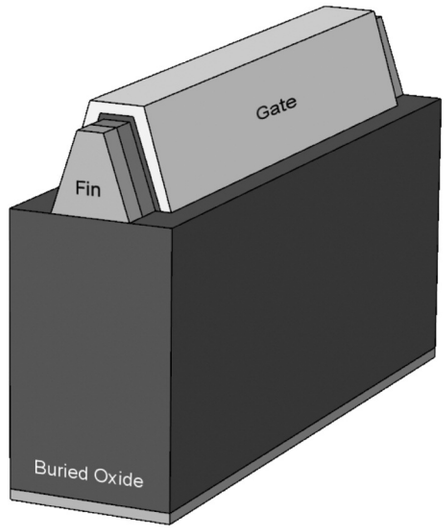

Figure 1. Simulated triple-gate MuGFET device.

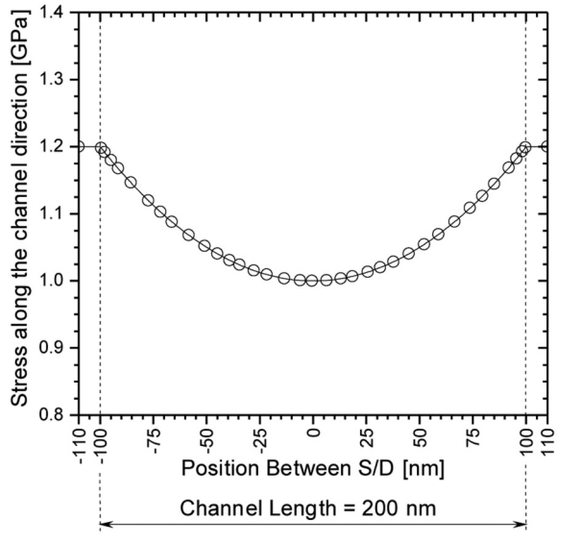

Figure 2. Uniaxial stress profile applied along the channel length.

devices, are the fin height of H_{Fin} = 30 nm, the gate oxide thickness of 2 nm, the channel length equal to L = 200 nm and buried-oxide thickness of 100 nm. The doping concentration is equal to $N_A = 10^{15}$ cm^{-3}, for all devices.

The uniaxial tensile stress profile presented in [11] is implemented in the device channel. The piezoresistive changes are implemented in the simulator to describe the strain effects on device operation. These changes are accounted by:

- The deformation of potential model, where strains are considered sufficciently small to the change in energy of each carrier, caused by the deformation of the lattice, being a linear function of the strain;
- The effective masses and effective Density-of-States (DOS), where the effective mass is a function of the temperature-dependent band gap;
- The strain-induced mobility model, through which Boltzmann statistics are assumed.

The uniaxial stress is applied along the channel length, as presented in figure 2, with the maximum value of 1.2 GPa at source/drain interfaces and decaying in the direction of the center of the channel, reaching the level of 1 GPa. The simulated device temperature ranges from 150 K to 400 K, allowing the study of the combination of the use of strained silicon channel with temperature reduction on trapezoidal MuGFETs.

The shape factor defined by equation (1) can be obtained by calculating the total width of the silicon / gate-oxide interface and dividing this by the channel length (L).

Simulations are conducted using the 3D Sentaurus Device numerical simulator, using the Shockley-Read-Hall and Auger recombination models, along with parallel and transversal electric field-dependent mobility model. For the linear region, a drain bias of V_{DS} = 50 mV is applied, for the saturation region V_{DS} = 600 mV. The gate voltage overdrive ($V_{GT} = V_{GS} - V_{th}$, V_{GS} is the applied gate voltage and V_{th} the threshold voltage) chosen is 200 mV, allowing the study of the devices operating in the saturation regime.

$$\frac{W}{L} = \frac{W_{top} + \sqrt{4H_{Fin}{}^2 + \left(W_{Top} - W_{Bottom}\right)^2}}{L} \qquad (1)$$

THRESHOLD VOLTAGE, SUBTHRESHOLD SWING AND DRAIN INDUCED BARRIER LOWERING

The maximum transconductance change method [12] is used for the threshold voltage extraction. This method establishes that the threshold voltage corresponds to the peak of the second derivative of the I_{DS} *vs* V_{GS} curve. For the threshold voltage extractions, the drain bias is V_{DS} = 50 mV. The second order derivative of drain current as a function of the gate bias is presented in figure 3.

With the reduction of the temperature, the peak of the second order derivative rises. Higher peak means larger variation of transconductance near the threshold voltage, with less gradual and faster switching between "on" and "off" states. The threshold voltage increased linearly with the reduction of temperature, at a ratio near -0.6 mV/K for both shapes, with a minor difference of ratio between conventional and strained devices. The increase of V_{th} with the reduction of the temperature is known from literature and is proportional to the variation of Fermi potential, with the temperature [13]. The applied stress led to

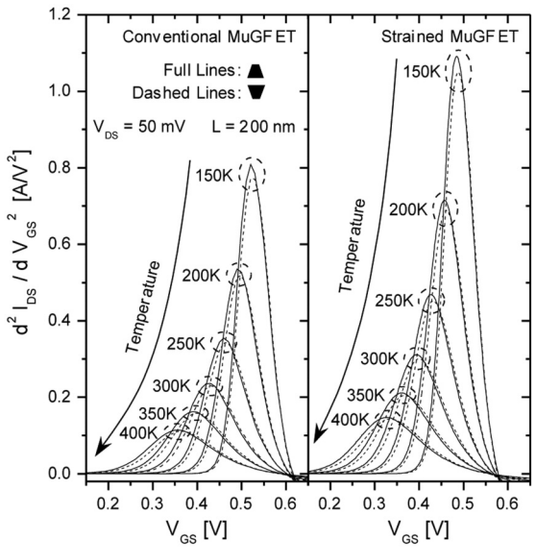

Figure 3. Plot of second order derivative of drain current for conventional and strained devices.

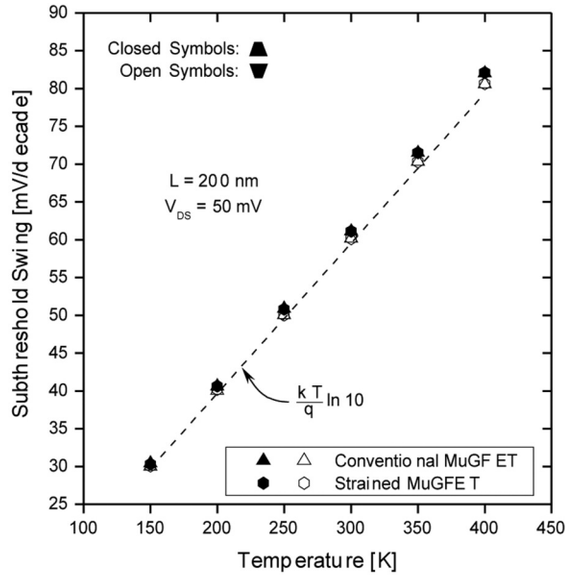

Figure 4. Subthreshold Swing as a function of temperature.

lower V_{th} when compared to the conventional MuGFET. The threshold voltage reduction with the strain application ranges from 30 mV at 400 K to 37 mV at 150 K and is related to the modification of the allowed energy levels of the carriers, and consequent band-gap repositioning. Table I presents the threshold voltage values obtained for conventional and strained devices for all analyzed temperatures.

The subthreshold swing is an important parameter for describing the drain current characteristics in subthreshold region and transition region, widely used to study the device susceptibility to short channel effects, is also extracted and showed in figure 4. Closed symbols represent the regular trapezium and open symbols represent the inverse trapezium. The subthreshold swing presents weak dependence on both the fin shape and strain technology, keeping its value near the theoretical limit of $(k \cdot T/q)\ln(10)$ with the temperature reduction [13].

Table I. Threshold voltage values for conventional and strained MuGFETs

	Threshold Voltage [V]			
	Conventional MuGFET		Strained MuGFET	
Temperature [K]	Regular Trap.	Inverse Trap.	Regular Trap.	Inverse Trap.
150	0.52	0.52	0.48	0.49
200	0.49	0.50	0.46	0.46
250	0.46	0.46	0.43	0.43
300	0.43	0.43	0.39	0.40
350	0.40	0.40	0.36	0.37
400	0.36	0.36	0.33	0.33

The Drain Induced Barrier Lowering (DIBL) parameter is defined as the shift in the threshold voltage divided by the increment in the drain bias, defined in equation (2). It measures how vulnerable is the control of the gate over the channel charges as the drain bias is raised. The DIBL was obtained from I_{DS} vs V_{GS} curves at drain bias of 50 mV and 600 mV.

$$DIBL = \frac{V_{th}(V_{DS1}) - V_{th}(V_{DS2})}{V_{DS2} - V_{DS1}} \qquad (2)$$

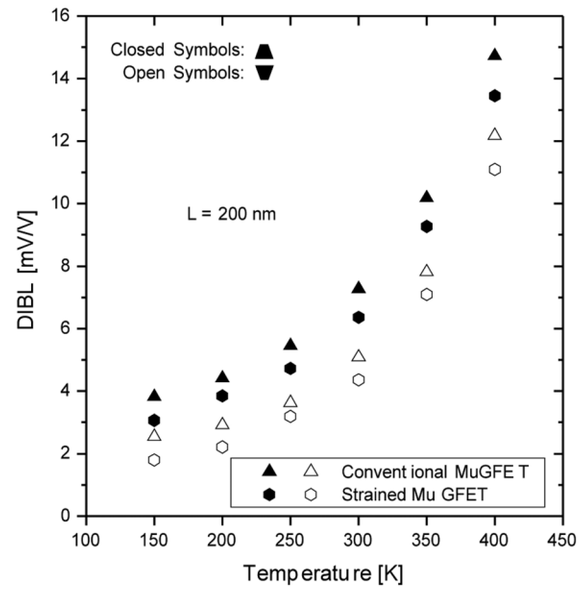

Figure 5. Drain Induced Barrier Lowering as a function of temperature.

Devices with the inverse trapezium shape present lower DIBL values as the gates have better electrostatic control of channel charges due to the stronger coupling of the gates. The reduction of temperature was beneficial for the reduction of DIBL effect, following a similar trend on both shapes and technologies. There is a small reduction in the difference between regular and inverse trapezium shapes as the temperature is reduced and an even smaller variation of values with the use of stress.

CHANNEL RESISTANCE

The simulated channel resistance behavior as a function of the temperature is observed in figure 6, at the gate overdrive voltage bias equal to 200 mV, extracted following the method described in [14]. As expected, the temperature reduction causes a channel resistance decrease. The influence of the channel shape is lower than the influence of the strain, for the used stress levels and trapezium angle. These influences are uniform over the whole studied range.

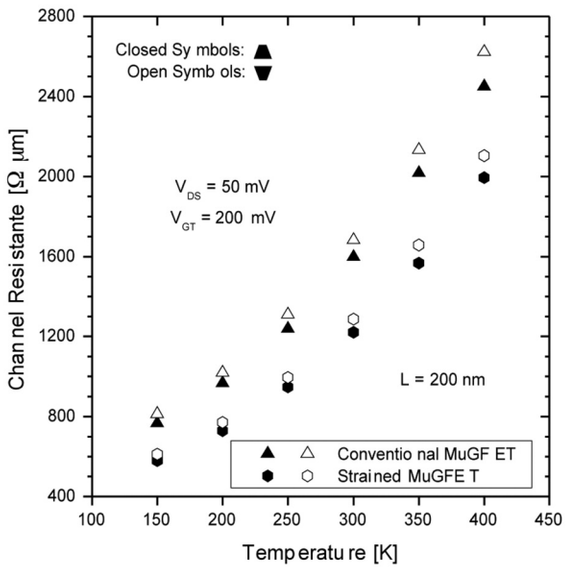

Figure 6. Channel Resistance as a function of temperature.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD), in figure 7, was calculated in order to evaluate the linearity of the output current as a function of the gate voltage, in saturation region. THD was calculated using the Integral Function Method (IFM), according to procedure described in [15].

The drain voltage was fixed in 600 mV and the DC gate voltage bias ranged from 0 to 1.2 V. The AC input amplitude was considered to be 0.2V.

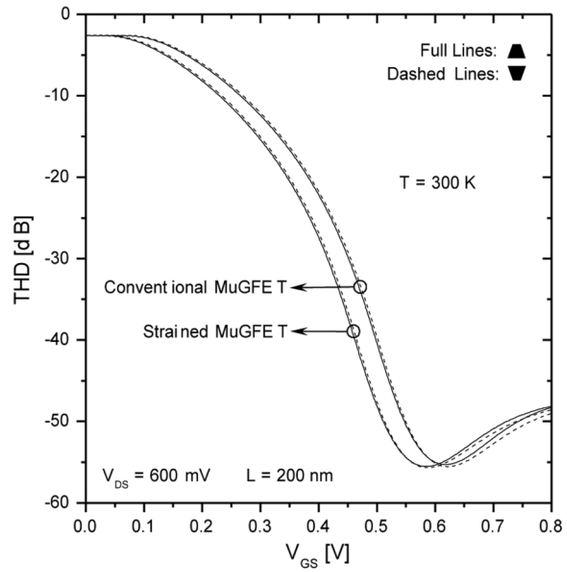

Figure 7. Total Harmonic Distortion for both conventional and strained MuGFETs.

Although the minimum distortion level was almost the same for all devices, about 60 dB, a 3 to 5 dB lower THD is observed for the strained devices in the input range from 0.4 to 0.8V. Thus, the strained devices offer a better linearity in a wide input range with a better current drive. The cross-section shape is of minor importance than the use of strained silicon. The curves for the studied shapes are close one to another, both for strained and non strained devices.

TRANSCONDUCTANCE

The transconductance curves may be observed in figure 8. These curves are obtained from the first order derivative of I_{DS} *vs* V_{GS} curve, with drain bias of 50 mV. The transconductance relates the drain current variation to the gate voltage, and presents some dependence with the fin shape, due to changes in the coupling of the channel charges to the gate and to the substrate. This dependence becomes more evident with the reduction of the temperature. The variation in g_m caused by the variation of fin shape is lower than the variation due to the appliance of stress. The stronger transconductance degradation after the point of maximum is observed. The enhancement of transconductance resulting from the applied strain varies from 28.3 % at 400 K up to 32.8 % at 150 K. The fin shape has a much lower influence than the use of strain. Table II presents the maximum transconductance values obtained for conventional and strained devices for all analyzed temperatures.

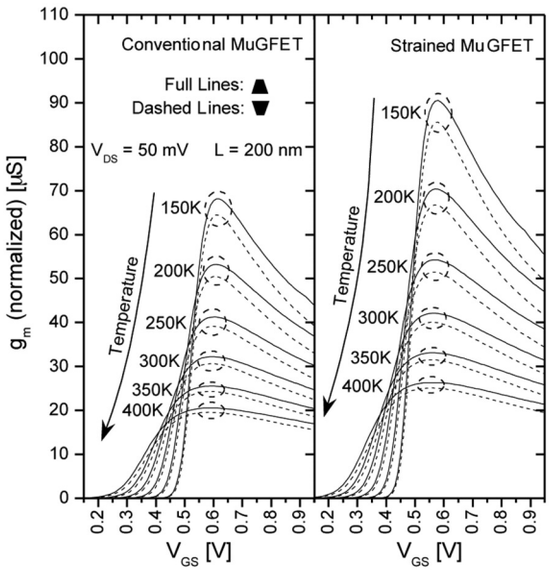

Figure 8. Transconductance curves ranging the temperature from 400 K down to 150 K for both conventional and strained MuGFETs.

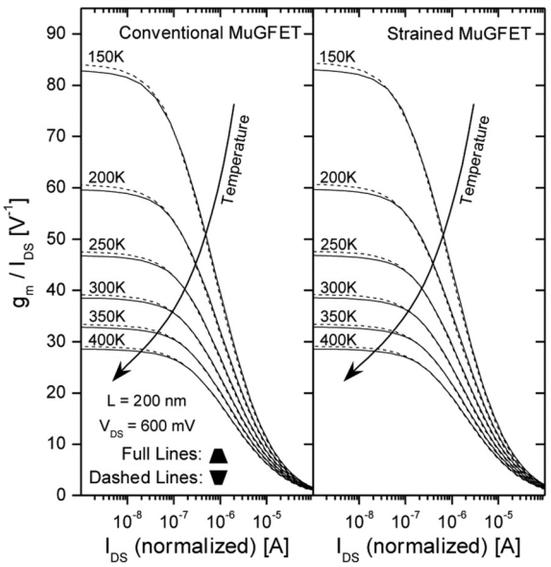

Figure 9. Transconductance to drain current ratio ranging the temperature from 400 K down to 150 K for both conventional and strained MuGFETs

Table II. Maximum transconductance values for conventional and strained MuGFETs.

	Maximum Transconductance [μS]			
	Conventional MuGFET		Strained MuGFET	
Temperature [K]	Regular Trap.	Inverse Trap.	Regular Trap.	Inverse Trap.
150	68.1	64.5	90.5	85.6
200	53.2	50.5	70.4	66.7
250	41.3	39.2	54.3	51.5
300	32.2	30.7	42.1	40.0
350	25.5	24.3	33.1	31.5
400	20.5	19.6	26.3	25.1

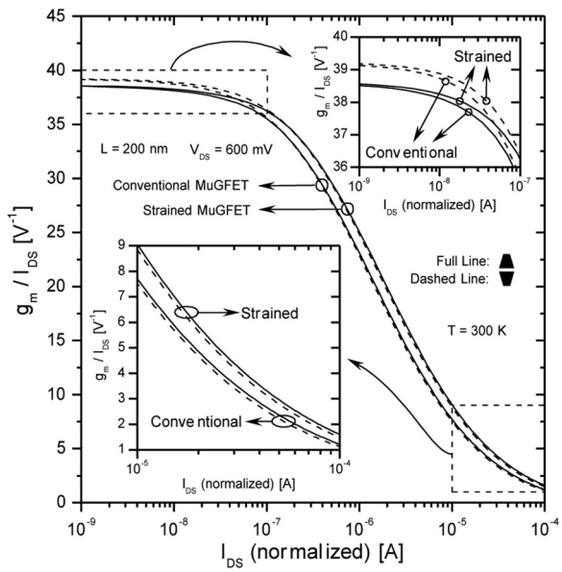

Figure 10. Transconductance to drain current ratio for the temperature of 300 K for both conventional and strained MuGFETs with zoomed details.

The transconductance to drain current ratio (g_m/I_{DS}), shown in figure 9, is evaluated for both shapes of fin and technologies (conventional and strained). Higher values are obtained for lower temperatures, with behaviors between conventional and strained devices that are similar. For clearness sake in the analysis that follows, figure 10 shows g_m/I_{DS} ratios on both technologies combined, for temperature of 300 K only.

The weak inversion region (zoomed in the upper right corner of the graph) is proportional to the subthreshold swing. Stated thus, inverse trapezium shapes have slight higher g_m/I_{DS} ratios (dashed lines) as a consequence of the lower subthreshold swing for these devices. The appliance of stress had negligible influence in this region, resembling the values obtained for conventional devices. On the strong inversion region (zoomed in the lower left corner of the graph) the g_m/I_{DS} ratio is proportional to the mobility of carriers. Higher ratios are present for strained devices and a reduction of shape and temperature dependence is also observed.

OUTPUT CONDUCTANCE, EARLY VOLTAGE AND DRAIN VOLTAGE SATURATION

The output conductance, normalized by the shape factor of equation (1), was obtained for gate overdrive voltage of V_{GT} = 200 mV. On both conventional and strained devices, the inverse trapezium has smaller values of g_d than the regular trapezium, and the difference increases as the drain bias is enlarged. The increase of temperature presented lower and better values. The fin shape led to variations on the output con-

ductance. This occurs because g_d is related to the channel susceptibility to the drain electric field, so as carriers in the inverse trapezium are better coupled to the gate, it suffers less influence from the potential originated at the drain junction, resulting on smaller output conductance values. Extracted at drain bias of 600 mV, the output conductance is presented as a function of temperature in figure 11. From this graph is observable the degradation of output conductance with the reduction of temperature for both fin shapes. A slight higher degradation rate for strained devices is also present. A similar variation on the magnitude of g_d by changing the fin shape and applying of strain is observed. On all cases, the use of strain degraded g_d performance. Comparing conventional to strained devices that have the same fin shape showed an increase from 19.2 % at 400 K up to 24.9 % at 150 K for the regular trapezium. For the inverse trapezium an increase from 15.5 % at 400 K up to 20.5 % at 150 K occurred, a significative lower variation for the latter.

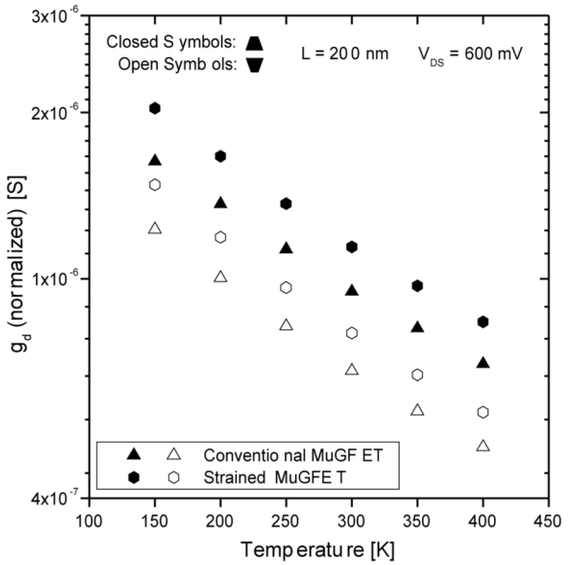

Figure 11. Output Conductance as a function of the temperature extracted at V_{DS} = 600 mV.

The Early voltage (V_{EA}), extracted for gate overdrive voltage of 200 mV, drain bias of 600 mV and for all range of temperatures, is plotted in figure 12. The inverse trapezium shape, that possesses narrower bottom fin width, has the best V_{EA} values for all temperature range. This occurs by reducing the electric field coming from the drain that penetrates inside the channel by reinforcing the electrostatic coupling between the gate walls. Comparing regular to inverse trapezium devices, the variation of Early voltage with temperature reduction is near half for inverse trapezium shape, maintaining a more stable trend. When comparing conventional to strained devices, strained devices have the highest V_{EA} values, although the higher g_d values. This unusual

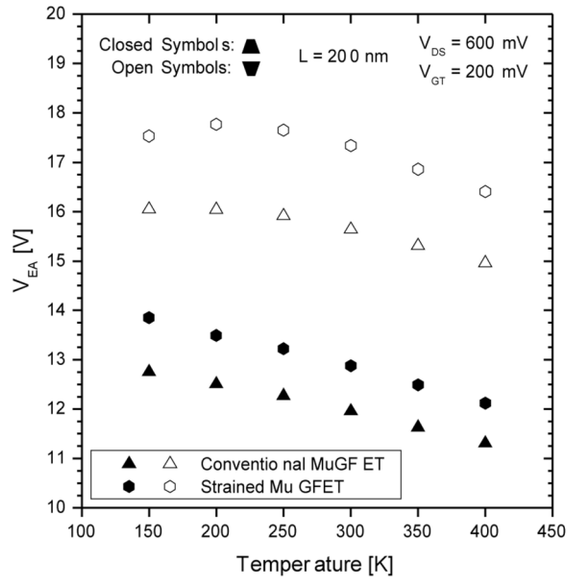

Figure 12. Early Voltage as a function of the temperature.

behavior occurs because the increment in the drain current by the use of stress is greater than the degradation suffered by g_d, resulting in higher Early voltages.

The drain voltage at which the device enters into the saturation region ($V_{DS.SAT}$) is also extracted and presented in figure 13, as a function of the temperature. The method used for extracting $V_{DS.SAT}$ was proposed by Jang *et al* [16]. This method is based on the general theory, being independent of specific MOS models and free of interference from extracted parameters. The values extracted correspond to the point where the velocity saturation begins (V_{DS} = $V_{DS.SAT}$). Above this point the effective channel length is a function of the

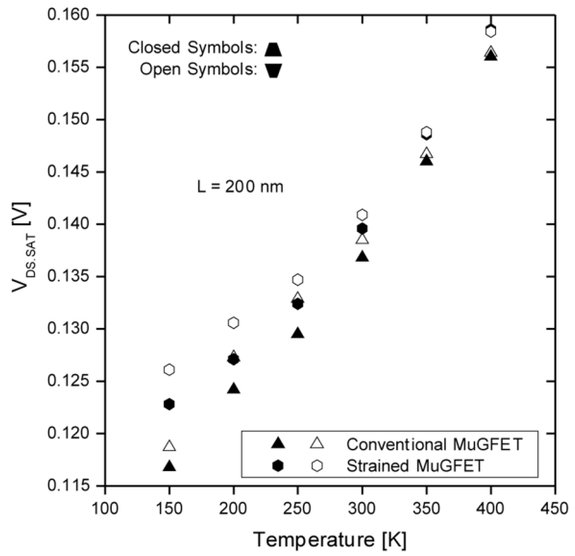

Figure 13. Drain voltage saturation in function of the temperature for conventional and strained MuGFETs.

applied drain bias, due to the channel length modulation. At high temperatures, the fin shape presents low importance, with a small larger $V_{DS.SAT}$ for strained devices. As the temperature is reduced down to 150 K, there is the reduction of $V_{DS.SAT}$ and the differentiation of values by fin shape and technology (conventional and strained). The first occurrence is well known from literature [3], as the threshold voltage increases with the temperature reduction.

The reduction of temperature increments the importance of the fin shape, with larger values for the inverse trapezium. Although strained devices present V_{th} smaller than conventional ones, larger $V_{DS.SAT}$ values are obtained for them, especially at lower temperatures.

INTRINSIC VOLTAGE GAIN

The intrinsic voltage gain is obtained from the relation between transconductance and output conductance ($A_V = g_m/g_d$), obtained with drain bias of 600 mV and gate overdrive voltage of 200 mV. Figure 14 shows the data obtained from this equation. The reduction of the temperature increased the carrier mobility, improving the transconductance, but the further decrease of temperature degraded the intrinsic voltage gain. The stronger degradation occurred for the inverse trapezium, compared to the regular trapezium, result of the slight higher degradation of g_d for this shape. The intrinsic voltage gain was improved by stress appliance 0.61 dB at 400 K and 0.51 dB at 150 K for the regular trapezium, and 0.85 dB at 400 K to 0.80 dB at 150 K for the inverse trapezium. A significative lower enhance for the first. The variation of fin shape led to a much higher variation in A_V than the strain application. If the conventional inverse trapezium device is compared to the strained regular trapezium, due to the inverse fin shape the conventional MuGFET presents a larger A_V of 1.97 dB at 400 K and 1.46 dB at 150 K, although the appliance of stress in the regular trapezium. The maximum A_V was obtained at 250 K for the regular trapezium and at 300 K for the inverse one, on both conventional and strained MuGFETs. After the point of maximum, A_V degrades for high temperature following a similar trend to the one observed for experimental rectangular MuGFETs in [10].

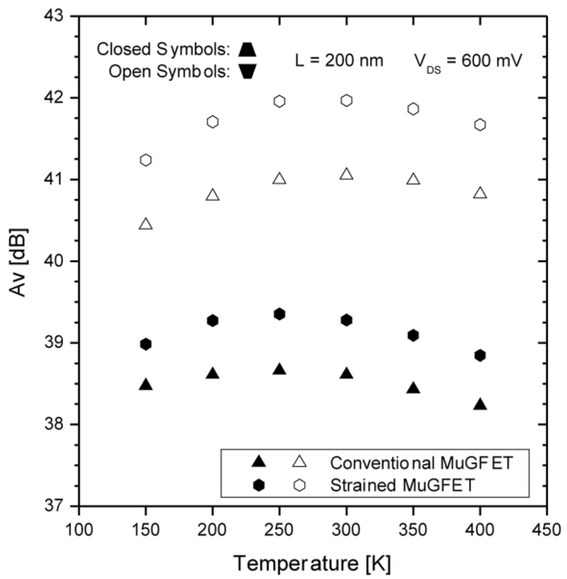

Figure 14. Intrinsic Voltage Gain in function of the temperature extracted at V_{DS} = 600 mV and V_{GT} = 200 mV for conventional and strained MuGFETs.

UNIT GAIN FREQUENCY

The unit gain frequency (f_T), extracted using equation (3), is known to be dependent on the shape of the fin and to follow a similar trend described by g_m [8,9]. Higher values of f_T are obtained reducing the temperature and for devices with the regular trapezium shape, as the unit gain frequency is inversely proportional to W and this shape has the shorter one. The appliance of stress improved the unity frequency gain over conventional devices on both fin shapes equally, from 27 % at 400 K up to 32 % at 150 K.

$$f_T = \frac{g_m}{2 \cdot \pi \left(\frac{2}{3} W \cdot L \cdot C_{ox} \right)} \qquad (3)$$

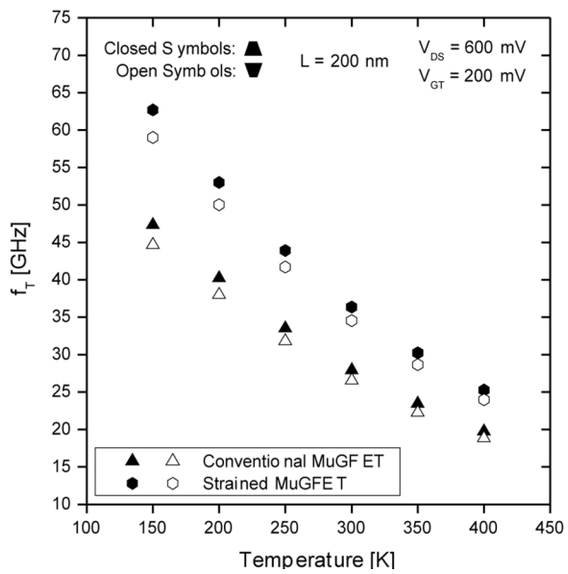

Figure 15. Unity Gain Frequency as a function of the temperature.

CONCLUSIONS

The influence of strained silicon, besides the occurrence of trapezoidal cross-section shape, in triple-gate FETs was analized for a wide temperature range. The effects of temperature reduction on some analog electrical parameters showed different intensities, depending on these device variations. Temperature decrease improves the transconductance, by increasing the carrier mobility, but although the intrinsic voltage gain degrades for lower temperatures due to the increase of the output conductance, the unity gain frequency improves. The inverse trapezium suffers a stronger decrease in the voltage gain than the regular trapezium, result of the slight higher output conductance degradation for this fin shape. The use of strained silicon boosted the voltage gain and unity gain frequency for all the studied devices and reduced the total harmonic distortion at room temperature, with the fin shape showing notably higher influence on voltage gain than on unity gain frequency or the total harmonic distortion.

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