Analog Performance of SOI nMuGFETs with Different TiN Gate Electrode Thickness and High-k Dielectrics

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ABSTRACT

This work presents an analysis of the analog performance of SOI MuGFET devices and the impact of different TiN metal gate electrode thickness. Thinner TiN metal gate allows achieving large gain and this effect can be attributed to the increased Early voltage values observed for thinner TiN metal gate. This V_{EA} increase suggests an increase of the transversal electrical field for thin TiN metal gate (reduced gate oxide thickness) that is confirmed with the increment of the GIDL current. This impact on the voltage gain is maintained for short channel length. The impact of different gate dielectrics was also studied where high-k dielectric indicated a higher V_T due to a V_{FB} variation. Additionally, lower intrinsic voltage gain was observed for hafnium dielectric and this can be related to the lower Early voltage (V_{EA}) present in this devices.

Index Terms: TiN**,** high k, analog performance, MuGFETs.

INTRODUCTION

Multiple gate structures (MuGFETs) are known to be one of the most promising alternatives in order to increase the transistor performance for sub 22nm technology nodes [1]. The higher electrostatic channel control due to the presence of more than one gate results in a reduced short-channel effect.

Additionally, the gate dielectric thickness has been a limitation for this scalability by an unacceptable increase of the gate leakage current [2]. As a result the integration of high-k dielectrics as gate insulator has been shown to be an alternative yielding a gate leakage current reduction [3]. The incorporation of nitrogen into these high-k materials can improve their thermal stability, reducing the dopant penetration and allowing further equivalent oxide thickness (EOT) scaling [4].

Alternative gate materials have also been studied to achieve a proper threshold voltage (V_T) setting in both n- and p-channel devices in high-performance CMOS applications [5]. Metal gate work function engineering has been shown an attractive technique for V_T engineering whereby the poly-Si gate material is replaced by metal gate electrodes [6-7]. For a MuGFET technology titanium nitride (TiN) has been widely studied, showing low resistivity and a mid gap work function for both transistor types [8-10]. This effective work function can be tuned by varying its thickness, although a thicker TiN metal gate introduces a higher interface trap density and a correspondingly lower mobility [11].

MuGFET structures also present an attractive behavior for analog applications with a reduced drain output conductance and an extremely large Early voltage value. Moreover, a quasi-ideal subthreshold slope and a better ratio between on-off current were also observed [12-16].

Based on that, the aim of this work is to investigate the analog performance of SOI MuGFETs with different TiN metal gate electrode thicknesses and high-k dielectrics.

EXPERIMENTAL

The SOI nMuGFETs under study have a 65 nm Si film on 150 nm buried oxide. Different gate dielectrics were considered: 1.9 nm SiON chemical oxide; 2 nm HfSiON (with an interfacial 1 nm chemical SiO_2 layer as a result of the cleaning process) and 1 nm ISSG (*in-situ* stream generated) SiO_2 with 2.3 nm HfSiO on top, where some devices were subjected to a thermal nitridation. For the TiN thickness, dif-

ferent splits were considered: 2 nm (64 ALD cycles), 5 nm (160 ALD cycles) and 10 nm (320 ALD cycles). TiN capped with 100 nm polysilicon was used as a gate electrode. More process details can be found elsewhere [17, 18].

EXPERIMENTAL RESULTS AND DISCUSSION

Effect of the different TiN metal gate thicknesses

In this section only the impact of the different TiN metal gate thickness was analyzed on MuGFET devices with ISSG SiO_2+HfSiO as gate oxide.

Figure 1 presents the threshold voltage (V_T) values extracted by the second derivative method [19]. The results are shown as a function of the channel length corresponding for the different process conditions. As can be seen, a thicker TiN metal gate implies a higher V_T. Additionally, the devices under study are not disturbed by the short channel effect for an effective channel length larger than L_{eff} ³ 400 nm for all TiN metal gate thicknesses studied.

The drain-induced barrier lowering DIBL was also extracted (Fig. 1) through the V_T variation in the linear (V_{T1}) and saturation (V_{T2}) region for V_{DS}=25mV and V_{DS}=1.2V. The V_{T2} was extracted using the current level related with V_{T1}. As expected, an increase in DIBL with reduced L_{eff} is observed, due to the drain bias influence on the potential barrier between source and channel. Thicker TiN metal gates present higher DIBL and this behavior is maintained and even more pronounced for short channel length (this is related with the smaller gate coupling resulting in an increase in V_T variations with drain bias). This behavior suggests a higher output conductance (g_D) for devices with thicker TiN metal gate.

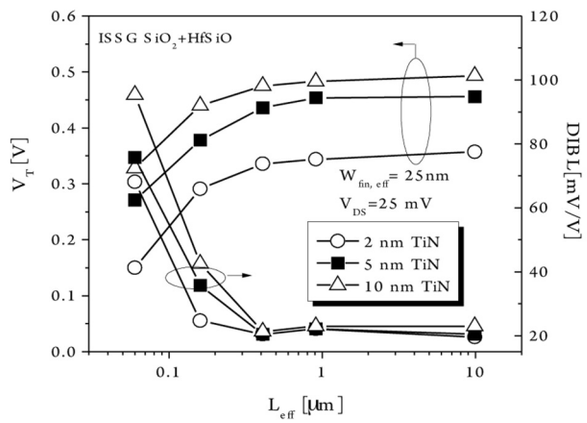

Figure 1. Extracted threshold voltage and DIBL as a function of the effective channel length for the different TiN metal gate thicknesses.

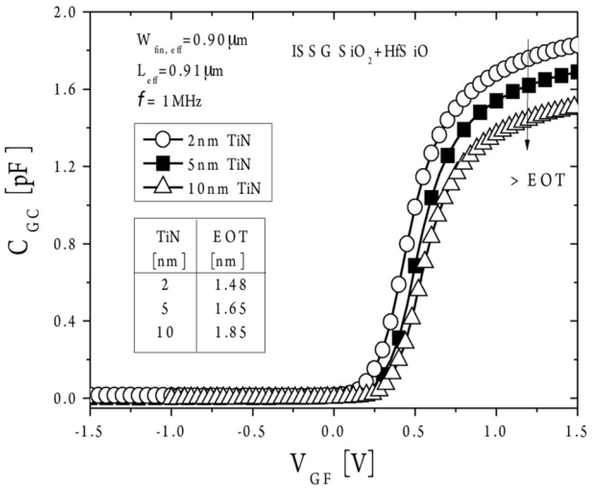

Figure 2. Gate to channel capacitance (C_{GC}) as a function of the gate voltage for different TiN metal gate thickness.

In order to explain this threshold voltage variation with the increase in the TiN metal gate thickness, the gate to channel capacitance (C_{GC}) as a function of the gate voltage curves was measured, enabling EOT extraction as presented in Fig. 2. Larger EOT (lower C_{GC}) is observed for thicker TiN metal gate (10 nm).

This phenomenon is related to a reaction between the higher concentration of oxygen atoms (O_2) (generated during the ALD process) and the interfacial layer (IL) re-growing during the spike annealing. The TEM picture of Fig. 3 clearly shows this IL increase [17,20].

Another important issue that we observed in our previous work [21] is an enhanced flatband voltage (V_{FB}) in devices with a thicker TiN metal gate. This phenomenon is related to a workfunction variation with the TiN metal gate thickness increase.

Figure 4 presents the drain current curve as a function of the gate voltage overdrive under saturation condition V_{DS}=1.2 V. The curve region under negative gate voltage is dominated by a component of the off-state leakage current, well-known as gate-induced drain leakage (GIDL) current [22]. From Fig. 4 it is possible to see that a thicker TiN metal gate results in a lower GIDL current.

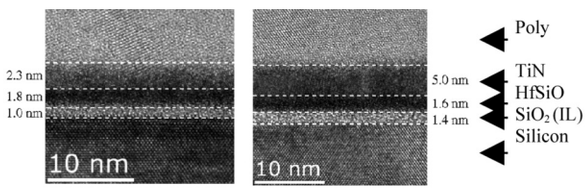

Figure 3. TEM picture for devices with a different TiN gate electrode thickness corresponding with (left) 2 nm and (right) 5 nm [17].

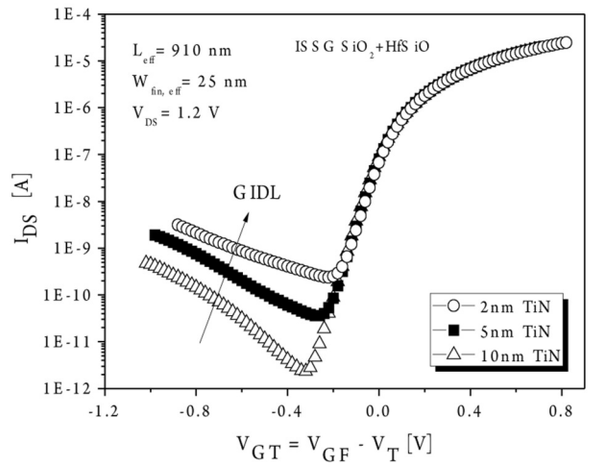

Figure 4. Drain current as a function of the V_{GF} - V_T for V_{DS}=1.2 V, L_{eff}=910 nm and different TiN metal gate thicknesses.

The GIDL current density can be modeled by equation (1) where A is a pre-exponential parameter, B (typically 23–70 MV/cm) is a physics-based exponential parameter and E_s is the transverse electric field at the surface [22]. Based on this it is clear to observe the impact of V_{FB} and T_{OX} on the transverse electric field. As discussed before, for an increase of the TiN metal gate thickness an increase of gate oxide thickness is observed and therefore a reduction of the gate capacitance. This variation in gate oxide thickness reduces the transversal electric field and as a consequence a lower GIDL current is observed for a thicker metal gate in Fig. 4.

$$J_{GIDL} = A \cdot E_s \cdot \exp(-B / E_s) \quad (1)$$

$$E_S = (V_{DG} - V_{FB} - 1.2)/(3 \cdot T_{OX}) \quad (2)$$

The electric field variation for devices with different TiN metal gate thickness can also be observed through the Early voltage (V_{EA}) values that are presented in Table I. V_{EA} was extracted at V_{DS} = 1.2 V and a gate voltage overdrive (V_{GT} =V_{GF}-V_T) of 200 mV on devices with different channel lengths and a narrow fin (W_{fin}=25 nm) ensuring a fully depleted operation. One can observe a reduction in the V_{EA} when the effective channel length shrinks as reported earlier for FinFET devices [13-14]. Furthermore, a thicker metal gate for the same L_{eff} leads to a reduction in V_{EA} and this behavior is in agreement with the larger DIBL (increased g_D) observed before. These observations can also be related to the increase of gate oxide thickness for a thicker metal gate that reduces the transversal electric field influence on the drain current, emphasizing more the horizontal electric field contribution and consequently decreasing V_{EA}.

Table I. V_{EA} extracted for the different TiN metal gate thicknesses and channel lengths

L_{eff} [µm]	2 nm TiN	5 nm TiN	10 nm TiN
9.91	2636.0	688.0	508.0
0.91	189.0	82.0	38.0
0.41	79.0	46.0	17.0
0.16	17.6	13.3	11.8
0.06	3.8	4.1	2.6

The impact of the effective channel length on the intrinsic gain (A_v=V_{EA}*g_m/I_{DS}) was also analyzed (Figure 5) showing a reduction with L_{eff} as expected. Higher A_V is observed for thinner TiN metal gate electrodes for the studied range of channel length.

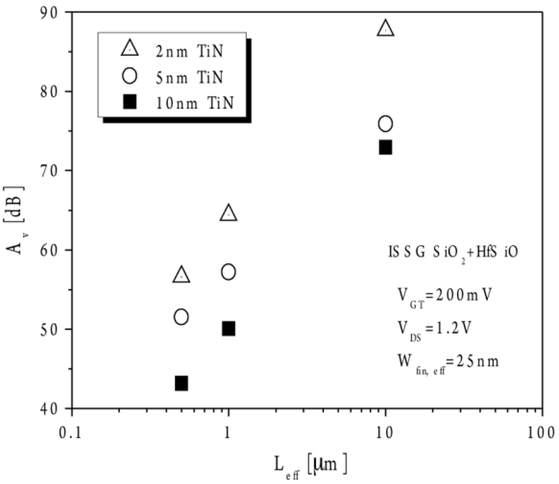

Figure 5. Calculated intrinsic gain as a function of the channel length for the different TiN gate electrode thicknesses at V_{DS}=1.2 V and V_{GT}=200 mV.

Effect of the different gate dielectric

This section presents an analysis of the analog behavior of MuGFET devices with different gate dielectric and 5 nm of TiN as metal gate deposited by MOCVD.

A summary of the V_T behavior is presented in Fig. 6 as a function of the effective channel width. Higher V_T is observed for the HfSiON dielectric and this is related with the increased V_{FB} [23] even for a reduced EOT, as shown in the inset of Fig. 6. This small EOT observed for HfSiON can be related to the larger dielectric constant observed for these devices [24].

The Early voltage (V_{EA}=I_D/g_D) was also extracted from the output conductance (g_D) at a gate voltage overdrive (V_{GT} =V_{GF} -V_T) of 200 mV for the different gate dielectrics and TiN deposited by MOCVD, as shown in Figure 7.

Reduced V_{EA} is observed for the hafnium dielectric and this phenomenon can be related to a smaller transverse electric field (Equation 2) influence on the drain current, emphasizing the horizontal electric field contribution. This lower E_S is related to the higher V_{FB} and slightly higher physical gate dielectric thickness

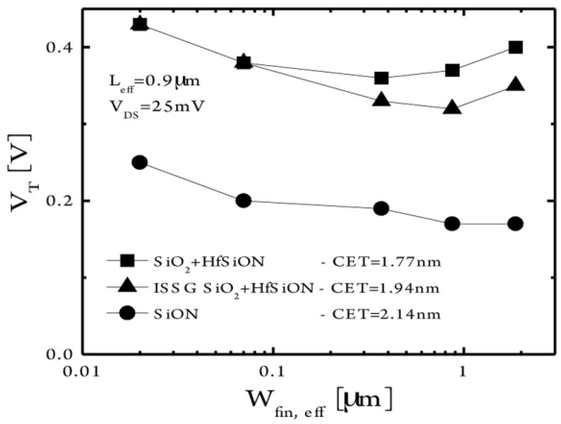

Figure 6. Threshold voltage as a function of W_{fin} for the different gate dielectrics.

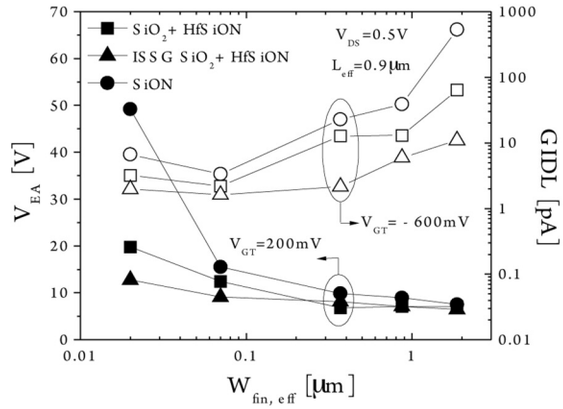

Figure 7. Extracted V_{EA} (V_{GT}=200mV) and GIDL (V_{GT}= - 600mV) as a function of W_{fin} for the different gate dielectric at V_{DS}=0.5V.

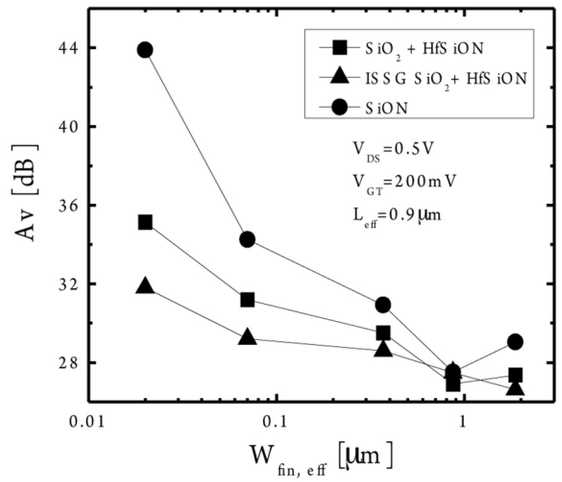

Figure 8. Calculated intrinsic gain as a function of W_{fin} for the different gate dielectrics at V_{DS}=0.5 V and V_{GT}=200 mV

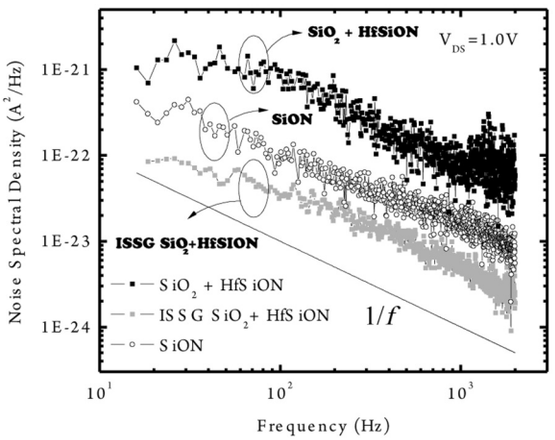

Figure 9. Noise spectral density versus frequency for the different gate dielectrics.

observed for the HfSiON (see note above) dielectric. This behavior can be seen in Fig. 7 through the gate-induced drain leakage (GIDL) current extracted at a saturation condition. As a result, lower GIDL is observed for a hafnium dielectric than for SiON. However, lower V_{EA} and GIDL are observed for the ISSG SiO_2+HfSiON gate stack when compared with the chemical SiO_2+HfSiON dielectric, but this is related to a higher gate oxide thickness for ISSG SiO_2+HfSiON.

Finally, the device intrinsic voltage gain (A_v=V_{EA}*g_m/I_{DS}) has been extracted and is presented as a function of the fin width at V_{DS}=0.5 V and V_{GT}=200 mV in strong inversion (Fig. 8). A SiON dielectric gives a higher A_V due to the increased V_{EA} and mobility (higher transconductance). For both hafnium dielectrics, even for the reduced transconductance observed for HfSiON, a higher A_V is seen thanks to the improved V_{EA}.

The noise spectra versus frequency (Fig. 9) are typically of the $1/f^{g}$ type for all the cases. It is clear that from a noise perspective the gate dielectric with ISSG SiO_2 as interfacial layer yields a lower noise.

CONCLUSIONS

In summary, we demonstrated that metal gate work function engineering by considering different TiN thicknesses can impact the analog performance of SOI nMuGFETs. It was shown that a thinner TiN metal gate results in a higher intrinsic gain mainly due to the larger Early voltage values. The reduced gate oxide thickness reported for thinner TiN resulted in a higher transverse electric field, causing a V_{EA} increase. This phenomenon can be verified through the GIDL current that showed an increase for reduced TiN metal gate thickness. Shorter channel lengths with thicker TiN presented a higher DIBL which resulted in a higher output conductance. Different gate dielectrics were also analyzed and a high-k dielectric showed a lower intrinsic voltage gain when compared with a SiON insulator. This was assigned to a lower V_{EA} obtained due to the higher V_{FB}. A dielectric with a silicon oxide as interfacial layer before the hafnium deposition presents the poorest gain but has a lower $1/f$ noise.

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