Analog Operation Temperature Dependence of nMOS Junctionless Transistors Focusing on Harmonic Distortion

Rodrigo T. Doria[1], Marcelo A. Pavanello[1,2], Renan D. Trevisoli[2], Michelly de Souza[1], Chi-Woo Lee[3], Isabelle Ferain[3], N. Dehdashti Akhavan[3], Ran Yan[3], Pedram Razavi[3], Ran Yu[3], Abhinav Kranti[3], and Jean-Pierre Colinge[3]

[1] Electrical Engineering Department, Centro Universitário da FEI, São Bernardo do Campo, Brazil
[2] LSI/PSI, University of Sao Paulo, Sao Paulo, Brazil
[3] Tyndall National Institute, University College Cork, Cork, Ireland
e-mail: rtdoria@fei.edu.br

ABSTRACT

This paper performs a comparative study of the analog performance of Junctionless Nanowire Transistors (JNTs) and classical Trigate inversion mode (IM) devices focusing on the harmonic distortion. The study has been carried out in the temperature range of 223 K up to 473 K. The non-linearity or harmonic distortion (HD) has been evaluated in terms of the total and the third order distortions (THD and HD3, respectively) at a fixed input bias and at a targeted output swing. Several parameters important for the HD evaluation have also been observed such as the transconductance to the drain current ratio (g_m/I_{DS}), the Early voltage (V_{EA}) and the intrinsic voltage gain (A_V). Trigate devices showed maximum A_V around room temperature whereas in JNTs the intrinsic voltage gain increases with the temperature. Due to the different A_V characteristics, Junctionless transistors present improved HD at higher temperatures whereas inversion mode Trigate devices show better HD properties at room temperature. When both devices are compared, Junctionless transistors present better THD and HD3 with respect to the IM Trigate devices.

Index Terms. Multiple Gate Transistor, Junctionless, Silicon-On-Insulator, Harmonic Distortion, Analog Operation.

INTRODUCTION

Planar MOS devices have become inadequate for nodes beyond 45 nm, due to the occurrence of short channel effects which induce a reduction of the gate control on the channel charge [1]. Thus, several alternative technologies have been developed aiming at the devices miniaturization. Multiple gate devices as FinFETs and Trigate FETs have shown to be strong candidates for future technologies. Such transistors are constituted by a silicon nanowire surrounded by gate material. These structures provide a significant improvement on the control of the channel charges. Nevertheless, as the channel length is reduced, the source and drain junctions to the channel have to be sharper to avoid the diffusion of impurities in the channel region. In devices of extremely reduced dimensions, the formation of ultra-sharp junctions becomes of high complexity since it requires extremely precise doping and thermal conditions. A novel structure, called Junctionless Nanowire Transistor (JNT), was recently proposed to avoid this problem [2].

Similarly to other multiple gate devices, the JNT is constituted by a nanowire surrounded by gate material. The outstanding characteristic of this device is related to its doping profile. The Junctionless presents a uniform heavy doping concentration, which is constant through source, channel and drain regions [2] and there is no formation of junctions eliminating the problem of the diffusion of impurities. The schematic view of a general multiple gate transistor is presented in Figure 1 (A) whereas the cross-sections of an nMOS inversion mode (IM) device and of an nMOS JNT are exhibited in Figures 1 (B) and 1 (C), respectively. Several advantages of the JNT over classical IM Trigate devices have been recently reported. Reference [3] describes the improvements in terms of subthreshold slope and DIBL whereas refs. [4-5] deal with the better analog performance of Junctionless devices. Also, the operation of JNTs at high temperatures is treated in [6] where it is shown that Junctionless devices present no "Zero Temperature Coefficient" (ZTC) in their I-V characteristics.

This paper investigates the analog parameters of JNTs as a function of the temperature focusing on their harmonic distortion (HD). The analog performance of JNTs is compared to the one of IM Trigate devices of similar dimensions. Section 2 describes the physical characteristics of the measured devices and presents the experimental results. In Section 3, the main analog parameters which influence the HD performance are evaluated. The harmonic distortion of JNTs and classical IM devices is addressed in Section 4 through the determination of the total and third order distortions (THD and HD3, respectively). Finally, the conclusions of this work are pointed out in Section 5.

DEVICES CHARACTERISTICS AND MEASUREMENTS

The devices measured along this work were fabricated according to the process described in [7]. Both IM Trigate devices and JNTs were fabricated on standard SOI wafers where the active layer was thinned down to 10~20 nm and patterned into nanowires through e-beam lithography. In the Junctionless transistor an N^+ ion implantation was performed just after the gate oxidation in order to uniformly dope the active region from source to drain with a concentration of $3x10^{19}$ cm^{-3}. In the IM devices, however, a P^+ ion implantation was performed only in the channel region to generate a doping concentration of $1x10^{18}$ cm^{-3}. The JNTs and IM devices were produced with P+ and N+ polysilicon gates, respectively. Thus, the threshold voltage (V_{TH}) of both devices could attain suitable values. The gate oxide and the silicon layer thicknesses (t_{ox} and t_{Si}, respectively) are equal to 10 nm. Devices with mask fin widths (W_{mask}) of 30 nm and 40 nm were produced. However, along the fabrication process these values are expected to be reduced by 15~20 nm. Due to the presence of a top and two sidewall gates the total channel width can be estimated as $W = 2.t_{Si} + W_{mask}$. All the devices present channel length (L) of 1 µm. The threshold voltage was extracted for both JNTs and IM devices according to the double derivative method described in [8]. At room temperature, the threshold voltage of JNTs with W_{mask} of 30 nm and 40 nm resulted in 0.39 V and 0.55 V, respectively whereas for IM devices with W_{mask} between 30 nm and 40 nm, V_{TH} resulted around 0.65 V.

Figure 2 shows measured I_{DS} curves as a function of the gate voltage (V_{GS}) and the gate overdrive voltage ($V_{GT} = V_{GS} - V_{TH}$) for both IM and JNTs at V_{DS} = 1.0 V and at temperatures ranging from 223 K to 473 K. As one can observe in Figure 2 (A), the ZTC point in Inversion-Mode transistors is clearly seen. It results from the concurrent reduction of V_{TH} and mobility with increased temperature. The higher dependence of V_{TH} on the temperature and the lower mobility degradation with temperature presented by Junctionless transistors (Figure 10 (B)) prevent JNTs from exhibiting a ZTC point. As can be seen in Figures 2 (C), IM Trigate transistors show a significant drain current decrease when temperature is

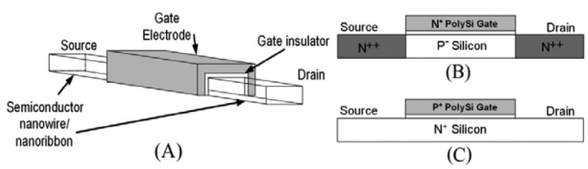


Figure 1. (A) Schematic view of a Multigate transistor, (B) cross-section of a classical Inversion Mode nMOS Trigate transistor and (C) cross-section of an nMOS Junctionless.

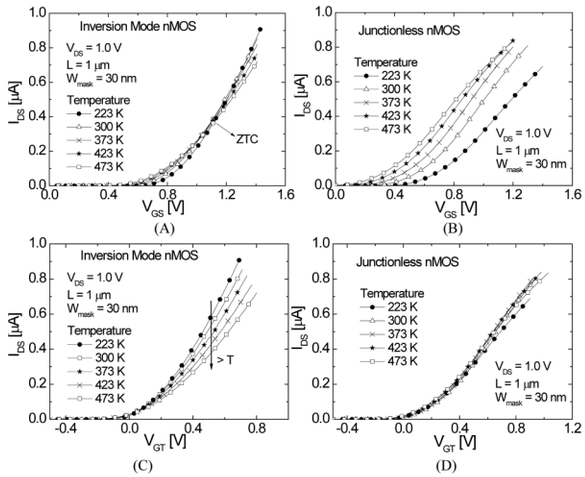


Figure 2. Measured (A) I_{DS} vs. V_{GS} for Inversion Mode nMOS Trigate, (B) I_{DS} vs. V_{GS} for nMOS Junctionless, (C) I_{DS} vs. V_{GT} (being $V_{GT} = V_{GS} - V_{TH}$) for Inversion Mode nMOS Trigate and (D) I_{DS} vs. V_{GT} for nMOS Junctionless at several temperatures.

increased, which can be mainly associated to mobility degradation. This strong mobility degradation observed for the IM devices agrees with the results presented in ref. [9] for triple-gate FETs. On the contrary, in Figure 2 (D), one can see that the mobility degradation with temperature is negligible in JNTs. Reference [6] attributes this behavior to the fact that mobility in JNTs is dominated by impurity scattering resulting from the higher doping concentration, and that the effect of phonon scattering is, in relative terms, much smaller than in devices with a lightly doped channel.

ANALOG PARAMETERS EVALUATION

Several analog parameters can be directly related to the HD performance of MOS transistors. As distortion analysis will be carried out when the devices are biased in saturation operating as single-transistor amplifiers, the more influent analog parameters will be verified in this condition. The transconductance over the drain current ratio (g_m/I_{DS}) is important for the present analysis since it indicates the inversion level of the devices guaranteeing that the JNTs and the IM Trigate devices are biased in a similar region of operation (weak, moderate or strong inversion). For this reason part of the HD evaluation will be performed as a function of g_m/I_{DS}. The curves of g_m/I_{DS} were extracted from the I–V curves exhibited in Figure 2 and have been presented in Figure 3 as a function of both $I_{DS}/(W/L)$ and V_{GT} for devices of W_{mask} = 30 nm.

In moderate and strong inversions IM transistors present larger g_m/I_{DS} than JNTs at a similar $I_{DS}/(W/L)$ as can be observed in Figure 3(A), which is associated with the higher mobility of IM devices

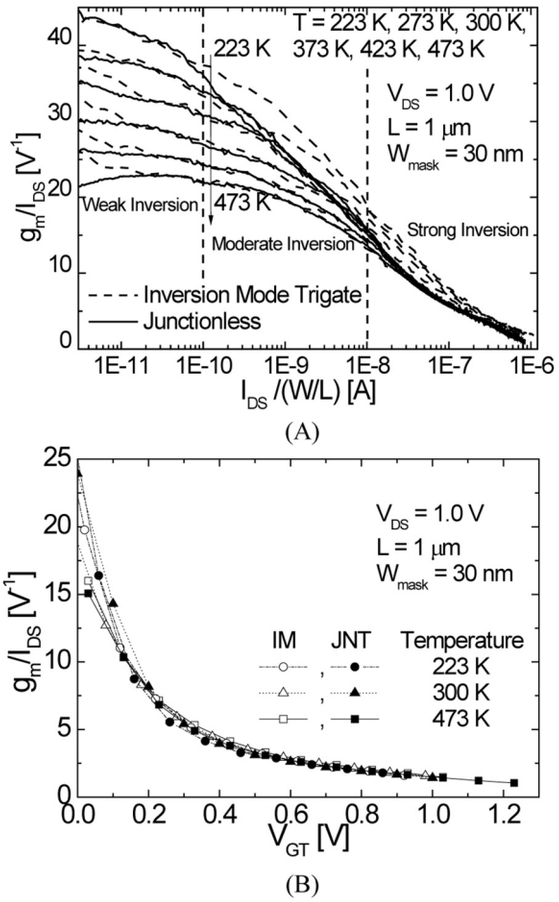


Figure 3. Curves of (A) g_m/I_{DS} *vs.* $I_{DS}/(W/L)$ and (B) g_m/I_{DS} *vs.* V_{GT} (V_{GT} = V_{GS} - V_{TH}) of measured Trigate and Junctionless devices at V_{DS} = 1.0 V for several temperatures.

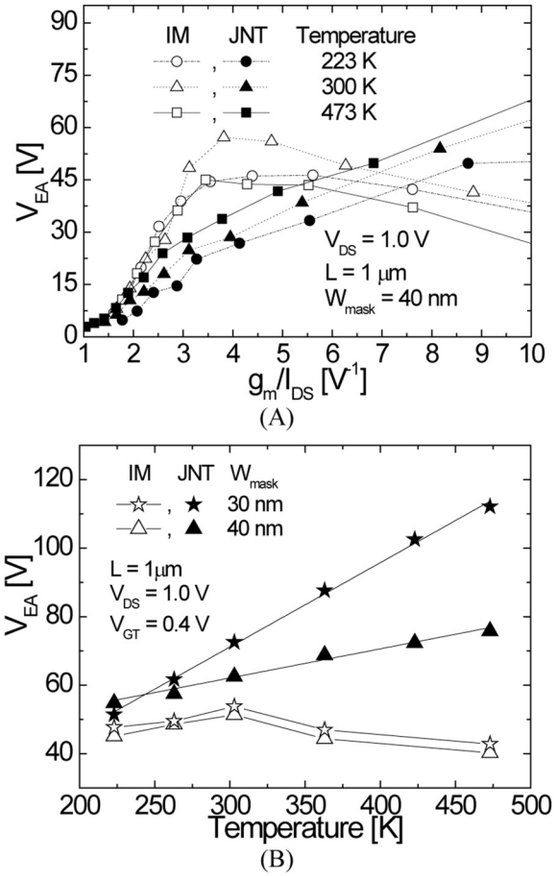


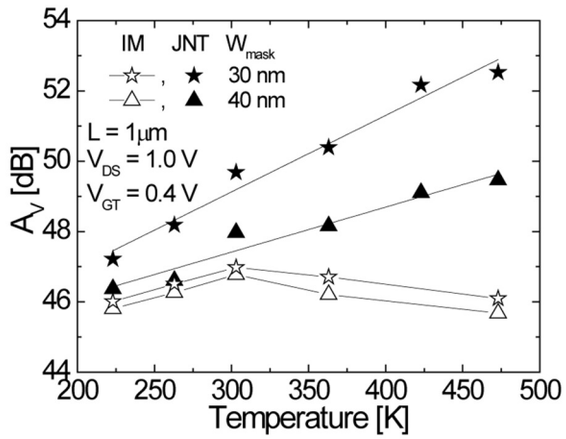
Figure 4. (A) Curves of V_{EA} *vs.* g_m/I_{DS} for measured IM devices and JNTs of W_{mask} = 40 nm and (B) V_{EA} *vs.* temperature for IM devices and JNTs of W_{mask} = 30 nm and 40 nm at V_{GT} = 0.4 V.

[5]. In these inversion levels, the influence of the temperature in g_m/I_{DS} is more pronounced in IM transistors in comparison to JNTs as stated in [4]. In weak inversion both devices present similar g_m/I_{DS} values which is mainly controlled by the body factor of the devices and is practically equal to the unit for both IM and Junctionless transistors. In Figure 3(B), it can be seen that JNTs and IM devices have similar efficiency for converting I_{DS} in g_m independently of the temperature.

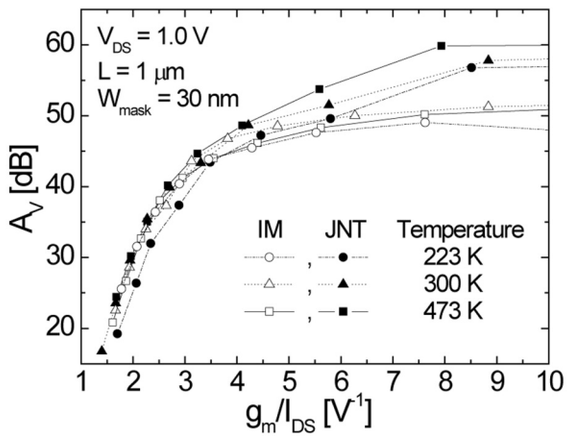
When combined with g_m/I_{DS}, the Early voltage (V_{EA}) indicates the intrinsic voltage gain (A_V) of the transistors as describes expression (1) [10]. The intrinsic voltage gain constitutes a fundamental parameter for analog applications as single transistor amplifiers and can affect the HD performance of the devices. The extracted V_{EA} has been exhibited in Figure 4 (A) at different temperatures for IM devices and JNTs of W_{mask} = 40 nm as a function of g_m/I_{DS}. In the present work, the analysis focuses on the strong inversion regime, i.e. g_m/I_{DS} < 10 V^{-1}. From these results one can note that Junctionless devices present an increase of V_{EA} with the temperature raise whereas IM devices exhibit maximum V_{EA} around 300 K for the entire g_m/I_{DS} range. These results agree to the ones described in reference [9] for triple gate FinFETs where the reduction of V_{EA} with the temperature increase is correlated to the higher mobility degradation. As stated in [5], JNTs are less sensitive to the mobility degradation at higher temperatures and V_{EA} present a monotonic increase with the temperature. For both devices, the reduction of V_{EA} with the temperature lowering is attributed to the increase of g_D due to the channel length modulation in both devices.

$$|A_V| = \frac{g_m}{g_D} = \left(\frac{g_m}{I_{DS}}\right) V_{EA} \quad (1)$$

In Figure 4 (B) Early voltage is plotted as a function of the temperature at a fixed V_{GT}. By comparing V_{EA} from devices of different W_{mask}, a reduction of the Early voltage is observed for wider devices. This effect is associated to the dependence of the W_{mask} on the characteristic length, which influences g_D and V_{EA} [11]. Indeed, in triple gate FinFETs, the parcel of V_{EA} due to the channel length modulation is inversely proportional to the characteristic length multiplied by the electrical field of the devices [11]. In



(A)



(B)

Figure 5. Curves of (A) A_V as a function of the temperature at V_{GT} = 0.4 V and (B) A_V *vs.* g_m/I_{DS} for measured IM devices and JNTs at V_{DS} = 1.0 V.

the JNT, the lower electrical field [12] can contribute for a stronger influence of the characteristic length in g_D, causing a larger degradation on V_{EA}.

The intrinsic voltage gain represents one of the most important parameters in several analog circuits such as amplifiers and has a strong impact in the harmonic distortion of the devices as it will be discussed in Section 4. A_V has been presented as a function of the temperature in Figure 5(A) for IM devices and JNTs at a fixed V_{GT}. Due to the correlation between V_{EA} and A_V, the maximum intrinsic voltage gain of IM devices is obtained at room temperature, whereas in Junctionless transistors A_V raises with the temperature similarly to the effect previously observed in V_{EA}. The A_V lowering with the temperature decrease is explained by the degradation of g_D due to the channel length modulation, whereas the gain degradation at higher temperatures in IM is associated to the mobility degradation. When devices of different W_{mask} are compared it is observed a similar tendency to the behavior observed for V_{EA} in Figure 4 with JNTs A_V presenting larger dependence on W_{mask} than IM devices.

The intrinsic gain is presented as a function of g_m/I_{DS} in Figure 5(B) for Inversion Mode Trigate devices and Junctionless transistors with W_{mask} = 30 nm. The A_V characteristics of both devices are presented for different temperatures and exhibit a similar shape along g_m/I_{DS}. A reduction of the intrinsic gain is observed at lower values of g_m/I_{DS} as the devices tend to change their operation region from saturation to triode and g_D exhibits an exponential behavior with the variation of g_m/I_{DS}. At larger g_m/I_{DS} JNTs present higher gain due to their improved g_D as previously mentioned.

HARMONIC DISTORTION EVALUATION

The non-linear I-V characteristics inherently obtained in MOS transistors can play a key role in several analog circuits fabricated for different purposes. Audio amplifiers, filters and AC/DC converters, for example, usually require the use of MOS devices with low distortion level to operate adequately. Despite several figures of merit can be used for the harmonic distortion analysis such as the interception voltage [13], along this work HD will be evaluated through the determination of the total and the third order harmonic distortions (THD and HD3, respectively). By observing simultaneously these two figures of merit, a satisfactory view of the distortion can be attained. THD is given by the sum of the distortions generated for all harmonics present in the output signal and, usually, can be essentially approximated by the second order distortion (HD2). Generally, harmonics of higher orders such as HD3 are extremely lower and can be neglected. HD3 only becomes the dominant non-linearity source in differential circuits where HD2 and the others even order harmonics are suppressed [14]. For the determination of the distortion, a mathematic algorithm called Integral Function Method (IFM) [15] was directly applied to the I_{DS}-V_{GT} characteristic of the transistor. This method allows for the extraction of HD2, HD3 and THD considering a sinusoidal input voltage bias of amplitude Va associated to V_{GT}. In this case, the gate to source voltage can be expressed as $V_{GS} = V_{GT} + Va.\sin(x)$, with x between 0 and 2π.

The curves of THD and HD3 are presented in Figure 6 for IM devices and JNTs of W_{mask} = 30 nm as a function of g_m/I_{DS}. HD was extracted for the devices biased in saturation at V_{DS} = 1 V for an input sinusoidal amplitude Va = 50 mV. According to the curves of THD in Figure 6 (A) both devices exhibit a similar distortion indicating that the total distortion presents no significant dependence on the devices type. Also, THD seems to be insensitive to the temperature. A study of the non-linearity exhibited by triple gate FinFETs showed that when such devices

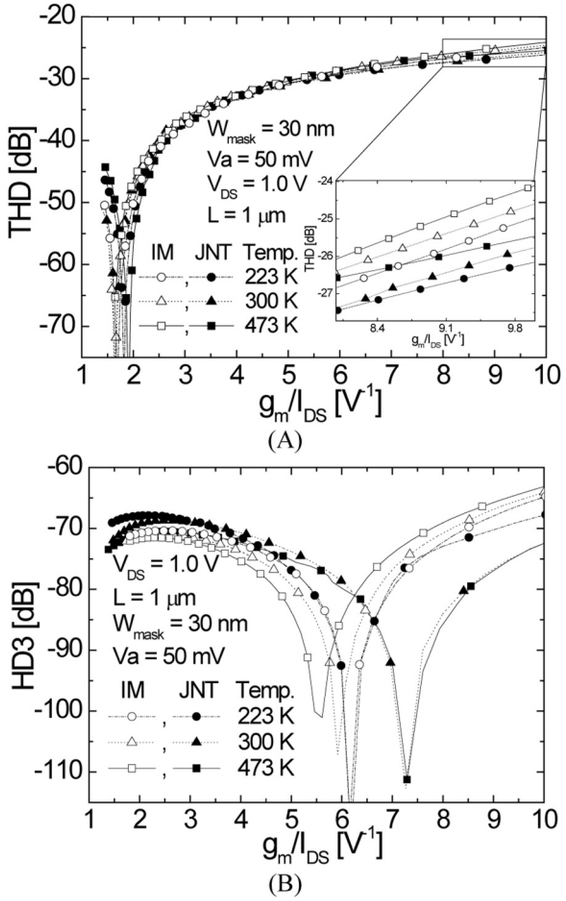


Figure 6. Curves of (A) THD *vs.* g_m/I_{DS} and (B) HD3 *vs.* g_m/I_{DS} for measured nMOS IM devices and JNTs at V_{DS} = 1.0 V for several temperatures.

operate as amplifiers THD can be described by HD2 which is substantially a function of the series resistance (R_S) and the mobility degradation factor (θ) [16]. It has been recently shown that the mobility degradation of Junctionless transistors is much less pronounced than in IM devices as a result of the reduced electric field perpendicular to the current flow [12]. On the other hand, the series resistance is expected to be higher in Junctionless nanowires with respect to IM Trigate devices as the source and drain doping concentrations of JNTs is in the order of 10^{19} cm^{-3} whereas in IM transistors the doping concentration of source and drain is superior to 10^{20} cm^{-3} which results a reduced R_S. For this reason, the lower mobility degradation of the JNTs in comparison to the IM devices is apparently compensated by their higher series resistance resulting in a similar THD. According to the insight of Figure 6 (A) Junctionless devices have a slightly better THD with respect to the IM device. When THD is observed for different temperatures, an inexpressive variation in the distortion is obtained. Anyway, the slight THD reduction at lower temperatures can be associated to the variation of the series resistance and the mobility degradation [16]. At $g_m/I_{DS} \approx 2$ V^{-1} linearity peaks are noted in the THD curves. These distortion minima are related with the bias in which the devices change their regime of operation from saturation to triode.

As expected, in the current analysis, HD3 is extremely lower than THD as presented in Figure 6 (B) where HD3 results in values smaller than -60 dB for both devices in the whole g_m/I_{DS} range. Considering that in Figure 6 (A) THD present values in the order of -25 dB it can be concluded that HD3 is not the dominant distortion component in a single transistor amplifier. The HD3 level observed in IM devices and JNTs is extremely similar and the main difference between the curves is the shift of the distortion minima along g_m/I_{DS}. According to [17], in planar MOSFETs the distortion minima can be related either to the bias where the predominant mobility degradation mechanism changes from phonon scattering to surface roughness or to the series resistance. Reference [16] states that, for triple gate FinFETs, the HD3 minima are associated to the change of the preponderant mobility degradation mechanism. In strong inversion (lower g_m/I_{DS}), the effective mobility is determined by the surface roughness whereas at larger g_m/I_{DS} the phonon scattering is the dominant factor. In the peaks region both effects acquire similar magnitude and the distortion generated by each mechanism is compensated by the other. This explanation remains valid for IM Trigate devices since the mobility-related phenomena are the same in FinFETs and Trigate transistors. However, the surface roughness is not supposed to play a significant role in JNTs since these devices present bulk conduction and the surface roughness should affect only devices where superficial conduction is dominant, as in the case of Inversion Mode transistors. For this reason, the linearity peaks in HD3 of JNTs are expected to be associated to their series resistance, which is higher than the one obtained in IM devices as already mentioned.

When the temperature is reduced, the HD3 level is barely affected, although a shift of the HD3 minima is observed along g_m/I_{DS}. In Inversion Mode transistors, the linearity peaks change their position to higher g_m/I_{DS} as the temperature is lowered. This effect is addressed for triple gate FinFETs in [18] where the shift of the peaks is attributed to the reduction of the phonon scattering with the temperate, indicating that at lower temperatures the surface roughness becomes effective in HD3 prevailing as the dominant mobility degradation mechanism at smaller V_{GT} (larger g_m/I_{DS}). Reference [19] confirms that in double gate FinFETs surface roughness prevails over phonon scattering as the main mobility degradation mechanism at low temperatures. In JNTs the linearity peaks move to smaller g_m/I_{DS} with the temperature reduction what could be related to the variation of the series resistance with the temperature.

In order to find out the real impact of R_S in the HD3 curves of the JNT, three-dimensional devices simulations were performed. The simulated devices present similar characteristics to the measured ones such as doping concentration, channel length, gate oxide and silicon film thicknesses. The fin width (W_{fin}) was set to 10 nm. Aiming at different series resistances, the source and drain contacts were made at the left and right sides of the device and JNTs with two different source/drain lengths were simulated. For a first analysis, the length of the source and the drain were set to 150 nm and the I_{DS}-V_{GS} curves were obtained at different temperatures. The simulations were performed using the Sentaurus tool [20] with the default simulator coefficients. Analytical models accounting for the mobility degradation due to vertical and lateral electrical fields, doping-dependent carrier lifetime, bandgap narrowing and density gradient quantization were included in the simulations.

Through the application of IFM, HD3 was extracted and is presented in Figure 7 as a function of g_m/I_{DS}. The simulated curves are in agreement to the experimental data, showing HD3 in the order of -60 dB and linearity peaks around g_m/I_{DS} = 5 V^{-1}, which are slightly shifted along g_m/I_{DS} with the temperature variation as showed in the insight of the figure. In the sequence, the extensions of source and drain were reduced to 10 nm and the structure was simulated at room temperature. HD3 was extracted without changing any other physical parameter and is also presented in Figure 7. In this new source/drain configuration the series resistance is expect to be reduced up to 15 times. Due to the R_S diminution, the distortion minima are shifted to significantly larger g_m/I_{DS} (around 17 V^{-1}), out of the region of interest for the operation in strong inversion. For g_m/I_{DS} between 1 V^{-1} and 10 V^{-1}, HD3 is kept practically constant confirming the correlation of the linearity peaks of HD3 in JNTs operating in strong inversion with the series resistance.

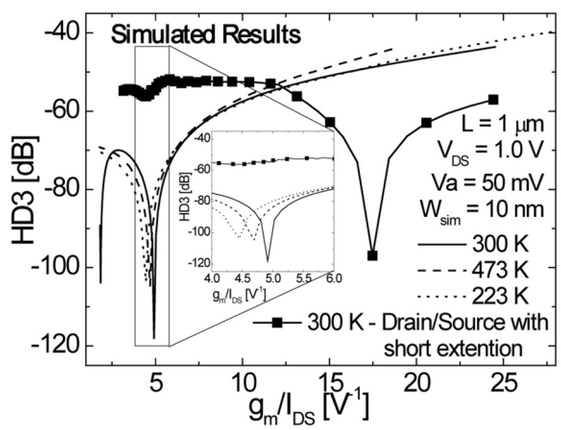


Figure 7. Simulated curves of HD3 *vs.* g_m/I_{DS} for JNTs at V_{DS} = 1.0 V for several temperatures (Va = 50 mV).

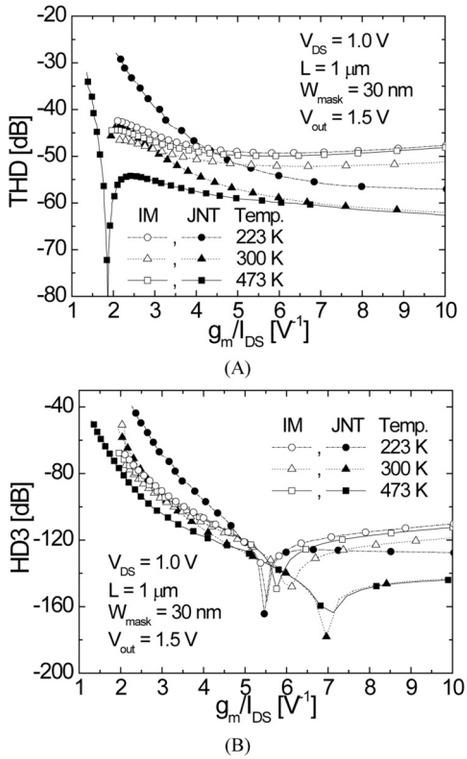


Figure 8. Curves of (A) THD *vs.* g_m/I_{DS} and (B) HD3 *vs.* g_m/I_{DS} for measured nMOS IM devices and JNTs at V_{DS} = 1.0 V for several temperatures (V_{out} = 1.50 V).

When two similar devices present different intrinsic voltage gains, the transistor with the lower A_V requires larger input signal amplitude to attain a given output swing. The increase of the input amplitude inherently raises the distortion in a single-transistor circuit as describes the Fourier analysis done in [13], making A_V and HD correlated variables. As IM devices and JNTs present different A_V as exhibited in Figure 5, the distortion of such devices has been evaluated when the transistors were biased aiming a targeted output voltage amplitude (V_{out}, defined as the peak-to-peak output voltage amplitude of the sinusoidal-like signal observed in the drain). THD and HD3 are presented in Figure 8 as a function of g_m/I_{DS} for IM Trigate devices and Junctionless transistors of W_{mask} = 30 nm for V_{out} = 1.5 V.

When the distortion analysis is performed considering the different gains between the devices as in Figure 8 one can see a sensible reduction of both THD and HD3 from both transistors with respect to the curves exhibited in Figure 6. As JNTs present larger intrinsic gains than IM devices as showed in Figure 5, the Junctionless needs smaller input amplitude to attain the required V_{out}, therefore, exhibiting lower values of THD and HD3. Due to the increase of A_V with the temperature raise, JNTs present better distortion at higher temperatures and improvements superior than 5 dB in THD and 20 dB in HD3 are obtained when the temperature is varied from 223 K

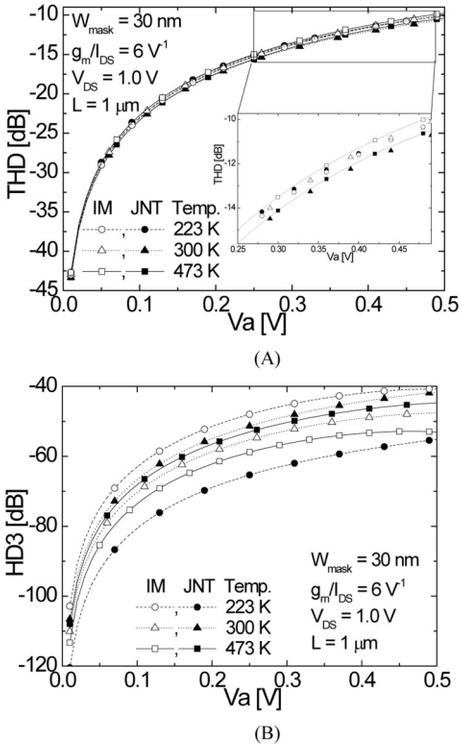


Figure 9. Curves of (A) THD *vs.* Va and (B) HD3 *vs.* Va for measured nMOS IM devices and JNTs at V_{DS} = 1.0 V for several temperatures (g_m/I_{DS} = 6 V^{-1}).

up to 473 K. As IM devices present their largest A_V around room temperature, they exhibit the lowest distortion at 300 K. However, as IM devices present smaller gain dependence on the temperature than Junctionless nanowires, the improvements obtained in THD and HD3 with the temperature variation are more pronounced in the latter.

Experimental results also showed that when W_{mask} is increased from 30 nm up to 40 nm, there is no significant variation in THD or HD3 obtained for devices biased at Va = 50 mV whereas a slight degradation of both THD and HD3 (up to 10 dB) was obtained when a similar V_{out} is targeted due to the reduction of the intrinsic gain obtained in wider devices. In spite of this fact both devices present similar tendency to the curves of THD and HD3 in Figure 8.

The distortion was also evaluated as a function of the input voltage amplitude as shown in Figure 9. THD and HD3 are presented as a function of Va for both IM devices and JNTs of W_{mask} = 30 nm biased at V_{DS} = 1.0 V and g_m/I_{DS} = 6 V^{-1}. As already mentioned, both THD and HD3 are worsened by Va rise. As it can be seen in Figure 9 (A), the temperature variation and the type of the transistor have slightly influenced THD for the entire Va range. However, JNTs have exhibited slightly better distortion than IM Trigate transistors as presented in the insight of Figure 9 (A). The importance of this small variation of THD between the transistors is verified through the maximum input bias that each device allows for attaining a certain THD level. When a THD a level of -12 dB is desired at room temperature, for example, the JNT allows for a maximum Va of 0.363 V whereas the maximum Va of the IM device is 0.291 V. Once more, HD3 has shown to be extremely reduced with respect to THD, remaining at least 30 dB lower than the total distortion in the whole range of Va. Apart from that, according to Figure 9 (B), HD3 seems to suffer influence of the device type and temperature. Indeed, the differences obtained in the third order distortion when the temperature or the device is changed can be correlated with the distortion minima observed in Figure 6 (B). In fact, at g_m/I_{DS} = 6 V^{-1}, the JNT is biased at a linearity peak in HD3 when operating at 223 K and, for that reason, the distortion is lowest obtained in Figure 9 (B).

CONCLUSIONS

This work presented a comparative analysis of the analog parameters of Junctionless transistors and Inversion Mode Trigate devices focusing on the harmonic distortion (HD). The HD evaluation considered the devices operating as amplifiers and was performed in a wide range of temperatures. Initially, both devices were biased at a similar input voltage and no significant variation was observed in THD either changing the device type or the temperature. HD3 also presented similar results for both devices in all the temperatures except for a shift in the linearity peaks along g_m/I_{DS}. These peaks have been attributed to mobility-related mechanisms in IM devices and to the series resistance in JNTs as demonstrated through three-dimensional simulations. When the devices were biased aiming at a targeted output swing, the intrinsic voltage gain showed to influence the distortion and JNTs exhibited better THD and HD3 than Inversion Mode devices due to the higher A_V. Finally, when evaluated in terms of the input voltage amplitude, both devices showed similar HD3 and THD in the whole temperature range.

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