Modeling of Thin-Film Lateral SOI PIN Diodes with an Alternative Multi-Branch Explicit Current Model

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ABSTRACT

We propose the use of an alternative multi-exponential model to describe multiple conduction mechanisms in thin-film SOI PIN diodes with parasitic series resistance over a wide operating temperature range, from 90 to 390 K. This alternative multi-exponential model can be used for semiconductor junctions which exhibit multiple conduction mechanisms with series and shunt resistances. Using Thevenin's theorem and the Lambert W function, the terminal current is expressed explicitly as a function of the terminal voltage. Its explicit nature allows higher computational efficiency and makes this model better suited for repetitive simulation applications than conventional implicit models. Additionally, direct analytic differentiation and integration are possible. This alternative model is used to describe the *I-V* characteristics of real SOI PIN diodes.

Index Terms: Multi-exponential diode model, Explicit junction model, Lambert Function, Thevenin equivalent circuit, SOI PIN diode.

I. INTRODUCTION

Semiconductor junctions are frequently modeled using the simpleified to include the effects of possible series and parallel parasitic loss mechanisms. Unfortunately, the inclusion of such resistive losses transforms the originally explicit equation into an implicit one that must be solved either numerically or approximately [2], [3]. On the other hand, the use of the Lambert *W* function makes the current and the voltage of this modified single-exponential equation explicitly solvable [4]. The Lambert *W* function is a special function defined as the solution to the equation W(x) exp[W(x)] = x [5].

A single-exponential equation is usually not enough to adequately describe the forward *I-V* characteristics of PIN (p+-i-n+) with a significant parasitic series resistance over a wide temperature range, especially at low temperatures [6]. Rather, proper modeling involves the summation of several exponential expressions, corresponding to each of the significant conduction mechanisms present in the device.

Figure 1 shows the equivalent circuit of such a generic model consisting of various exponential-type ideal diodes, a series parasitic resistance (R_s), and two possible parallel parasitic conductances at the junction and at the periphery (G_{p1} and G_{p2}). The current-voltage characteristics of this circuit can be written as:

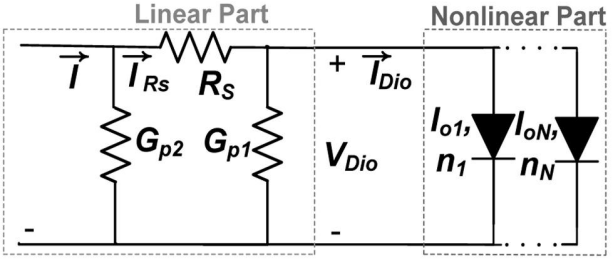

Figure 1. A generic conventional equivalent circuit of a semiconductor junction with multiple diodes and multiple parasitic resistances.

$$I = \left\{ \sum_{k=1}^{N} I_{ok} \left[\exp\left(\frac{V - R_S\left(I - G_{p2}V\right)}{n_k\, v_{th}} \right) - 1 \right] \right\} + G_{p2}V\left(1 + G_{p1}R_S\right) + G_{p1}\left(V - R_S I\right), \quad (1)$$

where v_{th}=kT/q is the thermal voltage, N is the number of different conduction mechanisms to be considered in the model, I_{ok} is the temperature dependent reverse current coefficient corresponding to each kth mechanism, n_k is the corresponding, possibly temperature dependent, "ideality" factor, R_S is the temperature dependent parasitic series resistance, G_{p1} is the parallel parasitic conductance at the junction, and G_{p2} is the parallel parasitic conductance at the periphery.

Equation (1) is in general not explicitly solvable for either the terminal current or voltage, even using the Lambert *W* function. There are two particular cases where an explicit solution is possible: a) the case of a single exponential (N=1) model, whose explicit solutions are well known [7], and b) the case of a double-exponential (N=2) model with series resistance, where the ideality factors are fixed and one equal to twice the other (n_2=2n_1), in which case a quadratic explicit solution is possible for the terminal voltage [6].

We propose here an alternative analytically explicit equation to avoid the explicit insolvability of Eq. (1). It is a multi-exponential model that can be used to describe any generic semiconductor junction.

Its explicit nature allows to significantly reduce simulation times, and to effortlessly differentiate or integrate it to derive other functions such as the device's dynamic resistance or its temperature dependence.

II. RIGOROUS GENERAL ANALYSIS

We will use Thevenin's theorem in a rigorous way to develop the alternative model for a generalized diode. Approximate simplified nonlinear Thevenin's models have been used to analyze solar panels [8] - [10]. Separating the linear and nonlinear components, indicated in Figure 1, the Thevenin equivalent circuit of the linear part, as shown in Figure 2, is made up of a Thevenin equivalent voltage, and a Thevenin equivalent resistance which only contains the contribution of R_S and G_{p1}:

$$V_{THE} = \frac{R_{THE}}{R_S} V \ , \tag{2}$$

$$R_{THE} = \frac{R_S}{1 + G_{p1} R_S} \ . \tag{3}$$

We note that the absence of G_{p2} from the Thevenin equivalent resistance is correct, since it is in perfect agreement with the fact that I_{Dio} does not depend on G_{p2}. Nevertheless, the effects of G_{p2} on the total current will be accounted for after I_{Dio} is calculated.

For a generic case of N diodes in parallel, the total current in the nonlinear part, I_{Dio}, will be obtained numerically by using the circuit in Fig 2. This procedure is equivalent to solving equation (1).Once the total current flowing into the parallel combination of all diodes, I_{Dio}, is known, the voltage across the nonlinear part, V_{Dio}, can be expressed by writing:

Then, once the values of I_{Dio} and V_{Dio} are found, the total current is obtained by going back to the original circuit shown in Figure 1:

$$V_{Dio} = V_{THE} - I_{Dio} R_{THE} \ . \tag{4}$$

$$I = G_{p2} V + G_{p1} V_{Dio} + I_{Dio} \ . \tag{5}$$

III. THE PROPOSED ALTERNATIVE MODEL

The alternative explicit model is proposed to be used instead of the conventional implicit model represented by the circuit of Figure 1 and mathematically described by (1). The proposed alternative model derives from a recently published idea [11] and is represented by the circuit shown in Figure 3.

This model's *I–V* characteristics may be found by solving each branch separately and then adding their solutions together. Accordingly, the following explicit equation may be written for the total current into the diodes:

$$I_{Dioa} = \sum_{k=1}^{N} \left\{ \frac{n_{ka} v_{th}}{a_k R_{THE}} W_0 \left[\frac{a_k R_{THE} I_{0k}}{n_{ka} V_{th}} \exp\left(\frac{V_{THE} + a_k R_{THE} I_{0k}}{n_{ka} v_{th}} \right) \right] - I_{0k} \right\} , \tag{6}$$

where the single global series resistance, R_{THE}, present in the conventional model, has been replaced in this alternative model by individual resistances, $a_k R_{THE}$, placed in series at each of the N parallel current paths representing the different conduction mechanisms to be modeled and W_0 is short hand notation for the principal branch of the Lambert function. Finally the total current is obtained by substituting (6) into (5) in combination with (2)-(4):

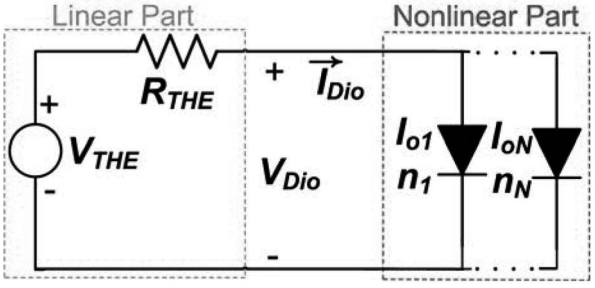

Figure 2. Thevenin equivalent circuit used to obtain the voltage and the total current in the nonlinear part.

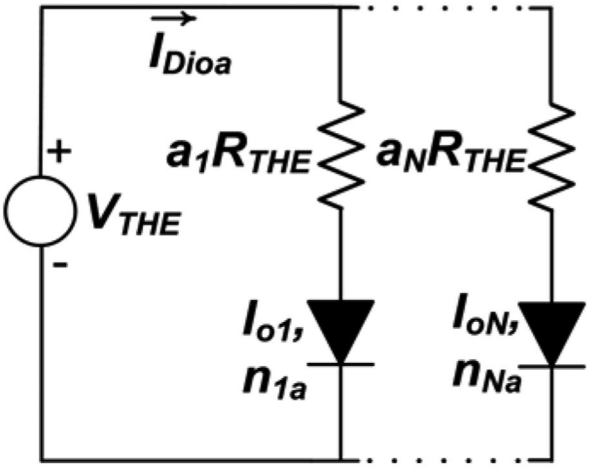

Figure 3. Alternative Model equivalent circuit with multiple diodes and Thevenin's resistance in series with each diode

$$I = \sum_{k=1}^{N} \left\{ \frac{n_{ka} v_{th}}{a_k R_S} W_0 \left[\frac{a_k R_S I_{0k}}{n_{ka} v_{th} \left(1 + R_S G_{P1}\right)} \exp\left(\frac{V + a_k R_S I_{0k}}{n_{ka} v_{th} \left(1 + R_S G_{P1}\right)} \right) \right] - \frac{I_{0k}}{\left(1 + R_S G_{P1}\right)} \right\} + \frac{V \left(G_{P1} + G_{P2} + G_{P1} G_{P2} R_S\right)}{1 + R_S G_{P1}} \quad . \qquad (7)$$

In this alternative model the terminal current is an explicit analytic function of the terminal voltage, as indicated by (7). However, it should be kept in mind that this model is only an approximation to the conventional model of Figure 1, since it is not exactly analogous for all arbitrary sets of parameters. Nevertheless, there is a broad range of practical situations, or model parameter sets, for which the correspondence between both models happens to be excellent. Most real PIN diodes, as well as many other useful junctions, clearly fall within this category. Further research is needed in order to determine precisely the limits of applicability of the present approximation.

IV. MODELING OF LATERAL SOI PIN DIODES

The alternative model was used to describe the forward current of experimental lateral thin-film SOI PIN diodes fabricated using a 150 nm technology from OKI Semiconductor on a 40 nm thick silicon layer over a 145 nm substrate oxide [12]. Figure 4 presents the schematic cross-section of this device.

I-V characteristics were measured from 0.1 to 1.5 V, using 10 mV voltage steps, at several temperatures. Figure 5 presents the *I-V* characteristics of a 0.8 μm long, 50 μm wide device measured from 90 to 390 K, with increments of 30K.

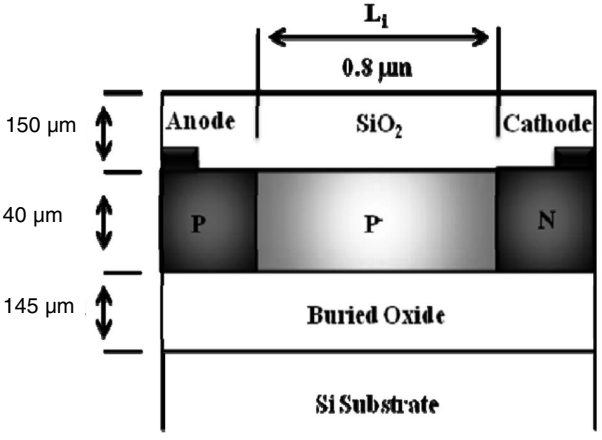

Figure 4. Schematic cross-section of the thin film lateral PIN diode under study.

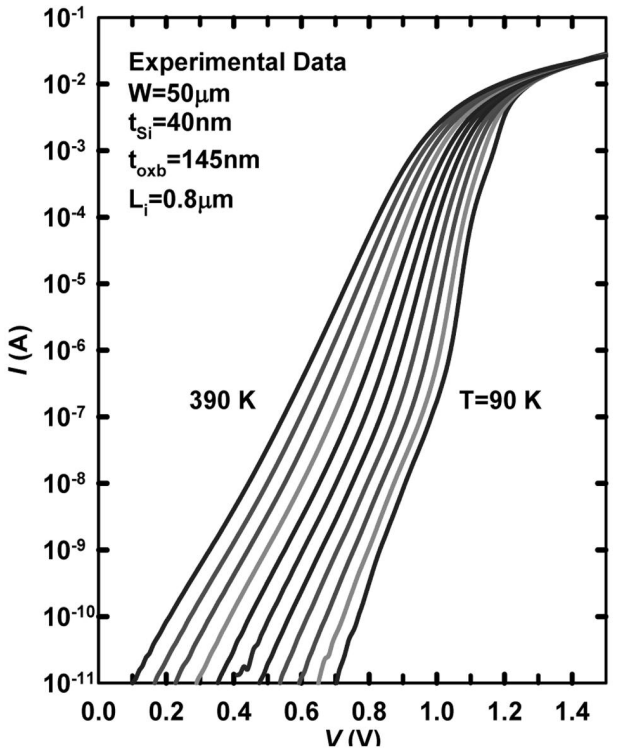

Figure 5. Measured forward *I-V* characteristics of an experimental 0.8 μm long lateral SOI PIN diode for a wide range of operating temperatures.

A. Preliminary Experimental Data Analysis

A detailed assessment of this device's measured data reveals that that there is a significant series resistance, and that resistive shunt losses are negligible in this case. Furthermore, several distinct regions corresponding to different conduction phenomena are observed. In order to determine these different regions in the *I-V* curve, the ideality factor can be approximately calculated over the entire range by simply taking the first derivative of the current

$$n = \frac{1}{v_{th}} \left(\frac{1}{d \ln(I) / dV} \right) = \frac{1}{v_{th}} \left(\frac{I}{dI / dV} \right) \quad . \qquad (8)$$

The previous equation is obtained by assuming an ideal single exponential diode model and negligible series resistance. The results for each temperature are presented in Figure 6a. It shows three apparent regions: a low conduction region where the diode ideality factor has a strong dependence on temperature, a medium conduction region where the ideality factor is approximately constant, and a high conduction region where the presence of the parasitic series resistance distorts the behavior of *n*, which seems to unduly increase.

To uncover the true behavior of the ideality factor at high conduction we resort to a useful property of the Integral Nonlinearity Function, also known as "*D* Function," defined in (9) [13]. Here we will use the abil-

ity of the *D* Function to eliminate the effect of any linear circuit components, in this case the effect of the series resistance [13].

$$D \equiv \int_{I_o}^{I} V dI - \int_{0}^{V} I dV = I\, n\, v_{th} \left[\ln\left(\frac{I}{I_0}\right) - 2 \right] . \quad (9)$$

Defining the ratio of the *D* Function to the terminal current as a "*G* Function," the ideality factor may be expressed independently of the series resistance as:

$$n = \frac{1}{v_{th}} \frac{dG}{d\left(\ln(I)\right)} . \quad (10)$$

The previous equation is obtained by assuming a diode model with a single exponential and negligible series resistance. Figure 6b shows the evolution of the ideality factor with forward voltage as obtained using (10). The effect of the series resistance has now been eliminated and we can say that the ideality factor temperature dependent within the range shown.

From the above analysis we conclude that this device may adequately modeled with an *N*=3. The corresponding circuit of the alternative model is shown in Fig 7. This model's *I–V* characteristics may be mathematically represented by the following explicit equation for the current:

$$\begin{aligned} I(V,T) = & \frac{n_L(T)v_{th}}{R_L(T)} W_0\left[\frac{R_L(T)I_{oL}(T)}{n_L(T)v_{th}} \exp\left(\frac{V + R_L(T)I_{oL}(T)}{n_L(T)v_{th}} \right) \right] \\ & + \frac{n_M(T)v_{th}}{R_M(T)} W_0\left[\frac{R_M(T)I_{oM}(T)}{n_M(T)v_{th}} \exp\left(\frac{V + R_M(T)I_{oM}(T)}{n_M(T)v_{th}} \right) \right] \\ & + \frac{n_H(T)v_{th}}{R_H(T)} W_0\left[\frac{R_H(T)I_{oH}(T)}{n_H(T)v_{th}} \exp\left(\frac{V + R_H(T)I_{oH}(T)}{n_H(T)v_{th}} \right) \right] \\ & - I_{oL}(T) - I_{oM}(T) - I_{oH}(T) \end{aligned} \quad (11)$$

all the parameters are defined as before, with the L, M, and H subindices referring to the conduction mechanisms that dominate at low, medium, and high forward voltages, respectively.

Notice that the Thevenin's series resistance, R_{THE}, of Figure 2, has now been replaced by three distinct individual series resistances, $a_1R_{THE} = R_L$, $a_2R_{THE} = R_M$, and $a_3R_{THE} = R_H$, placed at each of the parallel branches associated with the different conduction mechanisms. This feature is what makes the model analytically solvable.

Due to the fact that shunt losses are negligible in this device, $G_{p1} \approx G_{p2} \approx 0$ and:

$$\frac{1}{R_S} \approx \frac{1}{R_L} + \frac{1}{R_M} + \frac{1}{R_H} \approx \frac{1}{R_H} . \quad (12)$$

A word of caution is called for about using Eq. (11) for numerical calculations when the value of any of the associated individual branch series resistances takes the value of zero. In that unlikely case, the particular branch where the series resistance goes to zero must be directly described by the unmodified Shockley equation.

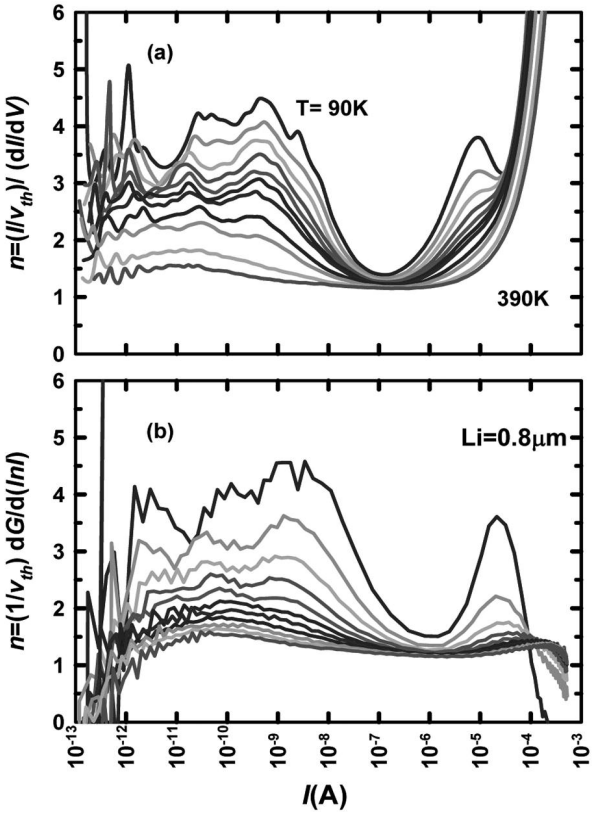

Figure 6. Approximate ideality factor vs experimental current for a wide temperature range, calculated from (a) the derivative of *I* and (b) the derivative of the *G* Function.

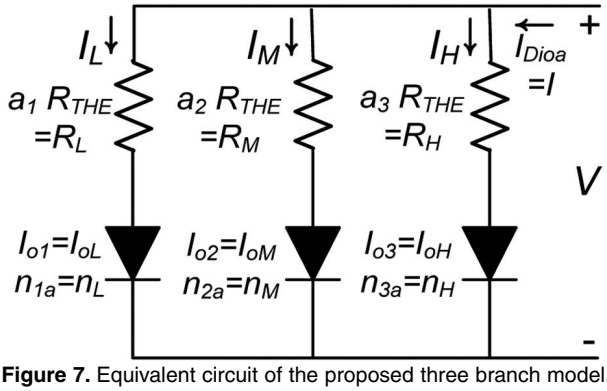

Figure 7. Equivalent circuit of the proposed three branch model.

It is worth mentioning here that Eq. (11) resembles the defining equation of a model proposed by Miranda et al. [14] to express the leakage post-breakdown *I-V* characteristics of HfO2/TaN/TiN gate oxide stacks used in MOSFETs. In that unrelated model, the most relevant post-breakdown conduction mechanisms that arise in the broken gate oxide are described by a parallel combination of two opposite-direction connected diodes with individual series resistances and a shunt leakage path [14].

Models which show some similarity to the present model have also been proposed to describe the current conduction mechanisms present in poly and multicrystalline solar cells [15-18].

B. Experimental Results

Parameter extraction was performed on these lateral SOI PIN diodes using global fitting of the logarithm of the alternative model (11) to the measured devices' *I-V* characteristics. The extraction was done in two steps: First, all parameters were considered to be temperature dependent and their values extracted. Second, the values of those parameters that exhibited small temperature dependence were fixed and the rest of the parameters were extracted again. Table I presents the results of this process.

Figure 8 presents the model playbacks obtained with the extracted model parameters which were used to calculate the current and its three branch components, versus the normalized applied forward voltage, plotted over the original measured data (represented by symbols) of the experimental 0.8 mm diode at three representative temperatures.

Figures 9, 10 and 11 present the extracted reverse current coefficients, low voltage conduction ideality factor and high voltage series resistance parameters, respectively.

An exponential $1/T$ dependence is observed for the reverse current coefficients in the medium and high forward voltage conduction regions, where the ideality factors have fixed values ($n_H = n_M = 1.2$).

Table 1. Extracted Model Parameter Values

Fixed parameter values: $n_H = n_M = 1.2$; $R_M = 150\Omega$; $R_L = 50k\Omega$

T (K)	Temperature dependent parameter values:				
	I_{oH} (A)	I_{oM} (A)	I_{oL} (A)	n_L	R_H (Ω)
90	6.85×10^{-58}	1.44×10^{-55}	1.00×10^{-21}	3.89	11.10
100	5.30×10^{-52}	3.17×10^{-50}	2.93×10^{-21}	3.59	11.92
110	2.99×10^{-47}	7.44×10^{-46}	8.02×10^{-21}	3.35	12.57
120	2.49×10^{-43}	3.29×10^{-42}	2.71×10^{-20}	3.17	13.07
150	8.72×10^{-35}	3.43×10^{-34}	5.57×10^{-19}	2.74	14.25
180	4.16×10^{-29}	8.04×10^{-29}	8.85×10^{-18}	2.46	14.99
210	4.81×10^{-25}	5.15×10^{-25}	9.55×10^{-17}	2.25	15.74
240	5.51×10^{-22}	3.83×10^{-22}	1.02×10^{-15}	2.13	16.05
270	1.41×10^{-19}	5.16×10^{-20}	5.29×10^{-15}	1.97	16.83
300	1.21×10^{-17}	2.45×10^{-18}	2.95×10^{-14}	1.88	17.45
330	4.50×10^{-16}	5.42×10^{-17}	1.46×10^{-13}	1.83	18.04
360	8.61×10^{-15}	1.07×10^{-15}	5.70×10^{-13}	1.78	18.59
390	1.09×10^{-13}	1.40×10^{-14}	2.42×10^{-12}	1.82	19.23

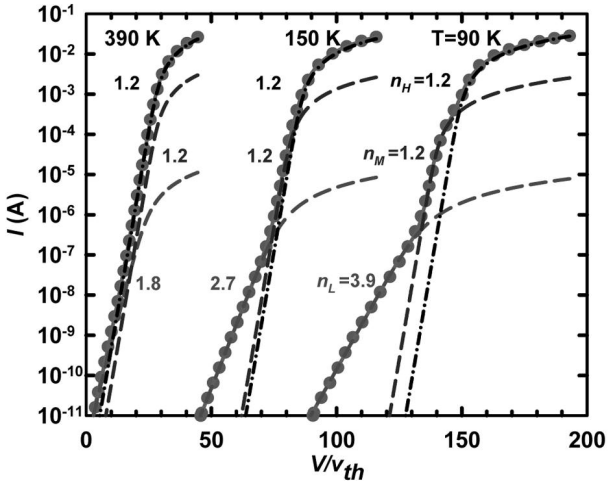

Figure 8. Measured (lines) and model playback (symbols) of the current of the experimental 0.8 mm long lateral SOI PIN diode as a function of normalized applied forward voltage at three representative temperatures.

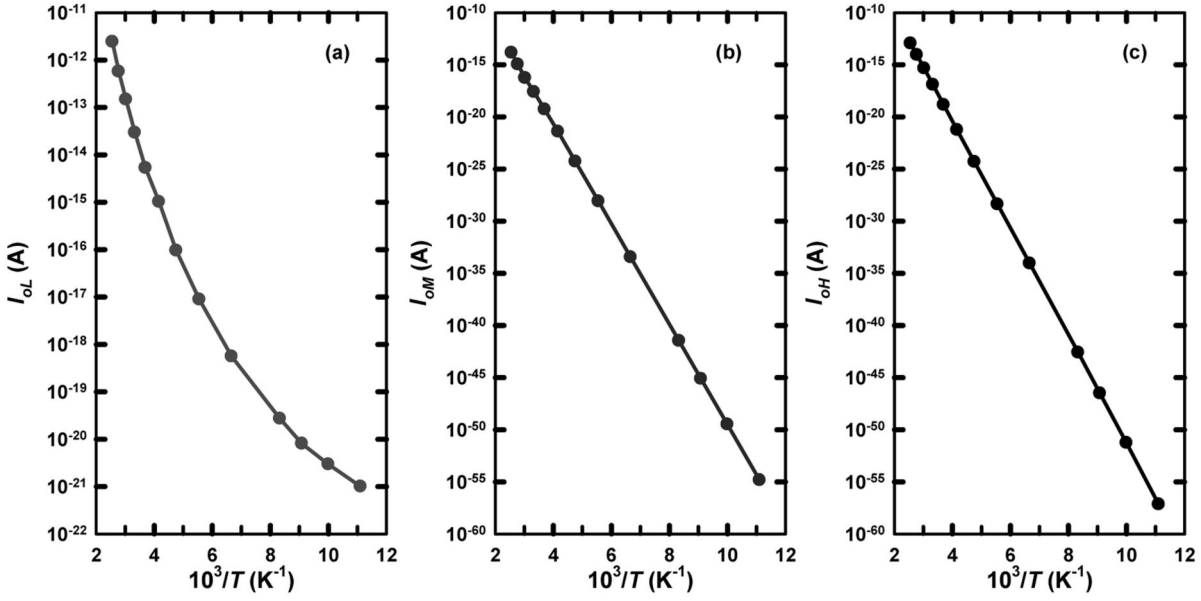

Figure 9. Extracted values of the temperature dependent reverse current coefficient parameters corresponding to the three conduction mechanisms considered.

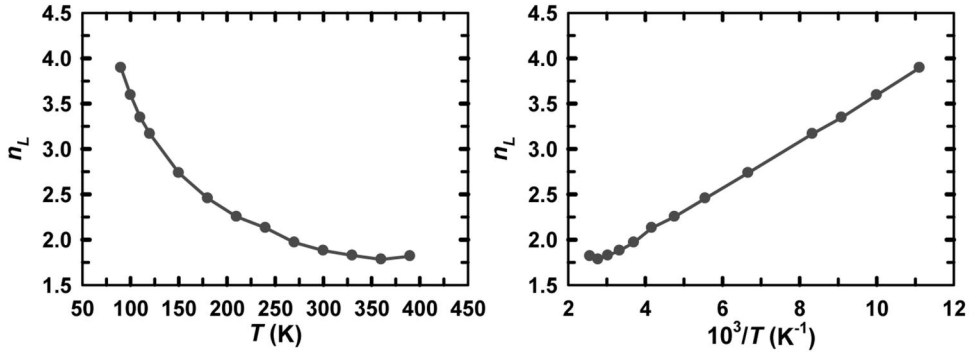

Figure 10. Temperature dependence of the extracted low voltage conduction ideality factor parameter.

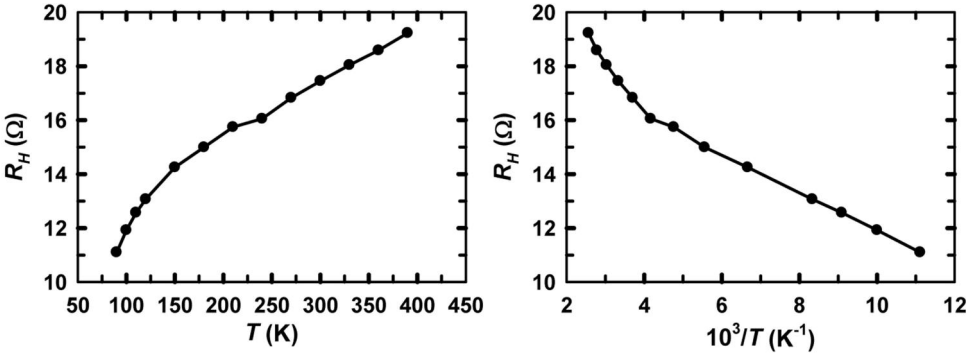

Figure 11. Temperature dependence of the extracted high voltage series resistance parameter (R_H » R_S)

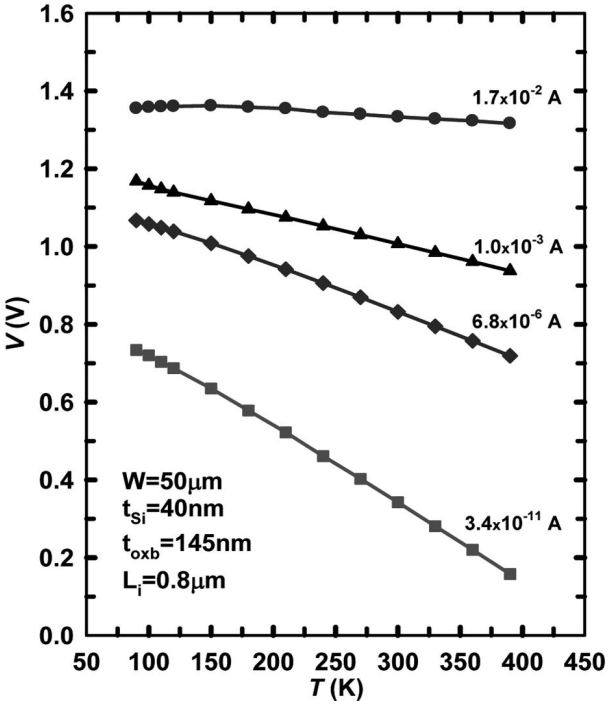

Figure 12. Temperature dependence of the voltage at four values of forward current, representative of each of the three low, medium and high forward conduction regions, plus the upper series resistance dominated conduction region (square, diamond, triangle, and circle symbols, respectively).

On the other hand, the low forward voltage conduction region exhibits a distinctly different behavior for both the reverse current coefficient and the ideality factor, as can be predicted by simple observation of Figure 8. The temperature dependence of the parasitic series resistance is represented by the high forward voltage resistance behavior (R_H), which shows a slight increase in resistance with temperature.

Figure 12 presents the temperature dependence of the terminal voltage at four representative values of forward current, chosen within each of the three distinctive low, medium and high forward conduction regions, plus the upper series resistance dominated conduction region.

As expected, each curve in Figure 12 exhibits a different quasi-linear temperature dependence of the forward voltage. Also, the almost flat curve corresponding to the region where the parasitic series resistance is dominant indicates an almost temperature independent behaviour in this region.

V. CONCLUSIONS

Our recent proposal for modeling PIN diodes [11,19] has been generalized by separating the nonlinear components and applying Thevenin's theorem to the remaining linear components. The present model accounts

for the various current transport mechanisms that usually coexist in real diodes with series and shunt losses.

The distinctive quality of the presently proposed alternative approach is that the terminal current may be expressed as an explicit analytic function of the applied terminal voltage. This valuable feature makes this model more attractive than the conventionally used multi-diode model with series and shunt resistances, whose current-voltage equation is in general unavoidably implicit, and thus must be solved by numerical iteration [20], [21].

The proposed alternative model was used for experimental *I-V* characteristics of lateral thin-fim SOI PIN diodes at several temperatures. The close match observed between the experimental and the playback *I-V* characteristics generated using the extracted parameters corroborates the excellent suitability of this multi-branch model approach to describe the lateral thin-film SOI PIN diodes over a wide temperature range, from cryogenic to above room temperatures. The appropriate modeling of their characteristics is vital for the practical use of these devices in practical applications. Such as their use as temperature sensors, and current controlled linear resistors for RF applications [22]. Moreover, lateral SOI PIN diodes are widely used in various "gated-diode" configurations [23, 24] as Gate-Controlled Field-Effect diodes [25] for clamping applications in ESD protection. The unique explicit nature of the proposed model allows for the analytically explicit description of other model-derived functions, such as the dynamic resistance or the temperature dependence that can be very useful in future device analysis, but are beyond the scope of the present characterization.

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