SOI n- and pMuGFET Devices with Different TiN Metal Gate Thickness and Crystallographic Orientation of the Sidewalls

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ABSTRACT

This work presents an analysis of SOI p- and nMuGFET devices with different TiN metal gate electrode thickness for rotated and standard structures. Thinner TiN metal gate allows achieving a higher intrinsic voltage gain in spite of the reduced variation observed of the gm/I_{DS} characteristics. This effect can be attributed to the increased Early voltage values observed for thinner TiN metal gate. Even with the larger mobility of the rotated nMuGFET devices when compared with the standard ones, the larger output conductance degradation resulted in an almost similar intrinsic voltage gain. P-channel devices, when implemented on the rotated layout, offer a lower intrinsic voltage gain. The GIDL current was also analyzed on these devices, indicating to be larger in thinner metal gate and rotated configuration.

Index Terms: TiN**,** high k, analog performance, MuGFETs.

1. INTRODUCTION

Amongst the technological solutions available that can achieve a higher current drive and better short-channel characteristics, one has the well known multiple gate devices (MuGFETs) (1). Some performance improvements have already been discussed, such as the ability in controlling the leakage current and reduced junction capacitances (2). They have an improved analog behavior due to a reduced drain output conductance, a quasi-ideal subthreshold swing and a better ratio between on-off current (3-7). Furthermore, high-k dielectrics such as hafnium oxide have also been implemented in order to continue the gate oxide scalability, reducing in that way the gate current (8, 9). To complete the gate stack structure, metal gate electrodes have been added allowing metal gate work function (WF) engineering. For MuGFETs, the integration of a metal nitride is straightforward and titanium nitride (TiN) has been widely studied (10-15). The interface quality has also been studied in MuGFET devices, where the fin width needs to be smaller than the gate length to control the short channel effects (16). The sidewall surfaces have a (110) crystallographic orientation that degrades the electron mobility as compared to the standard planar (100) orientation (17). In order to avoid this mobility degradation the devices can be rotated over 45º, yielding in that way the same top and sidewall (100) plane (18-19). Although, this improvement is observed only in nMuGFET devices while in p-type the hole mobility is reduced (20). In this paper we will present a study of the influence of different sidewall crystal orientations on the behavior of n- and p-channel SOI MuGFET devices with a TiN/HfSiO gate stack. Additionally, different TiN metal gate electrode thicknesses will be considered and investigated from an analog applications point of view.

2. DEVICES CHARACTERISTICS

The SOI MuGFETs used in this work are n- and p-type channels with a silicon film of 65nm on 150nm buried oxide. The channel is fully depleted, since the doping concentration is about $1x10^{15}$ cm^{-3}. The gate dielectric consists of 1nm SiO_2 chemical oxide (Interfacial Layer - IL), on which 2.3nm Metalorganic Chemical Vapor Deposition (MOCVD) HfSiO is deposited. TiN capped with 100nm polysilicon was used as a gate electrode. Concerning the TiN thickness, different splits were considered: 2nm (64 Atomic Layer Deposition - ALD cycles), 5nm (160 ALD cycles) and 10nm (320 ALD cycles). After gate patterning, the extensions were implanted and a 35nm wide nitride spacer was formed. Next, Si Selective Epitaxial Growth (SEG) was done in

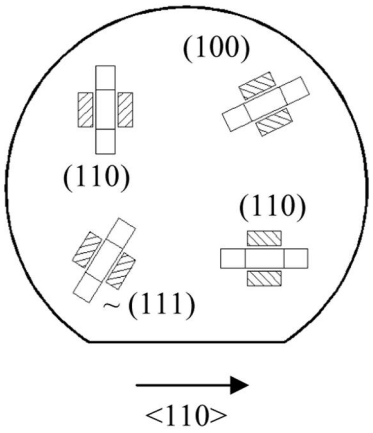

Figure 1. Crystallographic orientation of the sidewalls

the source and drain areas before the highly doped implantations. Subsequently, a 1050 °C spike anneal was given. Finally, NiSi was used to finish the devices. On the same wafer, some devices were rotated over 45º. Different effective channel lengths were considered for devices with an effective channel width of 25nm with 10 fins. More process details can be found elsewhere (21). Figure 1 shows the different crystal planes on a silicon surface.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1 Threshold voltage

Figure 2 presents the threshold voltage (V_T) as a function of the channel length (L_{eff}) for different TiN thicknesses for standard and rotated structures. A larger V_T is observed for the thicker TiN metal gate for both channel types, due to the larger metal gate work function as discussed in reference (22). Devices with a rotated layout show a slight increase in $|V_T|$ when compared to the standard ones.

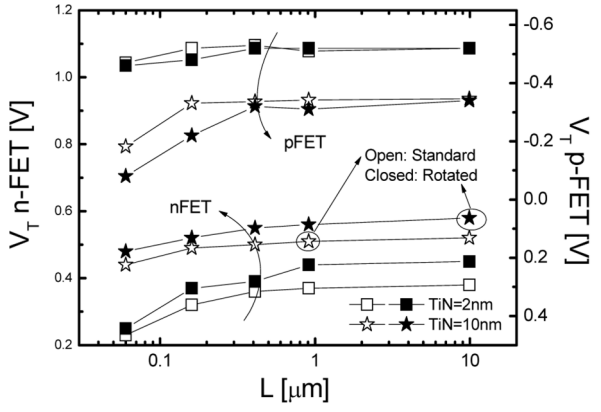

Figure 2. Extracted threshold voltage as a function of the effective channel length for standard and rotated n- and pMuGFETs with different TiN metal gate thickness.

In order to better discuss this V_T behavior the gate to channel capacitance (C_{GC}) curves were extracted as shown in Fig. 3 for the different devices under study. In spite of the slight variation in the capacitance, it is already possible to observe an increase in C_{GC} (reduced gate oxide thickness) for the rotated devices for all TiN thicknesses analyzed, and this behavior is not in line with the V_T variation, where a smaller gate oxide thickness leads to a reduced V_T.

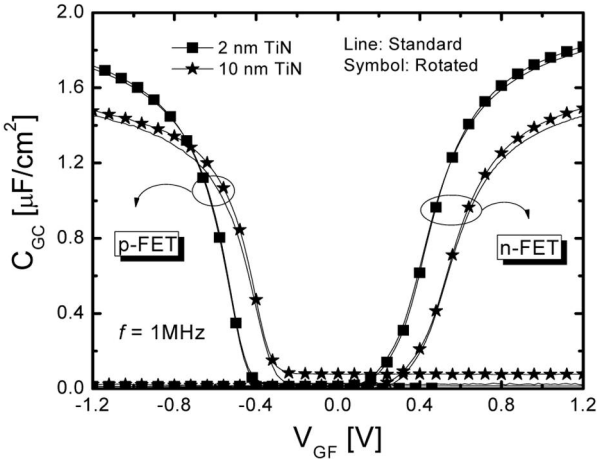

Figure 3. Gate to channel capacitance (C_{GC}) as a function of the gate voltage for standard and rotated n- and pMuGFETs with different TiN metal gate thickness.

Based on this, a possible reason for the V_T behavior of the rotated devices could be related to an increase in the flatband voltage (V_{FB}). This V_{FB} variation could be the result of different contributions: the rotated devices could present a higher amount of charges when comparing with the standard devices, increasing in that way the flatband voltage; another important consideration is a possible different work function that can be obtained on devices with TiN as metal gate together with different orientation (23). Finally, it is also possible to assign this higher V_T of the rotated devices to a possible fin width reduction due to a different fin process formation.

The maximum transconductance ($g_{m,max}$) was extracted for the different devices in the saturation regime, as presented in Fig. 4a for n-channel and in Fig. 4b for p-channel. In our previous work, we observed an improvement in transconductance for a thinner metal gate in the strong inversion region, and this behavior was maintained for rotated devices. This phenomenon is related to an improved mobility for the devices with a thinner TiN metal gate. This can be attributed to a lower density of Coulomb scattering centers. As expected for n-channel devices, rotating the layout improves the maximum transconductance due to the transport that now occurs in the (100) plane. This crystal orientation benefits the electron mobility as compared to the standard (110) orientation. However, rotated p-channel devices show no enhanced characteristics but a degradation of the transconductance is observed.

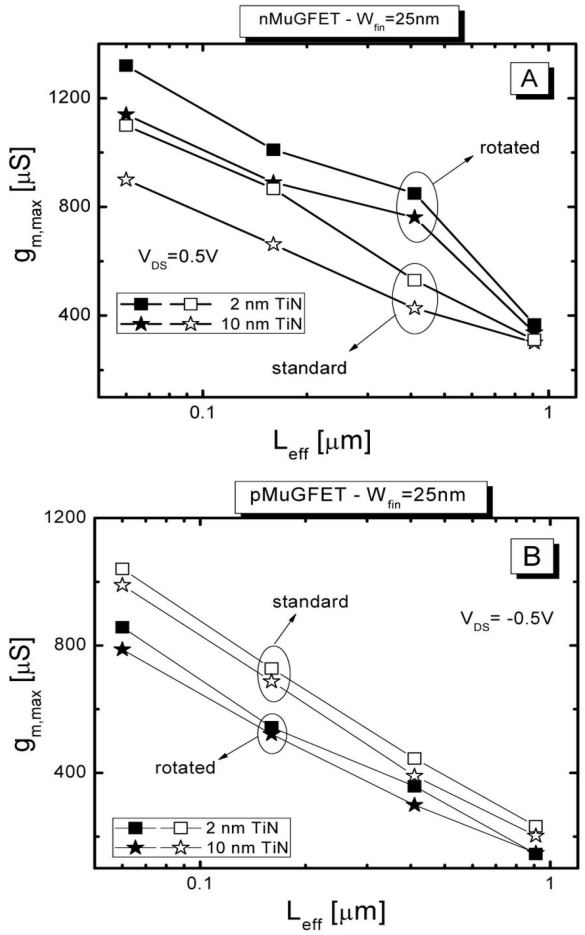

Figure 4. Transconductance as a function of the effective gate length for $|V_{DS}|$=0.5V on (a) nMuGFET and (b) pMuGFET.

3.2 GIDL current

The gate induced drain leakage (GIDL) is a tunneling current composed of the band-to-band tunneling (BTBT) and trap assisted tunneling (TAT) currents. The BTBT current is observed at high drain-to-gate electrical field (larger V_{DG}) and the TAT current at low field (reduced V_{DG}). These tunneling current takes place in the narrow-depletion region (formed due to a negative gate voltage) at the gate-to-drain overlap region (24-26). The GIDL current density can be modeled by Equation (1) (27).

$$J_{GIDL} = A \cdot E_T \cdot \exp(-B / E_T) \quad (1)$$

where E_T is the electric field at the maximum band-to-band tunneling point, A is a pre-exponential parameter given by Equation (2) and B (typically 23–70MV/cm) is a physics-based exponential parameter that is defined by Equation (3), where *h* is Plank's constant, m_r is the reduced effective mass of electrons and holes and E_g is the energy gap of silicon (26).

This GIDL current was also analyzed on devices with different crystal orientation. Figure 5 shows the drain current (I_{DS}) as a function of the gate voltage over-

$$A = \frac{2qm_r \pi E_g^{\ 2}}{h^3} \quad (2)$$

$$B = \frac{\pi^2 \sqrt{m_r} E_g^{3/2}}{qh\sqrt{2}} \quad (3)$$

drive (V_{GT} =V_{GF} -V_T) and at a saturation condition $|V_{DS}|$=1.2V and this GIDL current can be observed in the accumulation region. P- and nMuGFETs with different TiN metal gate thicknesses on standard and rotated devices are reported in this figure. It can be observed that in the accumulation region rotated devices show a larger GIDL current in both channel devices. Additionally, a thinner metal gate demonstrates an increased GIDL behavior.

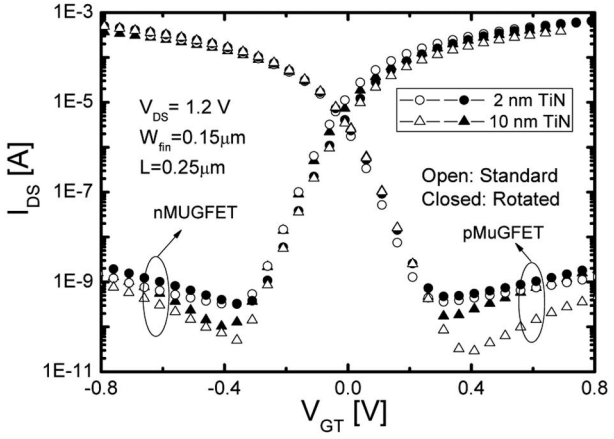

Figure 5. Drain current as function of the gate overdrive for the different devices analyzed.

This improvement in GIDL for thinner metal gate can be explained through Figure 6, which represents the schematic dependence of the electric field components on the gate oxide thickness. In summary, a thinner gate oxide leads to an increase of the vertical electric field, which increases the GIDL according to Eq. (1). As observed in Fig. 3 a thinner metal gate resulted in a reduced gate oxide thickness and this gives rise to this large GIDL current (28).

According to the literature when non-(100) surface orientations are used, the electron and hole mobility are modified due to the asymmetry of the carrier effective masses in the silicon crystal lattice. It is also known that the higher mobility values obtained for the (100) plane, correspond to a lower conduction effective mass. In spite of that, the other orientations have larger conduction effective masses and, therefore, lower mobility values (29-30). Additionally, the terms A an B defined in Eqs (2) and (3) are dependent on the reduced effective mass of electrons and holes (26). As a result, rotated devices present a smaller carrier effective mass that reduces the terms A and B. Considering that the B parameter is predominant in the GIDL current, this yields a larger GIDL current for rotated devices.

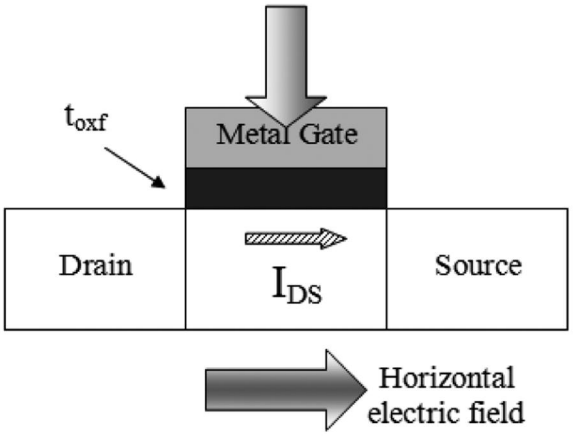

Figure 6. Schematic electric field components dependence on the gate oxide thickness.

3.3 Analog parameters

The g_m / I_{DS} ratio is presented in Fig. 7 as a function of the normalized drain current that was extracted at V_{DS}=0.5 V (it was also analyzed with larger drain voltage) for standard and rotated MuGFETs, with a TiN metal gate of 10 nm and for both channel types. The g_m/I_{DS} value of nearly $38V^{-1}$ in the weak inversion region is related to a nearly ideal value of the subthreshold swing (S) that is around 60mV/dec. The improvement in mobility observed for n-type rotated devices can also be seen in the g_m/I_{DS} ratio in the strong inversion region. The pMuGFETs show a lower g_m/I_{DS} ratio for the rotated layout, which is in agreement with the reduced transconductance.

The output conductance (g_D) has been extracted from the I_{DS} vs. V_{DS} curves measured at a gate voltage overdrive of V_{GT}=200mV (Fig. 8a). It is possible to observe an increase in g_D with increasing TiN metal gate thickness. A g_D degradation is observed for the rotated devices. This phenomenon suggests that they are more sensitive to the channel modulation. While n-type rotated structures show a higher g_D than the p-type ones, in standard devices the opposite behavior is observed.

Figure 8b presents the Early voltage ($V_{EA}=I_{DS}/g_D$) as a function of the channel length for the different TiN metal gate thickness in n-MuGFETs in the standard and rotated configuration at V_{DS}=0.5 V and a gate voltage overdrive ($V_{GT}=V_{GF}-V_T$) of 200 mV. As expected, a higher V_{EA} is observed for the standard devices and this for all the channel lengths studied.

The inset of Fig. 8b shows that for nMuGFETs V_{EA} improves over the p-type channel for both layout conditions. However, this difference is smaller for rotated structures because of the higher g_D and drain current for the n-channel devices. Instead, for standard structures the increased drain current associated with the smaller g_D (nMuGFET) contributes to this higher difference in V_{EA} when comparing n- and p-channels.

Furthermore, a thicker metal gate for the same L_{eff} leads to a reduction in V_{EA}. With increasing TiN metal

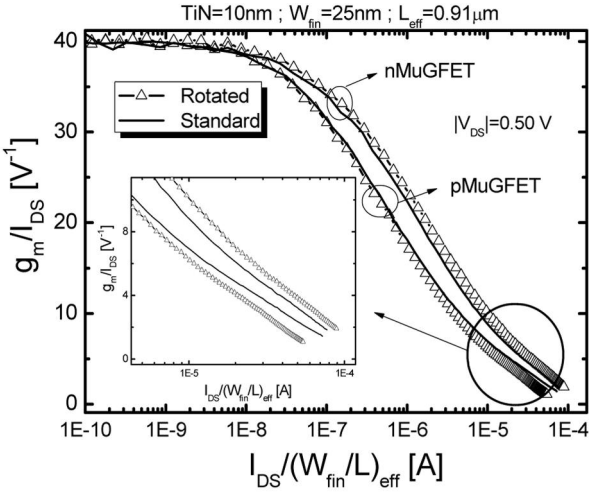

Figure 7. Extracted g_m/I_{DS} ratio for standard and rotated MuGFETs, with a TiN metal gate of 10 nm and for both channel types.

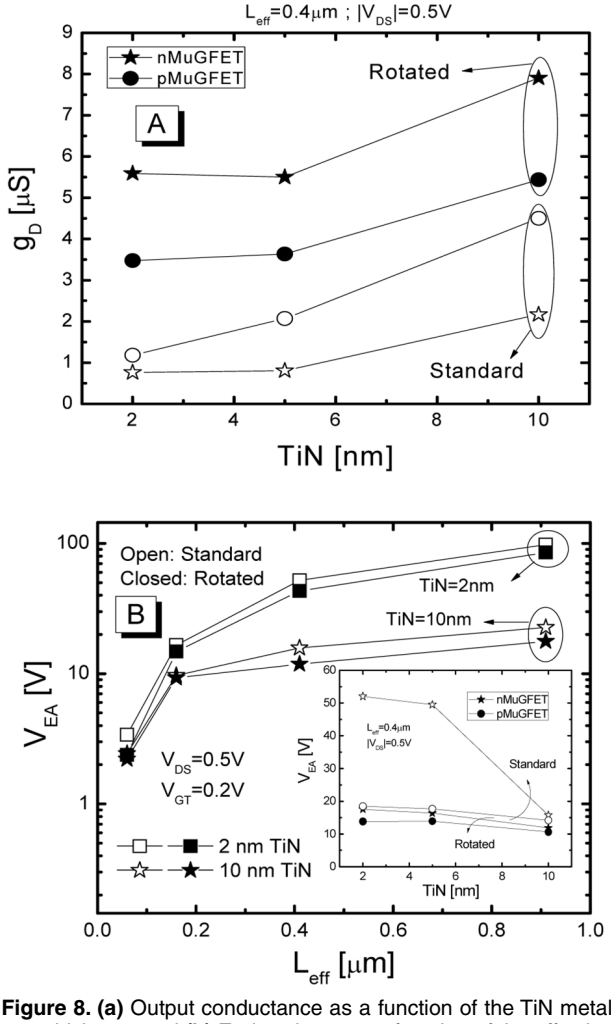

Figure 8. (a) Output conductance as a function of the TiN metal gate thickness and **(b)** Early voltage as a function of the effective channel length for standard and rotated MuGFETs with $|V_{DS}|$=0.5V and $|V_{GT}|$=200mV.

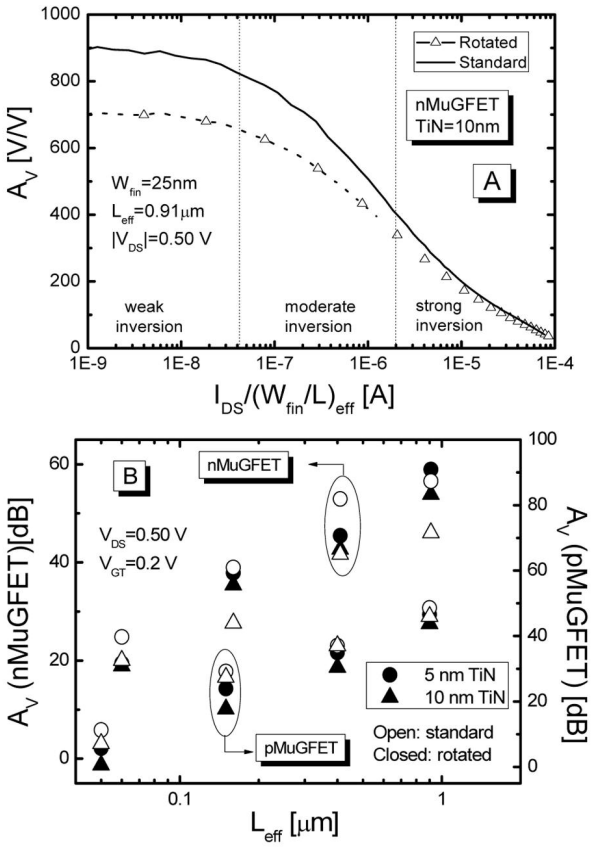

Figure 9. Calculated intrinsic gain as a function of the **(a)** normalized drain current and **(b)** channel length for the different devices studied at $|V_{DS}|$=0.5 V and $|V_{GT}|$=200 mV.

gate thickness an increase of EOT is observed and therefore a reduction of the gate capacitance. This variation in gate oxide thickness reduces the transversal electric field influence on the drain current, emphasizing the horizontal electric field contribution and, consequently, decreasing V_{EA} for all cases analyzed.

Finally, the intrinsic voltage gain ($A_V=V_{EA}*g_m/I_{DS}$) was extracted for the standard and rotated devices as can be seen in Fig. 9a for nFET devices with 10 nm TiN. In the weak inversion region standard devices can achieve a larger gain. The larger Early voltage for standard devices is resulting in this enhanced A_V.

In spite of that, in strong inversion, there is no large difference of the intrinsic voltage gain between both orientations, as can also be seen in Fig. 9b for the different channel lengths. For the rotated n-channel devices it can be observed that in spite of the reduced Early voltage, the gain is almost the same as for the standard devices. This is related to the g_m/I_{DS} behavior that is larger for rotated structures. On the p-type structures one can see a small reduction of the gain for the rotated devices, due to the V_{EA} reduction associated with the lower mobility.

Comparing the different TiN metal gate thicknesses, improved gain can be achieved with thinner TiN for both rotated and standard devices, due to the higher V_{EA}. A reduced voltage gain is observed for pMuGFETs as compared to the n-type devices which is in agreement with the lower mobility and Early voltage.

4. CONCLUSIONS

This paper compares the analog behavior of rotated SOI MuGFET structures fabricated on standard and rotated notch substrates. In addition, the impact of the different TiN metal gate thicknesses was also addressed. In summary, thinner metal gate devices show improved intrinsic voltage gain due to the larger Early Voltage. Rotated devices demonstrate a different behavior with respect to the channel type. 45º rotated nMuGFET structures showed a similar intrinsic voltage gain behavior as the standard ones. This is related to the better suitability of these rotated devices in modulating the channel even with larger mobility. For the p-channel devices, the reduced Early voltage and mobility present for the rotated structures lead to a slightly reduced intrinsic voltage gain when compared to the standard counterparts. Rotated devices and thinner TiN metal gate result in an enhanced GIDL current.

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