One Transistor Floating Body RAM Performances on UTBOX Devices Using the BJT Effect

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ABSTRACT

This work aims to analyze through 2D numerical simulations the minimum drain bias for the onset of the parasitic bipolar transistor (BJT) effect (V_{Latch}) of a Ultra-Thin-Buried-Oxide (UTBOX) Fully-Depleted-Silicon-on-Insulator (FDSOI) transistor used as a Single-Transistor-Dynamic-Random-Access-Memory (1T-DRAM) cell at high temperatures. The buried oxide thickness (t_{BOX}) and silicon film thickness (t_{Si}) variation were also taken into account and initial studies of the retention time (RT) and the data degradation have been performed. It was verified that the latch voltage, the sense margin current, the latch time and the retention time decrease as the temperature rises.

Index Terms: 1T-DRAM, UTBOX, BJT, high temperatures.

1. INTRODUCTION

1T-DRAM cell has been proposed in order to overcome the conventional 1T1C-DRAM scaling challenges [1]. Since it is composed by only one transistor, the 1T-DRAM cell presents better scalability, simpler process and shorter fabrication cycle time, besides it is more compatible with the SOI technology [2].

The floating body memory exploits the parasitic effects (such as the BJT effect, the impact ionization, the GIDL and the GIFBE) inherent in the MOS device to inject charges in into the body [3]. In this work, the BJT effect is used to program the bit '1'. This method has been proposed in order to improve the retention time and sense margin in 1T-DRAM cells [2]. Moreover, this method eliminates the need for a partially depleted body to increase the channel volume. In other words, the BJT method presents the best performance to programming '1' even in a fully depleted device due to its single transistor latch (STL) phenomenon [2, 4].

At low V_D, the UTBOX shows the normal operation. When the V_D is further increased, the subthreshold swing (SS) becomes very steep (SS < 10 mV/dec.) and a hysteresis is developed in the I_D-V_G characteristics. At this moment, impact ionization (II) activates the BJT effect, filling the body with holes. This floating body results in a positive feedback between the impact ionization current and the source-substrate forward biasing. This positive feedback maintains a high drain current (BJT current) even for V_G well below the threshold voltage [5-7], indicating the bit '1' current level.

Similarly, bit '0' means a lower current (BJT is off) due to the removal of holes from the body. In this work, a forward biased junction (FBJ) is used to expel the holes. More information about the physical mechanism of BJT effects for programming the 1-state and the FBJ for programming the 0-state can be found in [3, 5].

Since a high drain bias results in damage to the device due to the impact ionization and other high electric field effects, it forms a limiting factor for good FBRAM (Floating Body Random Access Memory) operation limiting the reliability [3, 8]. On the other hand, a low drain voltage is not sufficient to trigger the BJT effect [9]. Thus, it is necessary to choose the best drain write bias that is enough to store charges in the memory but minimizing the degradation.

Firstly, the usual operational temperature in most of the memory cells is not 25°C, the room temperature, but around 85°C. Moreover, a study at high temperature is also useful in applications such as in aerospace and military ones, in automotive industry and oil exploration. [10]

The impact of channel length and width on V_{Latch} for the BJT effects in 1T-DRAM is well understood [9, 11]. Nevertheless, a systematic simulation study of the t_{BOX} and t_{Si} dependence on V_{Latch} in a UTBOX operating with the BJT effect has not yet been undertaken. Therefore, the study connecting V_{Latch} at high temperatures with t_{BOX} and t_{Si} is timely and essential.

2. DEVICE CHARACTERISTICS AND SIMULATIONS DETAILS

The UTBOX FDSOI devices of this work were based on the ones developed at imec, Belgium. A schematic view of this device is presented in figure 1.

UTBOX devices have a thinner buried oxide thickness (less than 50nm [12]) presenting advantages such as better threshold voltage control, better thermal resistance and easier inducing of the floating body effect.

Nevertheless, the thin buried oxide becomes the behavior of the BOX/substrate interface more influent, but to solve this problem a higher doped region, called Ground Plane, is added to minimize the depletion of this interface, resulting in a greater control of the channel by the substrate without, however, interfering in the device operation by that depletion capacitance. [13]

The device operation was modeled using 2D numerical simulations [14] and the transistors have a channel length (L) and width (W) of 150 nm and 1µm, respectively, a gate oxide thickness (t_{OX}) of 5 nm, and a channel doping level (N_A) of $1x10^{15}$ cm^{-3}, which is not intentionally doped. The silicon film thickness ranges from 8 up to 50 nm and the buried oxide thickness was varied from 20 up to 50 nm. These thicknesses were chosen in order to cover the real dimensions: 10 nm of t_{BOX} and 30 nm of t_{Si}.

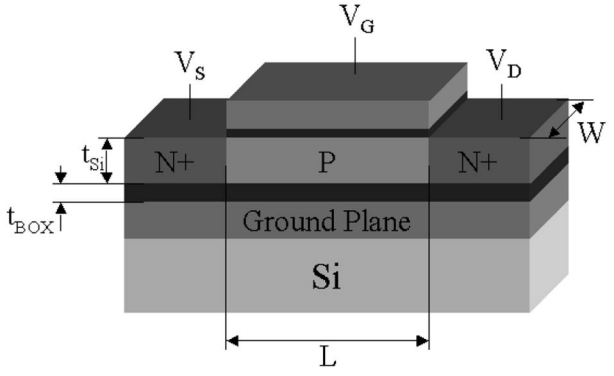

Figure 1. UTBOX structure.

The simulations were performed using the Selberherr's model to provide the BJT effect and the Lombardi one to the mobility adjustment [14]. The ground plane region was considered by calculating the substrate workfunction [15]. The gate stack of 5 nm of PEALD TiN, capped with 100 nm poly-Si and deposited on 5 nm of SiO_2 was modeled with the gate workfunction. In addition, the source and drain extensions regions was included in the doping profile as a concentration of $1x10^{19}$ cm^{-3}. [8]

3. RESULTS AND ANALYSIS

Figure 2 shows the biases used and the drain current (I_D) obtained by simulations for temperatures from 298 K up to 573 K, following the sequence of states and biases indicated by table I. The substrate and the source were grounded. It will be mentioned when different biases are used.

Between each state shown in table I, a holding condition was inserted, in which a gate bias, V_G, of -0.8 V and 0V as the drain bias, V_D, has been applied. starting with a V_G equal to -0.4 V and V_D to 1.2V, performing a read operation, it was verified that there is no charge stored in this cell. This was followed by a writing state (V_G = 0 V and V_D = 1.2 V) and its subsequent reading state (V_G = -0.4 V and V_D = 1.2 V), showing the writing '1' by the BJT method. Then, the erasing (V_G = 1 V and V_D = -1 V), by the FBJ method, and its reading state (V_G = -0.4 V and V_D = 1.2 V), complete the programming scheme, insuring that the holes were expelled.

In this work, a longer writing time (30 ns) than the usual specifications has been used due to the fact that one of the goals is to analyze the write speed as a function of the temperature. Usually the write time is about 10 ns.

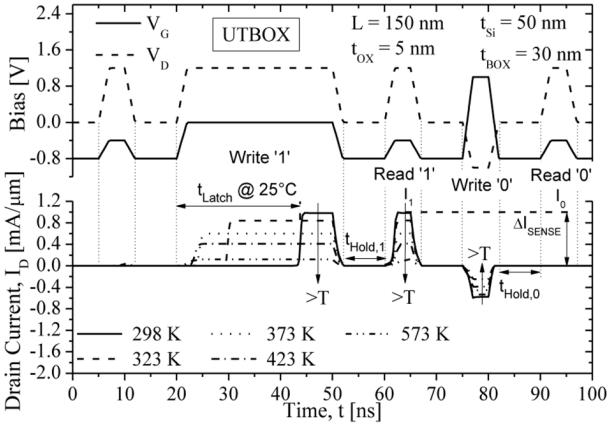

Figure 2. Transient analysis of the 1T-DRAM cell using BJT current.

Table I. Biasing Scheme.

Time [ns]	V_G [V]	V_D [V]	States
5 – 10	-0.4	1.2	Read
20 – 50	0	1.2	Prog. '1'
60 – 65	-0.4	1.2	Read
75 – 80	1.0	-1.0	Prog. '0'
90 – 95	-0.4	1.2	Read

Figure 2 also shows the definition of the latch time, i.e., the time required to activate the BJT effect. Figure 3-a illustrates the definition of the latch voltage, i.e., the minimum drain bias needed to turn on the BJT effect and figure 3-b presents the drain read current over hold time (t_{HOLD}) describing an example of the retention time extraction, in this figure the minimum current used to consider the '1' state was 80 µA/µm and the retention time was about 3 ms.

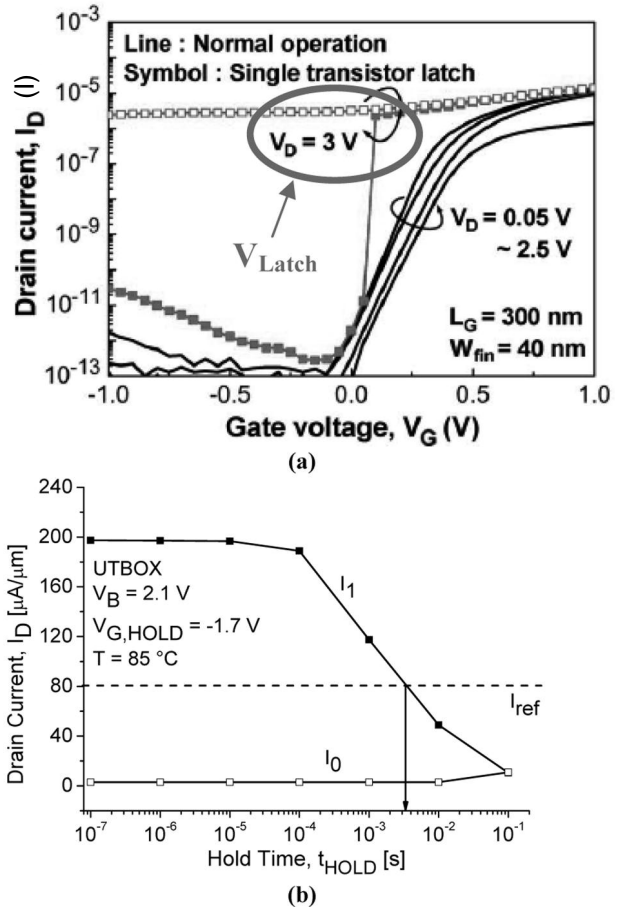

Figure 3.(a) BJT effect triggering in a ID x VG curve. [9] and **(b)** drain read current over hold time [17].

3.1 The BJT effect dependence on Temperature

Figure 4 illustrates the sense margin current, i.e., the difference between the level current in '1' state (I_1) and '0' state (I_0) as a function of the temperature. The sense margin current was decreased by 10 times as the temperature increases. This trend was also concluded in [16] by measurements.

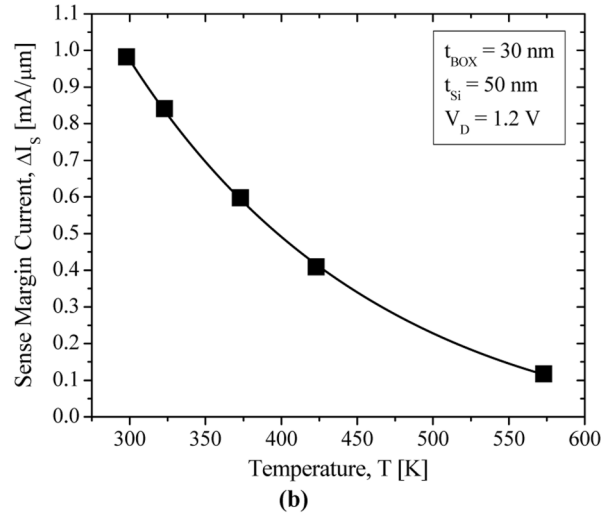

Figure 4. Sense margin current as a function of temperature.

Equation (1) [18] describes the collector current (I_C), or the amplified hole current ($\beta I_{holes,gen}$), of the BJT inherent in the NPN structure of the MOS device under the used conditions. In this structure, the collector refers to the drain, the emitter to the source and the base to the body.

$$I_C = \beta I_{holes,gen} = \alpha_F . I_{SSat} . \left[e^{\left(\frac{q.V_{Body,S}}{k.T} \right)} - 1 \right] \qquad (1)$$

Where α_F is the forward common-base gain, I_{SSat} is the emitter junction reverse saturation current, q is the elementary charge value, $V_{Body,S}$ is the emitter-base voltage and k is the Boltzmann's constant.

As could be explained in [19], through equation (1), it is possible to observe that the I_C decreases at higher temperatures lowering the I_D when the effect is active (state '1'). The hole current ($I_{holes,gen}$) is originated from impact ionization. At high temperatures, the mobility reduces due to higher phonon scattering, generating less electron-holes pairs (the hole current decreases) [19, 20]. Although both currents decrease (I_C and $I_{holes,gen}$) as the temperature increases, but the hole current is far more decreased than the collector current inducing a higher gain (β) [19]. The gain can be calculated through equation (2) [18].

$$\beta = \frac{I_C}{I_{holes,gen}} \qquad (2)$$

Equation (3) describes the abrupt rise of the drain current when the condition β(M-1) approaches unity [15], allowing understanding the relationship between the total drain current and the gain.

$$I_D = \frac{M.I_{CH}}{1 - \beta(M-1)} \qquad (3)$$

where M is the multiplication factor due to the impact ionization and I_{CH} is the channel current associated with the MOS transistor.

While the gain increases, the threshold voltage (V_{TH}) reduces at higher temperatures, anticipating the positive feedback loop. The result is a shorter time to turn on the BJT effect, as can be seen in figure 5 where it is indicated a decrement of one order of magnitude in the latch time at higher temperature [19].

Figure 6 shows the latch time as a function of drain voltage for different temperatures, from where it is possible to see that the latch time required to write '1' also becomes shorter (almost 10 ns shorter in the voltage range considered and at 298 K) as the V_D increases due to the BJT effect . A higher V_D results in a higher electric

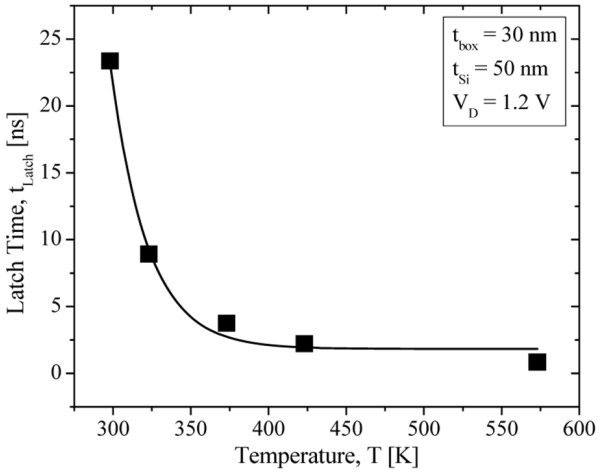

Figure 5. Latch time as a function of temperature.

field in the channel region close to the drain which leads to a greater generation by impact ionization, triggering the BJT effect earlier.

With respect to temperature, for high V_D the difference of t_{Latch} from 298K to 573K decreases (from 10ns down to almost 0) meaning that the latch time depends on the drain voltage and the operating temperature. This behavior was also observed for other devices. Figure 6 can also be used to determine the drain bias needed to reach a latch time previously selected.

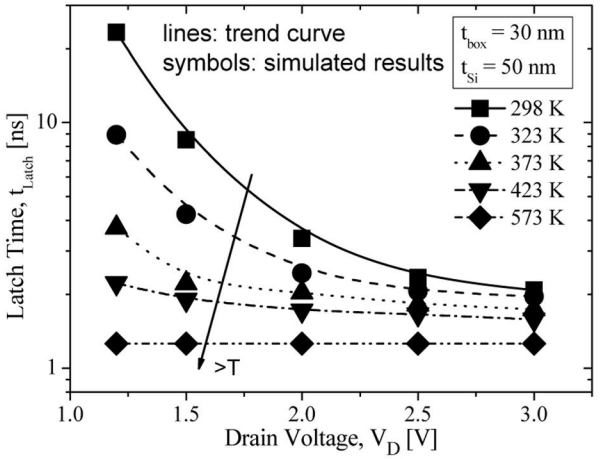

Figure 6. The latch time versus the minimum drain voltage required for writing '1'.

The latch voltage for various buried oxide thickness and silicon film thickness at different temperatures are presented in figures 7-a and -b, respectively.

The variation of V_{Latch} as a function of the t_{Si} can be seen in figure 7-a. For thicker t_{Si} the V_{Latch} will be smaller (about 3.8 times lower at 298 K) due to its higher volume which facilitates the accumulation of holes in the body.

For the V_{Latch} dependence on t_{BOX}, one observes in figure 7-b that the latch voltage increases (50% higher at 298 K) for a thinner buried oxide. As the t_{BOX} decreases,

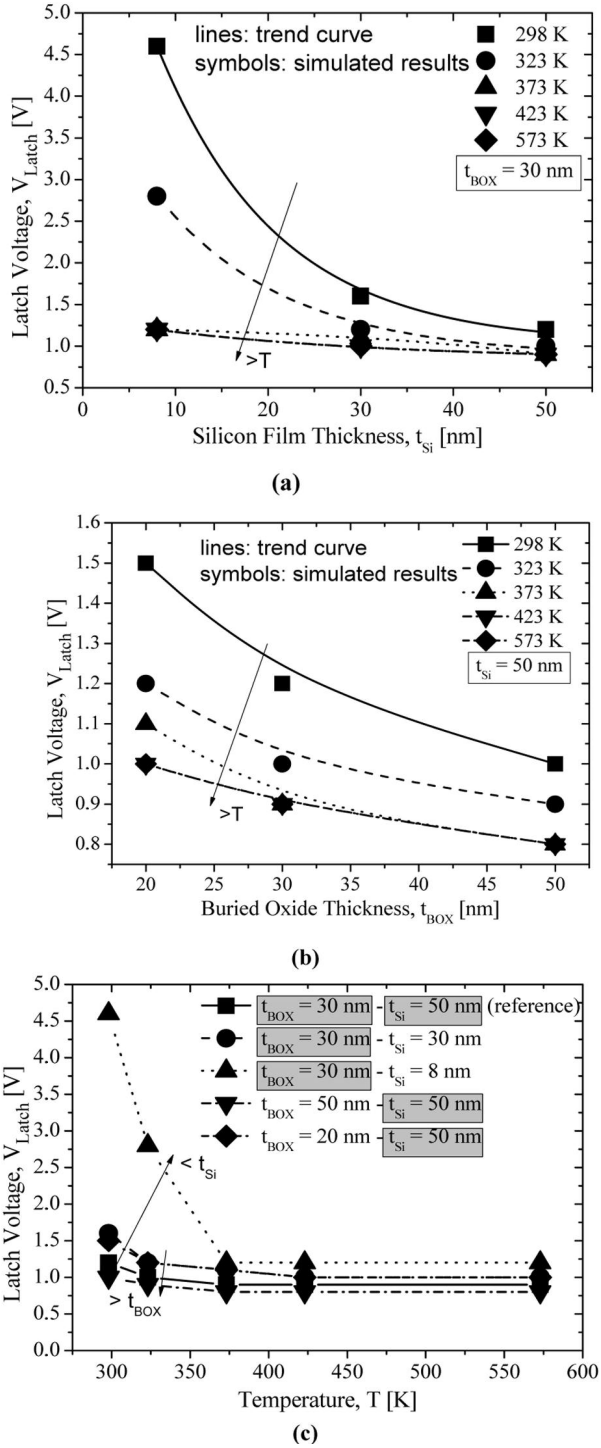

Figure 7. Latch voltage as a function of silicon film thickness **(a)**, buried oxide thickness **(b)** and temperature **(c)**.

the substrate potential becomes nearer to the body and there is an improvement of its control over the channel charges. Thus, the drain bias becomes less influential and a higher value is needed to latch the BJT effect.

Although the increase of temperature causes a reduction in the factor M (the hole current from impact ionization is diminished), the product $\beta*(M-1)$ is increased (due to the β which is more dominant), allow-

ing that a lower lateral electric field is required to trigger the BJT. This means that a lower V_D (reduction of up to 3.8 times) is able to turn on the effect at high temperatures as can be seen in figure 7-c, where it is presented the latch voltage as a function of the temperature for different buried oxide thickness and silicon film thickness.

Another important phenomenon that occurs at high temperatures is the reduction of V_{TH} which can speed up the development of hysteresis.

Figure 8 shows a simple scheme of these effects on the drain current.

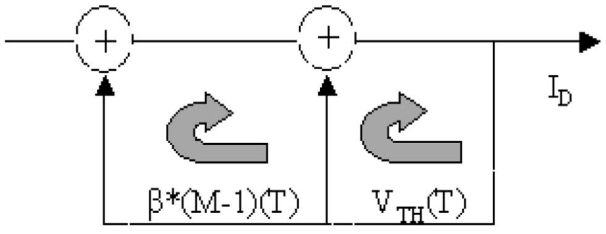

Figure 8. The two positive feedback loops dependence on temperature. The enlargement of β(M-1) and the reduction of V_{TH} due to increased temperature contribute to start the BJT effect for a smaller V_{Latch}.

In this study a strong dependence of V_{Latch} on the substrate bias was also observed. Figure 9 presents the latch voltage as a function of the substrate bias for t_{BOX}=30nm, t_{Si}=8nm and 298 K, that is the worst case as can be seen in figure 7-c. It is possible to verified that a positive voltage applied to the substrate ($V_{BS} > 0$) results in the reduction of about 2.5 times on the minimum drain voltage required to write '1'. This can be explained by feedback loop of the threshold voltage. A positive substrate bias induces a higher body potential which would be, originally, resulted from the first cycles of the impact ionization [16].

According to [17], it was demonstrated by experimental results that the substrate voltage need to be high

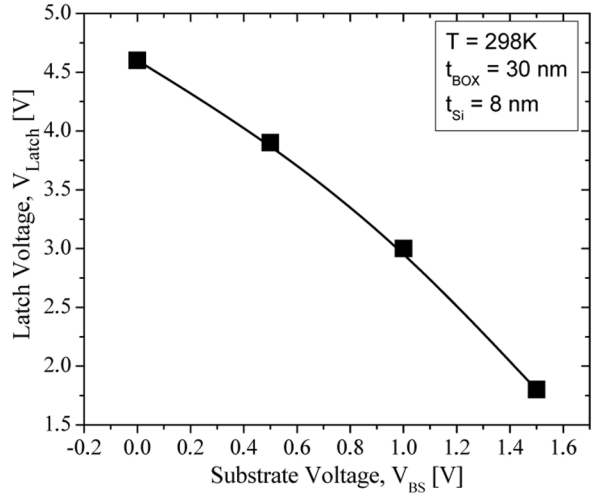

Figure 9. Substrate bias dependence on the latch voltage at 298 K, t_{BOX} = 30nm and t_{Si} = 8 nm.

enough to provide the floating body effect but not so much high in order to avoid the inversion of the back channel, which become impossible the erasing. This means that the ideal substrate bias is with the back channel depleted.

Therefore, it is a good alternative to enable the use of thin-film devices as a memory cell with the characteristics considered [16]. Recently, it has been demonstrated by measurements that the substrate bias can be optimized in order to improve the retention time or the sense margin as well[17].

3.2 Retention Time

Another important parameter to study is the retention time, i.e., the maximum time interval between a programming ($t_{Hold,1}$) or a erasing ($t_{Hold,0}$) and its subsequent reading where the data is still read correctly. In this case, the limiting factor was the $t_{Hold,1}$, it means: there was the degradation of the bit '1'.

Figure 10 presents the retention time dependence on the temperature. To extract this parameter a minimum current of 40μA was used to consider the '1' state.

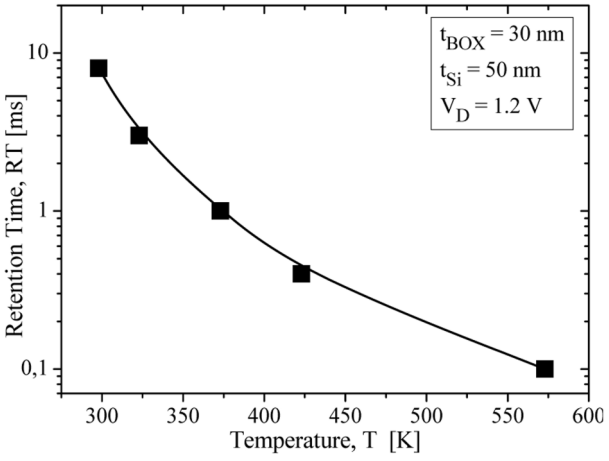

Figure 10. Retention time as a function of the temperature.

According to figure 10 and as can be seen by equations (4) and (5), the retention time decreases (about 2 orders of magnitude according to figure 10) for higher temperatures. Reference [16] also observed this behavior.

According to [17], the main mechanisms involved on the retention time are the generation (for lower gate hold bias) or recombination (for higher gate hold bias) of the carriers originated from the leakage currents, raising or reducing, respectively, the holes concentration in the body during the holding state. In this study, there was a recombination of the carriers. Thus, the observed behavior is due to the increase of the junction leakage current. This means that the holes are removed faster with increasing device operation temperature.

The leakage current of a reverse-biased junction ($I_{leak,pn}$) is expressed by equation (4) [20]

$$I_{leak,pn} = q.A\frac{n_i.W_d}{\tau_e} + q.A\left(\frac{D_n}{\tau_n}\right)^{\frac{1}{2}}.\frac{n_i^2}{N_A} \quad (4)$$

where the intrinsic carrier concentration (n_i) is given by equation (5) [21].

$$n_i = 3.9x10^{16}T^{\frac{3}{2}}e^{-\left(\frac{Eg}{2kT}\right)} \quad (5)$$

In these equations, A is the area of the transversal section of the current, W_d is the depletion-layer width, τ_e is the effective lifetime, τ_n is the electron lifetime, D_n is the electron diffusion coefficient and E_g is the energy gap.

From equation (5), one can observe the strong temperature dependence of n_i, demonstrating the higher leakage current at higher temperature.

3.3 Multiple and sustained read

Figure 11 compares the I_1 in two situations: during a reading state (figure 11-a) and in repeated reading (figure 11-b), where one can see that there is no degradation of the bit '1' in both cases. On the other hand, figure 12 shows the repeated I_0 behavior for shorter (figure 12-a) and longer (figure 12-b) readings, indicating that there was degradation of the bit '0' (in the present case, it appeared after 16 readings) when the reading time becomes significant (here, the cited degradation occurred with the reading time equal to the holding time) compared with the hold time. It means that a '0' degradation occurs during the reading state due to extra hole injection in the body.

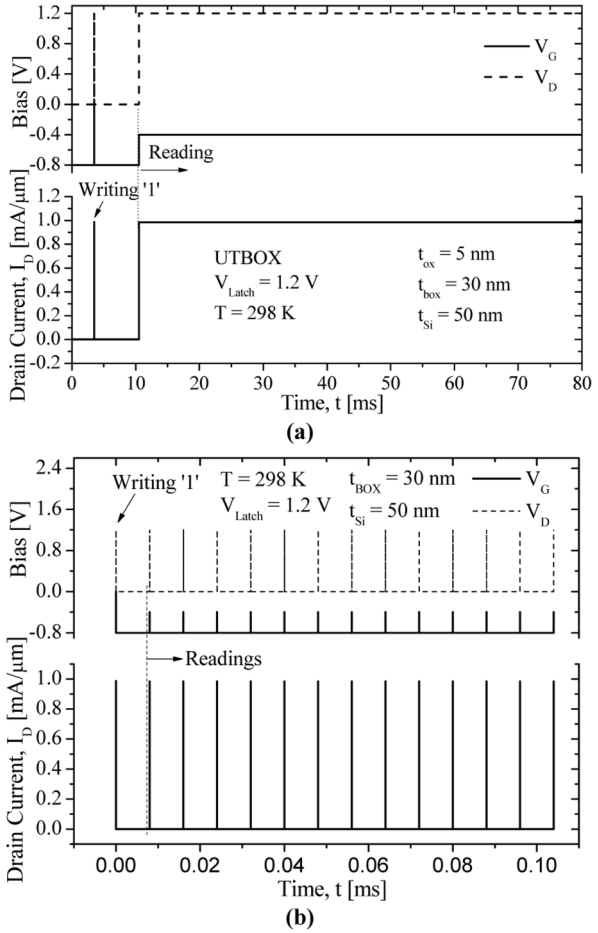

Figure 11. I_1 behavior during a reading state **(a)** and in repeated readings **(b)**.

The reference [22] presented a comparison of the retention time and sense margin using high and low drain biases to read, demonstrating the direct relationship between the impact ionization and the degradation during the read state. And in [17] it was demonstrated that, during the hold time, there may be the degradation of the bit '0' or '1', depending on the gate voltage applied in this state.

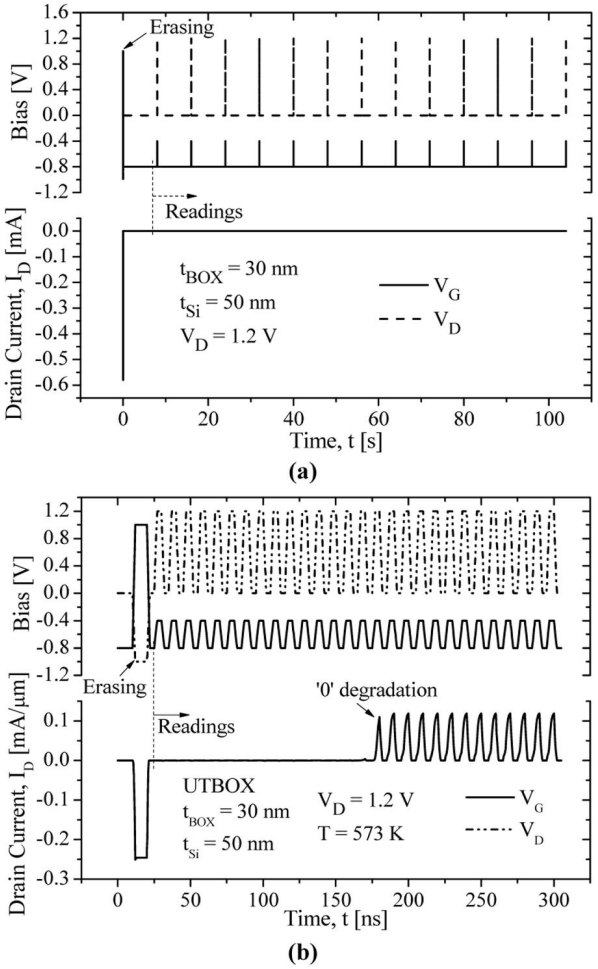

Figure 12. Repeated I_0 behavior for shorter **(a)** and longer **(b)** reading.

As can be seen in figure 13, the maximum time allowed for reading without degrading the '0' state gradually decreased about 4 orders of magnitude as the temperature increases due to a higher injection of holes in the body, which onsets the BJT effect much earlier.

The time needed to read properly by BJT method is about 5 ns. Even for 573 K, which is the worst case (45 ns to degrade '0'), this requirement is achieved.

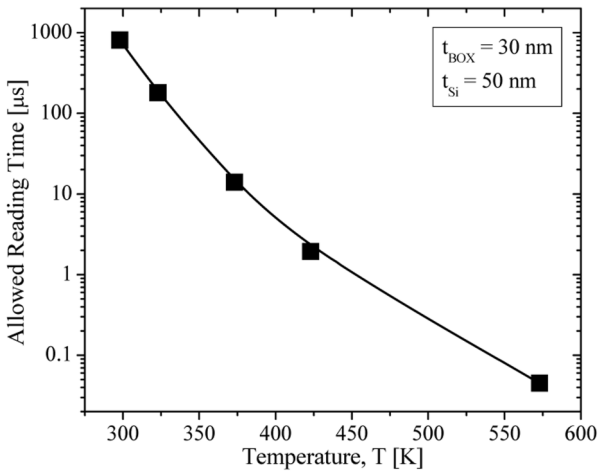

Figure 13. Maximum time of reading without degradation of bit '0' as a function of the temperature.

4. CONCLUSIONS

The temperature influence on the UTBOX working as a 1T-DRAM has been studied by 2D simulations. The latch voltage (V_{Latch}) dependence for the BJT effect was simulated for various buried oxide thicknesses (t_{BOX}) and silicon film thicknesses (t_{Si}). An initial analysis of the data degradation was made.

When the temperature increases, the V_{Latch}, the sense margin current (ΔI_{SENSE}), the latch time (t_{Latch}) and the retention time are decreased. Nevertheless, the device showed satisfactory performance even operating at high temperatures.

The V_{Latch} showed to be strongly dependent on the t_{Si} and t_{BOX}. Although it was observed that the minimum drain voltage required to trigger the BJT increases as the t_{Si} and t_{BOX} become thinner, a positive potential to the substrate (V_{BS}) can reduce this requirement, being a good alternative to overcome this problem, allowing the use of thin film devices as a memory cell.

There is a '0' degradation during the read mode which can limit the multiple read operation, being worse as the temperature increase.

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REFERENCES

[1] D. Fisch, "Innovative Approach to drive Floating Body Z-RAM® Embedded Memory to 32 nm and Beyond", *33rd Annual IEEE International SOI Conference*, October 4th, 2007

[2] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, E. Faraoni, "New Generation of Z-RAM", *IEDM Tech.*, 137, 925 (2007).

[3] M. Jurczak, "Memories on SOI: Floating Body Cell Memory", Training Course, 7*th Workshop of the Thematic Network on Silicon on Insulator technology, Devices and Circuits*, Granada, January 17th, 2011, In: http://www.eurosoi.org/public/T5_EUROSOI2011_MJurczak.pdf.

[4] J.Y. Choi and J. G. Fossum, "Analysis and Control of Floating-Body Bipolar Effects in Fully Depleted Submicrometer SOI MOSFET's", *IEEE Trans. Electron Devices*, 38, 1384 (1991).

[5] M. Bawedin, S. Cristoloveanu, D. Flandre, F. Udrea," Floating-Body SOI Memory Concepts, Physics and Challenges", *ECS Transaction*, 19, 243 (2009).

[6] C.D. Chen, M. Matloubian, R. Sundaresan, B.Y. Mao, C.C. Wei, G.P. Pollack, "Single-Transistor Latch in SOI MOSFET's", *IEEE Electron Device Lett.*, 9, 636 (1988).

[7] D. Flandre and S. Cristoloveanu, "Latch and Hot-Electron Gate Current in Accumulation Mode SOI p-MOSFET's", *IEEE Electron Device Lett.*, 15, 157 (1994).

[8] N. Collaert, M. Aoulaiche, M. Rakowski, B. De Wachter, K. Bourdelle, B.-Y. Nguyen, F. Boedt, D. Delprat, M. Jurczak, "Analysis of Sense Margin and Reliability of 1T-DRAM Fabricated on Thin-Film UTBOX Substrates", *IEEE Int. SOI Conference*, 1 (2009).

[9] D.-I. Moon, S.-J. Choi, J.-W. Han, S. Kim, Y.-K. Choi, "Fin-Width Dependence of BJT-Based 1T-DRAM Implemented on FinFET", *IEEE Electron Dev. Lett.*, 31, 909 (2010).

[10] M.E. Kaamouchi, M.S. Moussa, J.P. Raskin, D. Vanhoenacker-Janvier, "Zero-Temperature Coefficient Biasing Point of 2.4 GHz LNA in PD SOI CMOS Technology", *Microwave Conference*, p.1101 (2007).

[11] T.-S. Jang, J.-S. Kim, S.-M. Hwang, Y.-H. Oh, K.-M. Rho, S.-J. Chung, S.-O. Chung, J.-G. Oh, S. B., J. Kwon, D. Kim, M. Nagoga, Y.-T. Kim, S.-Y. Cha, S.-C. Moon, S.-W. Chung, S.-J. Hong, S.-W. Park, "Highly scalable Z-RAM with Remarkably long data retention for DRAM application", in *VLSI Symp. Tech. Dig.*, 234 (2009).

[12] O. Kononchuk, "Precise Oxide Dissolution", US2010/-0193899 A1, 5 Agosto 2010.

[13] T. Ohtou, T. Saraya, T. Hiramoto, Variable-Body-Factor SOI MOSFET with Ultrathin Buried Oxide for Adaptive Threshold Voltage and Leakage Control, *IEEE Transactions on Electron Devices*, Janeiro 2008. 40-47.

[14] ATLAS Device Simulation, User's Manual, version 5.14.0.R, Silvaco International, Santa Clara (2010).

[15] J. P. Colinge, *Silicon on Insulator Technology: Materials to VLSI*, 3rd edition, p.210, Springer, New York (2004).

[16] Z. Lu, N. Collaert, M. Aoulaiche, B. De Watcher, A. De Keersgieter, W. Schwarzenbach, O. Bonnin, K.K. Bourdelle, B.-Y. Nguyen, C. Mazure, L. Altimine, M. Jurczak, "A Novel Low Voltage Biasing Scheme for Double Gate FBC Achieving 5s Retention and 10^{16} Endurance at 85°C", *IEDM Techn. Digest*, 288 (2010).

[17] L.M. Almeida, K.R.A. Sasaki, M. Aoulaiche, N. Collaert, E. Simoen, C. Claeys, J.A. Martino, M. Jurczak, "The Dependence of Sense Margin and Retention Time on the Front and Back Gate", in Proceedings of 8*th Workshop of the Thematic Network on Silicon on Insulator technology, Devices and Circuits*, 23 (2012).

[18] J. P. Colinge and C. A. Colinge, *Physics of Semiconductor Devices*, p.265, Springer, New York (2006).

[19] L.M. Almeida, K.R.A. Sasaki, M. Aoulaiche, E. Simoen, C. Claeys, J.A. Martino, "Analysis of UTBOX 1T-DRAM Memory Cell at High Temperatures", *ECS Transactions*, 39, 61 (2011).

[20] S. M. Sze, *Physics of Semiconductor Devices*, 2nd edition, p.91, J. Willey & Sons Eds, New Jersey (1981).

[21] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd edition, p.56, J. Willey & Sons Eds, New Jersey (1986).

[22] L.M. Almeida, M. Aoulaiche, K.R.A. Sasaki, T. Nicoletti, M.G.C. de Andrade, N. Collaert, E. Simoen, C. Claeys, J.A. Martino, M. Jurczak, "Comparison between low and high read bias in FB-RAM on UTBOX FDSOI Devices", *Proceedings of 13th Ultimate Integration on Silicon*, p.85 (2012)