Impact of the Series Resistance in the I-V Characteristics of Junctionless Nanowire Transistors and its Dependence on the Temperature

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ABSTRACT

The effect of the source/drain parasitic resistance (R_S) on the *I-V* characteristics of Junctionless Nanowire Transistors (JNTs) has been evaluated through experimental and simulated data. The impact of several parameters such as the temperature, the fin width, the total doping concentration, the source/drain length and the source/drain doping concentration on R_S has been addressed. The source/drain parasitic resistance presented by JNTs was compared to the one presented by classical inversion mode (IM) triple gate devices, showing opposite behavior with the temperature variation in IM triple transistors and JNTs. In the latter, a reduction on R_S is noted with the temperature increase, which is related to the incomplete ionization. This effect inhibits the presence of a Zero Temperature Coefficient (ZTC) operation bias in the Junctionless devices.

Index Terms: Junctionless, series resistance, incomplete ionization, zero temperature coefficient.

I. INTRODUCTION

The continuous miniaturization of the MOS technology has allowed for the use of planar transistors over a wide range of analog and digital circuits since the 80's [1]. The continuous scaling of such structure has, therefore, imposed several technological limits to the application of planar MOS devices for nodes beyond 22 nm [2]. In extremely shorter devices, part of the depletion charge is no longer governed by the gate and is controlled by the source/drain depletion regions. Aiming at improving the gate dominion over the channel charge, devices with more than one gate have been developed. The so-called multiple gate transistors such as double gate FinFETs, and Trigates constitute one of the better approaches to be employed in sub-22 nm technologies since they are able to reduce sensitively the short channel effects thereby increasing the gate control over the channel charge.

For devices with even smaller channel length, the application of Inversion Mode (IM) multiple gate transistors is quite challenging since the source and drain implantations must be carried out in extremely precise thermal and doping conditions, otherwise part of the impurities can diffuse into the channel region. The diffusion-related problems have been addressed through the development of the Junctionless Nanowire Transistor (JNT) [3]. Besides eliminating such problems, the JNT facilitates the fabrication process since it presents no doping gradients. Although the JNT is a silicon nanowire surrounded by gate oxide and gate material like several others multigate transistors, it presents a constant heavy doping concentration in the order of 10^{19} cm^{-3} from source to drain, i.e. source, channel and drain exhibit the same dopant type and concentration and there are no junctions [3]. The longitudinal-sections of the schematic views from both an inversion mode triple-gate device and a Junctionless transistor are shown in Figure 1.

Several recent studies [4-9] have shown advantages of JNTs over IM devices. Improved short channel effects leading to an ideal subthreshold slope and reduced DIBL are reported in [4-6] whereas its reduced electric field over IM transistors is addressed in [7]. References [8-9] demonstrate the better analog properties and lower harmonic distortion exhibited in JNTs with respect to IM device. Also, Junctionless devices have shown an interesting behavior with the temperature variation as described in [10-11]. JNTs present no "Zero Temperature Coefficient" (ZTC) operation point as usually observed in inversion mode transistors, i.e. they do not have a gate to source bias (V_{GS}) for which the drain current (I_{DS}) is always the same independently on the temperature.

Another parameter extremely important for the analog operation of the devices is the series resistance (R_S). This parameter can be divergent in JNTs and IM devices due to the different doping concentration observed in the source/drain of the devices and the absence of junctions

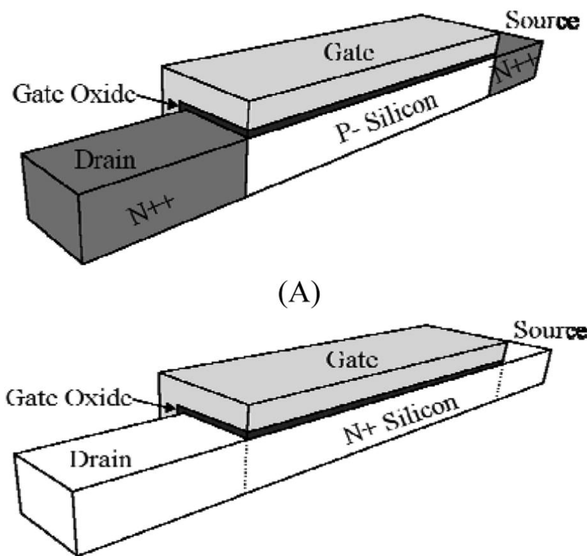


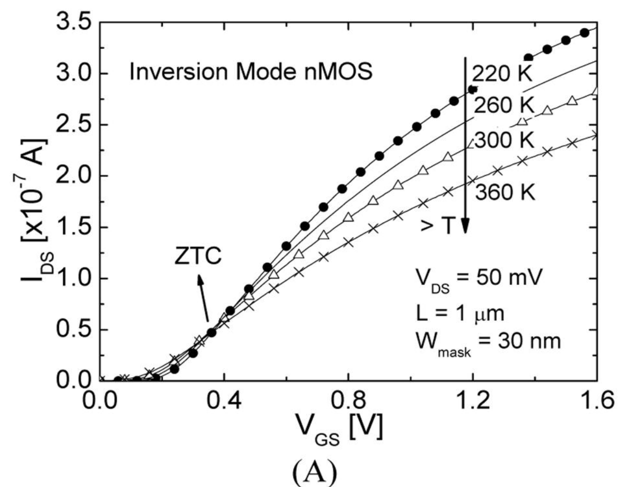
Figure 1. Cross-section of the schematic view of both **(A)** a classical Inversion Mode Trigate transistor and **(B)** an nMOS Junctionless device.

presented by the former one. This paper aims at evaluating for the first time R_S from JNTs through experimental data and three-dimensional device simulations comparing the results to the ones obtained for inversion mode Trigate transistors of similar dimensions biased at different temperatures. The total series resistance is not only influenced by the source and drain regions' resistivity dependence on the temperature, but also to the contact resistance which can exhibit Schottky behavior in experimental devices [12]. The overall analysis intends to clarify the whole of R_S in the *I-V* characteristics of both devices making explicit the differences observed as a function of the temperature (T), the effective fin width and the source and drain lengths (L_{SD}).

II. DEVICES CHARACTERISTICS AND MEASUREMENTS

Along the current work, experimental *I-V* characteristics were obtained from IM and JNTs. The measured transistors were fabricated in standard SOI wafers according to the process briefly described in [13] and present channel length (L) of 1 μm, mask fin width (W_{mask}) of 30 nm, silicon and oxide thicknesses of 10 nm. In the beginning of the fabrication process, the silicon layer thickness (t_{Si}) was thinned down to 10~15 nm through sacrificial oxidation and wet removal and molded into nanoribbons through electron beam lithography. In the sequence, an ion implantation was performed to dope the active region. Junctionless devices present constant n-type doping concentration (N_D) from source to drain (devices were produced with $N_D = 3X10^{19}$ cm^{-3} and $5X10^{19}$ cm^{-3}) whereas inversion mode transistors exhibit a P$^+$ doping concentration of about $N_A = 1X10^{18}$ cm^{-3} in the channel region and an n-type doping concentration of $5X10^{20}$ cm^{-3} in the source/drain regions. The threshold voltage (V_{TH}) was adjusted through the use of P$^+$ and N$^+$ types polysilicon as gate material in JNTs and IM devices, respectively, and resulted in the order of 0.40 V for JNTs and around 0.65 V for IM devices at room temperature. In both transistors, the effective fin width (W_{fin}) is expected to be 15~20 nm smaller than the mask width due to intentional linewidth loss during the fabrication process [13]. Due to the presence of a top and two sidewall gates, the total channel width is estimated to be $W = 2t_{Si} + W_{fin}$.

The measured curves of the drain current as a function of the gate voltage for both IM and JNTs are exhibited in Figure 2 (A) and (B), respectively, at drain voltage (V_{DS}) of 50 mV and several temperatures from 220 K up to 470 K. From the figures it can be observed that the temperature increase is followed by a raise of I_{DS} in JNTs and a reduction of I_{DS} in IM devices. As previously mentioned, unlike the experimental curves of I_{DS} *vs.* V_{GS} from IM transistors, the *I-V* characteristics of JNTs present no ZTC. This fact was addressed in [11] and has been correlated to both the smaller mobility of the Junctionless with respect



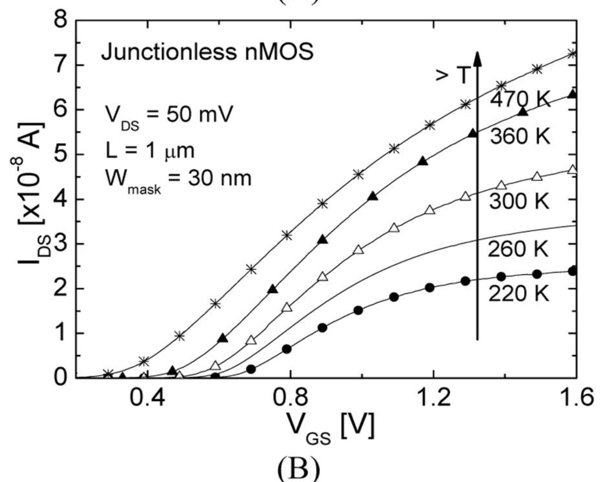


Figure 2. Experimental curves of I_{DS} vs. V_{GS} for **(A)** inversion mode Trigate devices and **(B)** nMOS Junctionless transistors at several temperatures and V_{DS} = 50 mV.

to inversion mode devices and the higher dependence of the threshold voltage of JNTs with the temperature variation. The higher sensitivity of V_{TH} with T in the Junctionless is confirmed in [14] where it has been shown that JNTs exhibit $|dV_{TH}/dT|$ larger than 1 mV/K whereas IM devices present $|dV_{TH}/dT|$ around 0.6 mV/K and has been attributed to the incomplete ionization.

The parasitic source/drain resistance was extracted from *I-V* curves shown in Figure 2 for both IM and Junctionless transistors according to the method described in [15]. Contrary to several methods described in the literature [16-17], this method is not derived from any analytical expression for the drain current and consists in splitting up the parasitic source/drain resistance from the channel resistance. Indeed, the R_S extraction methods based on analytical models found in the literature were developed essentially for IM devices and cannot be straightly applied to JNTs. The curves of R_S are presented in Figure 3 as a function of the temperature for both classical IM and JNTs. At a first glance in Figure 3, one can see that IM devices present extremely lower parasitic resistance than their Junctionless counterparts. Furthermore, JNTs exhibit a dramatic increase of R_S when lowering the temperature whereas an opposite trend is observed for IM devices. This latter effect is in accordance to the results presented for IM triple gate nMOS FinFETs in [18] where the reduction of R_S with temperature in these devices is assigned to the raise of the carriers mobility. When Junctionless devices with higher doping concentrations are evaluated, one can note that the abrupt increase of the series resistance takes place at lower temperatures and a slight reduction on R_S is observed at room temperature.

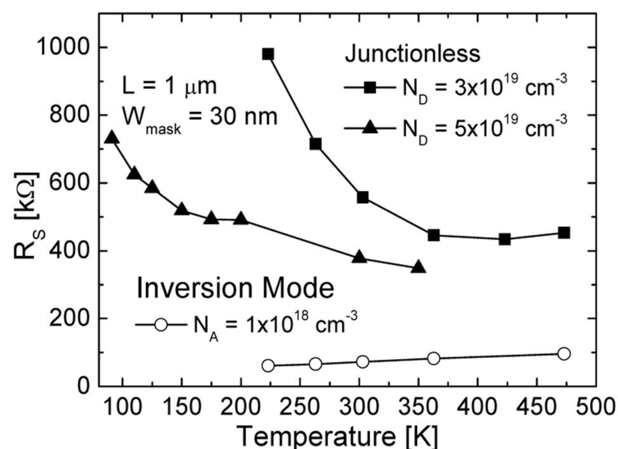


Figure 3. Curves of the parasitic source/drain resistance as a function of the temperature for measured Trigate and Junctionless devices of L = 1 μm and W_{mask} = 30 nm.

III. DEVICES SIMULATIONS VALIDATION

Most papers evaluating the series resistance of inversion mode MOS transistors have shown a decrease of R_S with the temperature which has been attributed to the raise of carriers mobility [17-20]. Only at cryogenic temperatures (T < 100 K) an increase of R_S could be expected due to carriers freeze out [20-21]. For this reason, in this section, an explanation for the abnormal behavior observed in the source/drain parasitic resistance dependence on the temperature of JNTs is proposed.

Tridimensional numerical devices simulations have been performed with the Sentaurus TCAD simulator [22] in order to find out the main mechanisms, which can influence the series resistance of JNTs. The simulated devices present similar physical characteristics to the measured ones such as overall n-type doping concentration of $1X10^{19}$ cm^{-3} and channel length of 1 μm. The gate oxide and the silicon film thicknesses were considered equal to 2 nm and 10 nm, respectively. The effective fin width (W_{fin}) was set to 10 nm. For a first analysis, the source and the drain lengths (L_{SD}) were considered equal to 150 nm and the source and drain contacts were made at the left and right extremities of the device. The threshold voltage has been adjusted by setting the gate material workfunction equal to the one of P^+ polysilicon. In order to make a comparative analysis, IM devices have also been simulated with physical parameters similar to the ones of the Junctionless with exception of the doping concentration which was set to $N_A = 1X10^{18}$ cm^{-3} in the channel and to $N_D = 5X10^{20}$ cm^{-3} in the source and drain regions. The threshold voltage of IM devices was adjusted by considering the use of N^+ polysilicon as gate material. Analytical models accounting for the mobility degradation due to vertical and lateral electrical fields, bandgap narrowing, doping-dependent carrier lifetime and incomplete ionization were considered along the simulations. Since the simulations were done for a qualitative analysis, default coefficients were applied and no optimizations were carried out.

Figure 4 exhibits the simulated curves of the drain current as a function of the gate voltage for inversion mode Trigate devices and Junctionless nanowire transistors at V_{DS} = 50 nm and several temperatures. As it can be seen, despite the different absolute values for I_{DS} obtained in experimental curves from Figure 2 and simulated data of Figure 4 because of the un-optimized model coefficients, a similar trend of I_{DS} with the temperature variation is obtained in both figures for JNTs and IM devices. Moreover, a clear ZTC operation point is observed in the simulated curves from IM devices whereas no ZTC is presented by JNTs. For this reason, the simulations could be validated.

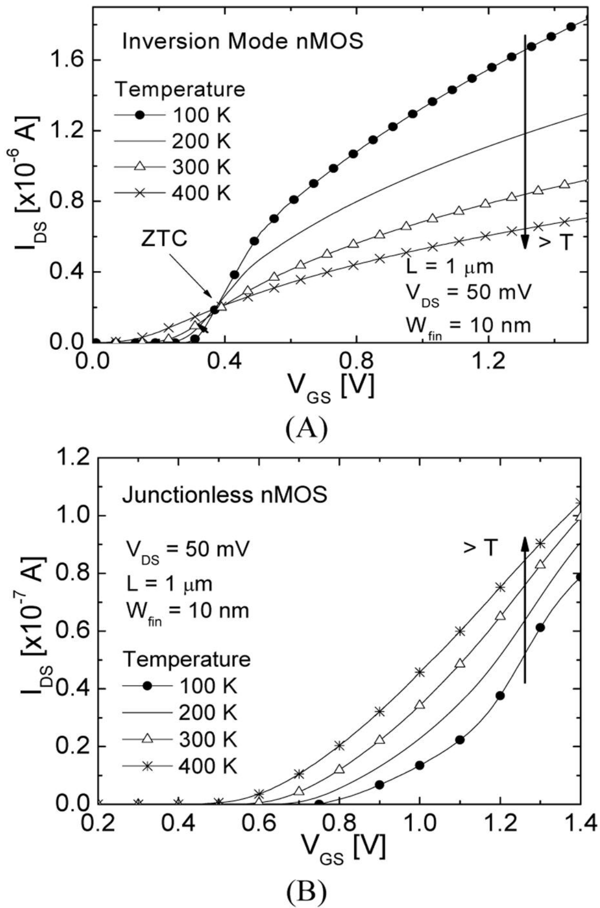


Figure 4. Simulated curves of I_{DS} vs. V_{GS} for **(A)** inversion mode Trigate devices and **(B)** nMOS Junctionless transistors at several temperatures and V_{DS} = 50 mV.

IV. SERIES RESISTANCE ANALYSIS

Although the channel region of JNTs contains a higher doping concentration than IM devices, JNTs usually have a lower doping concentration in their source/drain regions than their IM counterparts. According to references [23-25], silicon devices doped in the range between 10^{16} cm^{-3} to 10^{19} cm^{-3} are more susceptible to the occurrence of the incomplete ionization of dopant atoms. This phenomenon is more effective at cryogenic temperatures and can influence source and drain resistivity [23].

Incomplete ionization takes place when the thermal energy is not enough to ionize all the dopant atoms in the silicon layer. In this case, the effective doping concentration (N_D^+) becomes smaller than the total doping concentration and depends on the quasi-Fermi level for the electrons (E_{Fn}), the donor ionization energy (E_D) and the temperature as demonstrated in expression (1) where k is the Boltzmann constant. The reduction on the effective doping concentration inherently results in a raise of the silicon resistivity as described by (2).

$$N_D^+ = \frac{N_D}{1 + 2\exp\left(\frac{E_{Fn} - E_D}{kT}\right)} \quad (1)$$

$$R = \frac{1}{q\mu_n N_D^+} \quad (2)$$

The ionization ratio of the carriers, defined as the ratio of ionized dopants to the total doping concentration, has been calculated for the simulated JNTs doped with arsenic according to the model described in [25] and is presented as a function of the doping concentration in Figure 5. As one can see, for doping concentrations in the order of 10^{19} cm^{-3}, the arsenic ionization ratio is lower than 100 % even at room temperature, which can influence on R_S of JNTs. On the other hand, for total doping

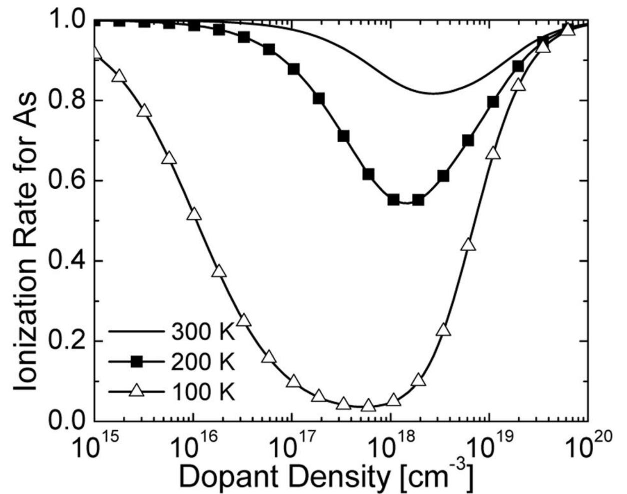


Figure 5. Calculated ionization ratio for As as a function of the dopant density at several temperatures.

concentrations higher than 10^{20} cm^{-3}, the incomplete ionization can be neglected. As the source/drain regions of inversion mode transistors usually fit this condition, the series resistance is only dependent on the mobility variation. In fact, the dependence of the ionization ratio on the total doping concentration can explain the increase of R_S perceived at lower temperatures in devices with larger N_D as shown in the experimental results from Figure 3.

Aiming at clarifying the effect of the incomplete ionization in the series resistance of JNTs, the series resistance was extracted for the simulated Junctionless nanowires with and without considering the impact of the incomplete ionization and is presented in Figure 6 as a function of the temperature. The curve of R_S *vs.* T for an inversion mode Trigate transistor of similar dimensions is also presented in Figure 6 considering the incomplete ionization model. From the figure, one can observe that by disabling the incomplete ionization model from the Junctionless device, its series resistance presents a mean-

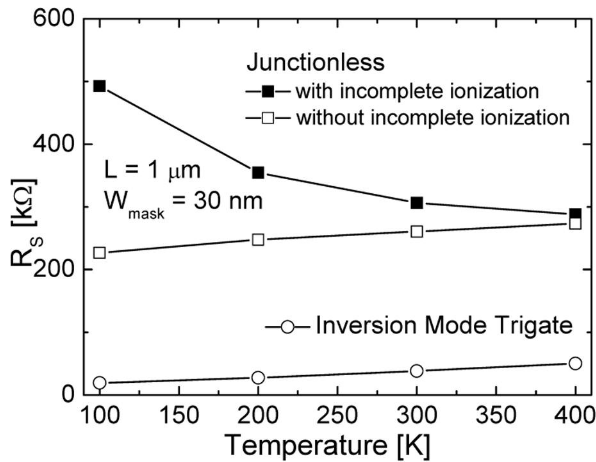
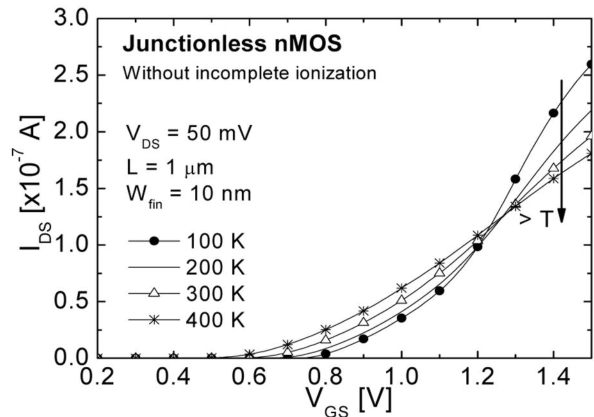


Figure 6. Curves of R_S *vs.* T for simulated IM and JNTs of W_{mask} = 30 nm with and without considering the incomplete ionization.

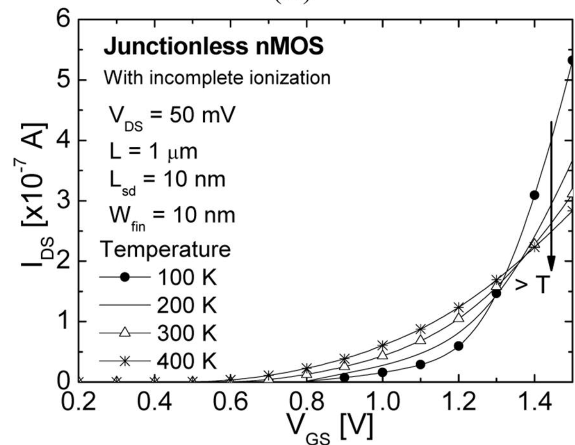
ingful reduction mainly at lower temperatures where the incomplete ionization effect is more pronounced. Anyway, the effect of the incomplete ionization can be distinguished even at room temperature due to the low source/drain doping concentration of the Junctionless. At 400 K, nevertheless, the JNT exhibited a similar R_S when considering or not the incomplete ionization model, indicating that at higher temperatures the ionization ratio in silicon with doping concentration around 10^{19} cm^{-3} approaches unity.

Indeed, the curves from Figure 6 show that the series resistance of JNTs and IM devices present a similar behavior with the temperature when the incomplete ionization is disabled in the former one. In this case, R_S is determined by the increase of the carriers' mobility with the temperature reduction. The inherently higher R_S presented by JNTs is related to its lower source/drain doping concentrations. In order to verify the effect of the incomplete ionization in the *I-V* characteristics of the Junctionless, the curves of the drain current as a function of the gate voltage at V_{DS} = 50 mV were simulated at several temperatures for the Junctionless devices without considering this effect as shown in Figure 7 (A). According to the figure, when the incomplete ionization is neglected a clear ZTC bias is observed around V_{GS} = 1.25 V, indicating that the absence of zero temperature coefficient in JNTs can be correlated to their large R_S .

In order to confirm if the $I_{DS} - V_{GS}$ characteristics of the Junctionless transistors are severely affected by the series resistance, the devices were simulated with several source/drain lengths (L_{sd}) considering and neglecting the incomplete ionization. As the simulated structures present source and drain contacts at the extremities of the active region the series resistance of such devices is given by expression (2) multiplied the source and drain areas, resulting in (3)



(A)



(B)

Figure 7. Simulated curves of I_{DS} vs. V_{GS} for nMOS Junctionless transistors of **(A)** *Lsd* = 150 nm without considering the incomplete ionization and of **(B)** *Lsd* = 10 nm considering the incomplete ionization.

$$R_s = \frac{1}{q\mu_n N_D^+} \frac{2L_{sd}}{H_{fin}W_{fin}} \quad (3)$$

The curves of the series resistance as a function of the source/drain lengths for IM devices and JNTs with and without the incomplete ionization model are presented in Figure 8. For the inversion mode devices and the Junctionless transistors without considering the incomplete ionization, R_S reduces slightly for lower values of L_{sd} and the temperature variation has a similar influence for any L_{sd}, making the curves of R_S *vs.* L_{sd} for each device present the same slope for different T. By applying the incomplete ionization in JNTs, the curves of R_S *vs.* L_{sd} for several temperatures acquire different slopes. A higher slope is observed at lower temperatures due to the stronger effectiveness of the incomplete ionization. For smaller source/drain lengths, the series resistance of the Junctionless transistors considering or not the incomplete ionization present a similar value, which is slightly larger than the one exhibited by inversion mode devices. Thus, it can be concluded that for $L_{sd} \leq 10$ nm, the resistance derived from incomplete ionization rep-

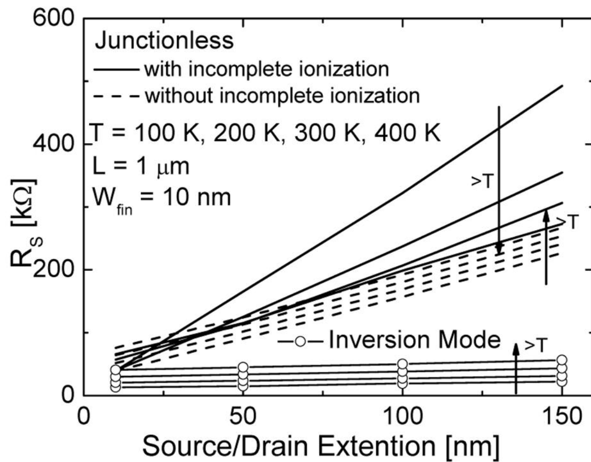


Figure 8. Curves of R_S *vs.* L_{sd} for simulated inversion mode and Junctionless nanowire transistors of L = 1 μm and W_{fin} = 10 nm.

resents only a small part of R_S. Figure 7 (B) shows the curves of I_{DS} *vs.* V_{GS} for a Junctionless transistor with L_{sd} = 10 nm at different temperatures applying the incomplete ionization model. Similarly to Figure 7 (A), a ZTC bias can also be seen in Figure 7 (B).

The effect of the incomplete ionization can also be noted by plotting the curves of R_S as a function of the temperature for Junctionless and inversion mode devices with different source/drain lengths as shown in Figure 9. As it can be seen, for smaller values of L_{sd}, the series resistance of the JNT approaches to the one of the IM transistor independently on the temperature. As L_{sd} is increased, there is an inherent raise on the R_S of the JNT, which is related with the lower doping concentration with respect to the source and drain of the IM device. Also, for longer L_{sd}, R_S presents an increase with the temperature lowering for the whole T range, which can be directly correlated to the higher effectiveness of the incomplete ionization. When T is varied from 400 K down to 100 K Junctionless of L_{sd} = 150 nm, presents a raise of almost 200 kΩ in R_S whereas for L_{sd} = 10 nm R_S reduces about 20 kΩ for in the same temperature range.

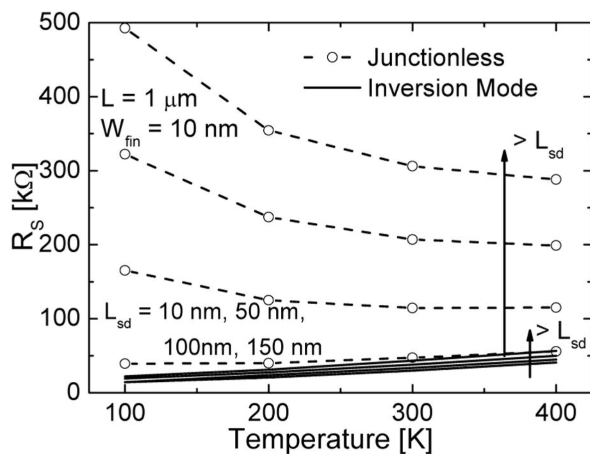
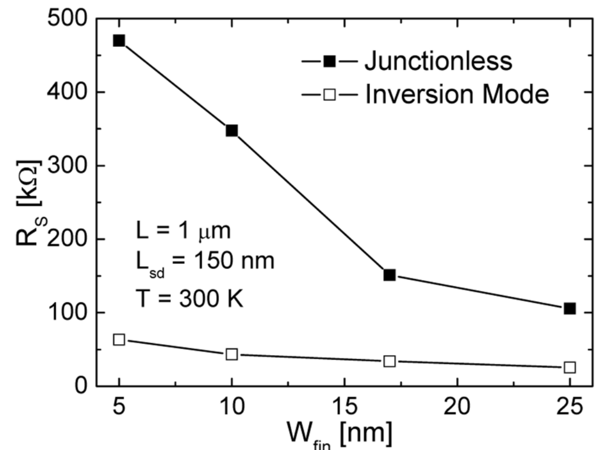


Figure 9. Curves of the series resistance as a function of the temperature for simulated IM and JNTs of L = 1 μm and W_{fin} = 10 nm with several L_{sd}.



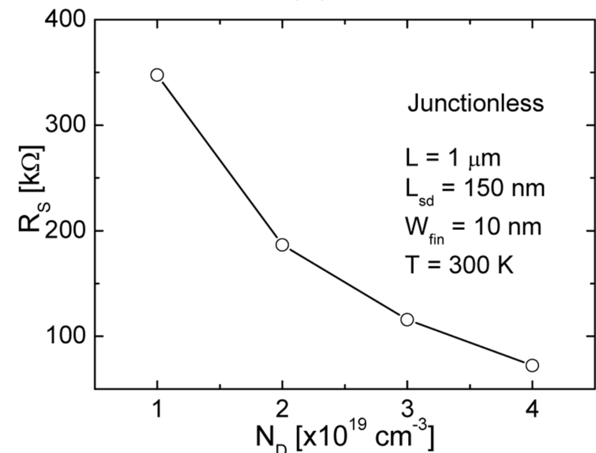


Figure 10 Simulated curves of the series resistance for simulated JNTs of L = 1 μm and L_{sd} = 150 nm as a function of **(A)** the fin width and **(B)** the doping concentration.

The effects of the fin width and doping concentration variations on the parasitic source/drain resistance has also been evaluated through tridimensional devices simulations as exhibited in Figure 10 for transistors of L = 1 μm at T = 300 K. Despite both Junctionless devices and inversion mode transistors exhibit a reduction of R_S with the raise of W_{fin}, the dependence of the series resistance on W_{fin} is much more pronounced in Junctionless devices, indicating that wider JNTs could be more interesting for analog applications. However, this assumption is no longer valid since Junctionless devices present a huge V_{TH} dependence on W_{fin}, leading to negative threshold voltages when W_{fin} > 20 nm for N_D = 10^{19} cm^{-3} as described in [14]. Anyway, as the resistivity is proportional to the inverse of the carrier concentration, the R_S of JNTs suffers a diminution with the raise of the doping concentration of the devices as one can observe in Figure 10 (B).

V. SOURCE/DRAIN DOPING CONCENTRATIONS

Although the concentration of the devices has been varied along the entire active region, the devices could be produced with channel doping concentration in the order of 10^{19} cm^{-3} and source/drain regions more strongly doped aiming at a decrement of the overall series resistance with the reduction of the incomplete ionization [4,26]. Figure 11 shows the series resistance of Junctionless nanowire devices as a function of the source/drain doping concentration (N_{sd}) with the channel doping concentration kept at N_D =1X10^{19} cm^{-3}. As one can observe, only by changing N_{sd} a huge variation in R_S is obtained. The increase of the source/drain concentration from 1X10^{19} cm^{-3} up to 5X10^{19} cm^{-3} implies a reduction on R_S of about 65 %. On the other hand, the increment of N_{sd} from 2X10^{20} cm^{-3} up to 5X10^{20} cm^{-3} results in a raise of R_S smaller than 10 %, which indicates that the experimental devices could be fabricated with N_{sd} around 2X10^{20} cm^{-3}, to minimize the series resistance related

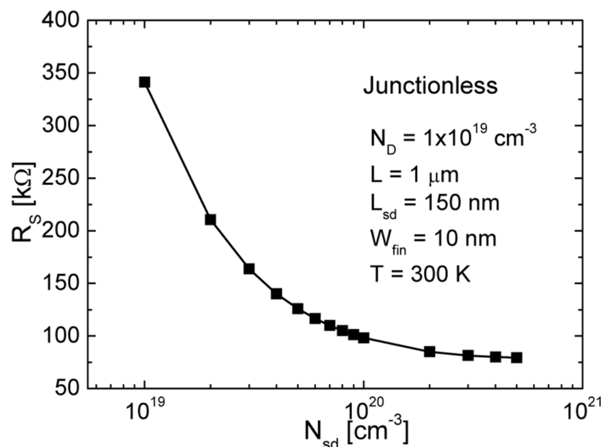


Figure 11. Simulated curves of R_S as a function of the source/drain doping concentration (N_{sd}) for simulated Junctionless devices of L = 1 μm and W_{fin} = 10 nm.

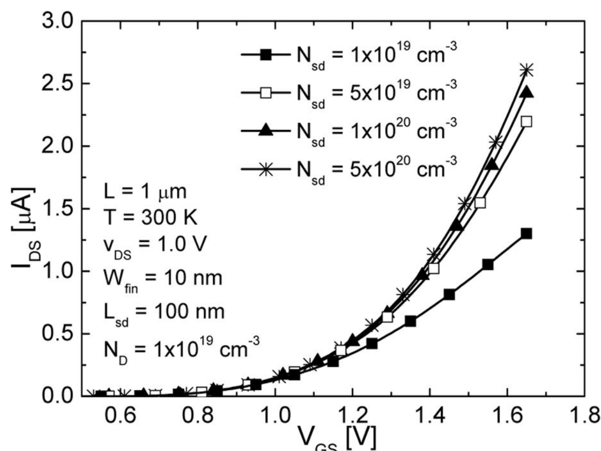


Figure 12. Curves of I_{DS} *vs.* V_{GS} for simulated JNTs with different source/drain concentrations (L = 1 μm and W_{fin} = 10 nm).

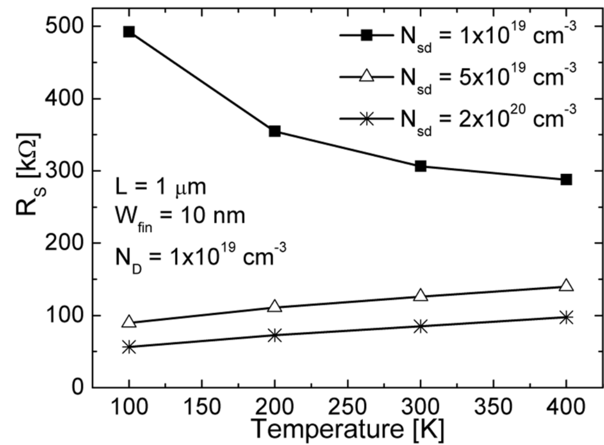


Figure 13. Series resistance as a function of the temperature for JNTs with different source/drain doping concentrations (L = 1 μm, W_{fin} = 10 nm and N_D = 1X10^{19} cm^{-3}).

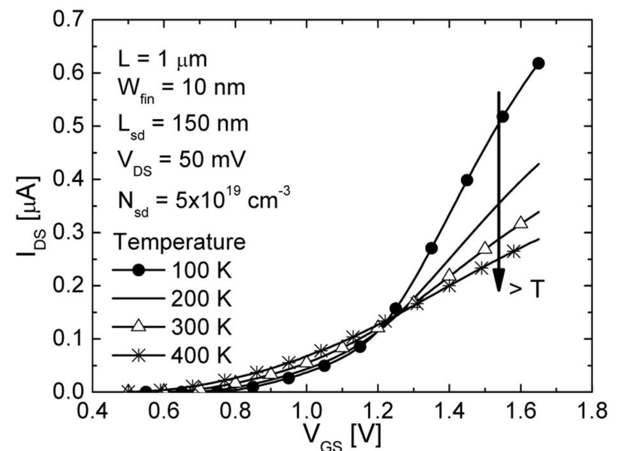


Figure 14. Curves of I_{DS} *vs.* V_{GS} for simulated Junctionless nanowire transistors with N_{sd} = 5X10^{19} cm^{-3} (L = 1 μm, W_{fin} = 10 nm, V_{DS} = 50 mV and N_D = 1X10^{19} cm^{-3}).

The impact of the source/drain doping concentration on the drain current of the JNTs can be seen in Figure 12, which exhibits I_{DS} *vs.* V_{GS} for devices with different N_{sd}. When N_{sd} is varied in one order of magnitude from 10^{19} up to 10^{20} cm^{-3} an increase superior than 40 % is observed in the drain current at V_{GS} = 1.6 V. Indeed, at room temperature the impact of the incomplete ionization on R_S is not so pronounced as in cryogenic temperatures. In order to evaluate the dependence of the N_{sd} on R_S with the temperature variation, the series resistance has been extracted as a function of the temperature for Junctionless devices with several source/drain doping concentrations as shown in Figure 13.

As one can observe in the figure, the effect of the incomplete ionization can be clearly seen for source/drain doping concentrations around 1X10^{19} cm^{-3}. When N_{sd} is increased to 5X10^{19} cm^{-3}, the series resistance no longer presents a raise with the reduction of the temperature, indicating the lighter influence of the incomplete ionization. This effect is similar to the one obtained in Figure 7 (A)

when not considering the incomplete ionization, which leads to the conclusion that for N_{sd} equal or higher than $5X10^{19}$ cm^{-3} the incomplete ionization can be neglected in JNTs. Finally, one can see a clear ZTC bias in the I_{DS} *vs.* V_{GS} curves from Figure 14 for Junctionless devices with channel doping concentration of $1X10^{19}$ cm^{-3} and source/drain doping concentration of $5X10^{19}$ cm^{-3}, which is associated to the negligible incomplete ionization.

VI. CONCLUSIONS

An exhaustive evaluation of the parasitic source/drain resistance (R_S) of Junctionless nanowire transistors (JNTs) was performed considering the influence of the temperature (T), the source/drain length (L_{sd}), the fin width (W_{fin}) and the total and the source/drain doping concentrations (N_D and N_{sd}, respectively). The overall study compared experimental and simulated data of JNTs and classical inversion mode (IM) Trigate devices. Junctionless transistors have shown higher R_S than IM transistors of similar dimensions, which is essentially related to the lower source/drain doping concentration (N_{sd}). Besides inherently increasing the series resistance, the lower N_{sd} is more susceptible to the occurrence of the incomplete ionization of dopant atoms. Although at room temperature, a raise of the R_S can be attributed to this phenomenon; its occurrence is more pronounced at lower temperatures, where JNTs present an increase of R_S instead of a reduction of the series resistance as observed in IM devices. However, the dependence of R_S on the temperature changes as L_{sd} is varied. For extremely shorter L_{sd}, R_S behaves similarly in JNTs and IM devices. Due to the presence of the incomplete ionization, R_S from JNTs exhibits a stronger dependence with W_{fin} than IM devices. When the influence of N_D on R_S of JNTs is analyzed, an exponential decrease of the series resistance is noted with the N_D raise. Considering the huge influence of the doping concentration on R_S, it is advised the fabrication of JNTs with N_{sd} slightly higher than the doping concentration from the channel region.

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