Fin Cross-Section Shape Influence on Short Channel Effects of MuGFETs

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ABSTRACT

Multiple-gate FETs is normally constructed on pre-etched silicon fins. These devices often present casual width variations along the silicon height; mostly caused by technological limitations of the fin definition process, due to non-ideal anisotropic etch. The resulting devices have, consequently, non-rectangular cross-sections, which can affect their electrical behavior. This work addresses the dependence of fin width non-uniformity on the occurrence of short-channel effects through comparative analysis, based on three-dimensional numeric simulation of non-rectangular cross-section devices. The influence of the fin cross-section shape on electrical parameters showed to be dependent on channel length, becoming more sensible to the fin shape as the channel length is reduced, with better DC performance present on devices with bottom fin width smaller than top fin width due to the higher transconductance and lower output conductance, resulting on higher intrinsic voltage gain. For opposite fin shapes the total gate capacitance present higher values, beneficiating AC analog parameters, such as unit gain frequency.

Index Terms: SOI, MuGFET, Fin Geometry, Electrical Parameters, Short Channel Effects, Nanotechnology.

1. INTRODUCTION

Multiple-gate MOSFETs (MuGFETs), among the many different technologies investigated nowadays, have been developed as a possible answer to further downscale of transistor dimensions, reducing undesirable effects suffered by planar single-gate devices. Short channel effects (SCE) such as threshold voltage roll-off, worsening of drain induced barrier lowering (DIBL) and source/drain leakage currents, together with interconnect capacitance and RC delays, cause the degradation of device parameters. Double and triple gate MuGFET devices are known to have better control of the channel charges, nearly ideal subthreshold slope and reduced threshold voltage roll-off by reducing SCE, allowing better scalability than conventional devices [1,2,3]. Some planar MuGFET non-related SCE issues, such as the perfect alignment between both top and bottom gates as well as the self-alignment of source/drain regions are well known from literature and become mandatory with the channel length shrink to maintain short gate delays [4]. Quasi-planar MuGFETs, like FinFETs possesses the advantage of easier fabrication than planar MuGFETs, allied to the possibility to grow the fin height (i.e. increase the channel surface which leads to higher I_{ON}) without losing substrate area. The use of Silicon-On-Insulator technology (SOI) helps to minimize the degradation of channel charges control by minimizing SCE [5]. Frequently, MuGFETs present width variations along the silicon fin height caused by technological limitations of the fin definition process, as the non-ideal anisotropic etch resulting in non-rectangular fins [6]. Such fin geometry variations adds a new and not well-known variable to the present scenario, affecting the electrical parameters when the device is downscaled. The effect of the fin geometry variations on devices subject to different temperatures where the strain technology is applied has been also reported in the literature [7,8]. Some of the main electric parameters that are affected by fin non-rectangular geometry are transconductance, output conductance, intrinsic voltage gain, gate capacitance and unit-gain frequency, amongst others [9,10,11].

In order to address the impact of the non-rectangular channel geometry when the device dimensions are downscaled, the electrical parameters such as subthreshold swing, drain induced barrier lowering, threshold voltage, transconductance to drain current ratio, I_{ON} and I_{OFF}, transconductance, output conductance, intrinsic voltage gain, intrinsic unit-gain frequency and total gate capacitance, for several different channel lengths are studied through three-dimensional numerical simulations, starting from observed channel device geometries and extrap-

olating to less usual formats as a way to predict other geometries. The paper is organized as follows: section 2 presents some experimental devices from references that suffer from such process precision deficiency from literature and the simulated device structure characteristics adopted in this work; section 3 presents the simulation results obtained alongside the description of methods used to obtain them, followed by discussions of each important aspect observed. The main conclusions are presented in section 4.

2. ANALYZED DEVICE STRUCTURES

From cross-section geometries of n-type SOI MuGFET devices found in references [12,13,14] and the respective schematic shapes presented in figure 1, the non-rectangular geometry of the fins is clear. Based on these three cross-sections, the trapezium geometry was chosen as it better represents the observed experimental shapes. Looking at the shape 3 in figure 1, the concave fin geometry is observed [15]. An approximation to fit this shape is to divide the fin into two regions near at the half height and expressing the silicon fin as two opposite trapeziums combined [16]. The regular and the inverse trapezium fin geometries are studied in this work.

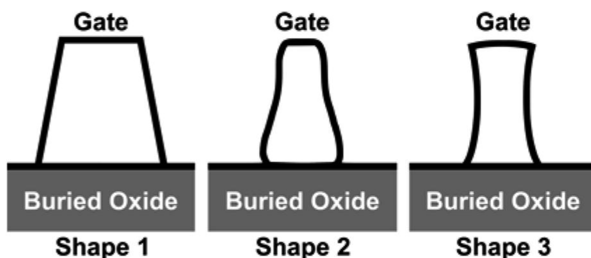

Figure 1. Schematic representations of experimental cross-section fins. Shape 1: SOI FinFET/NanoWire [12,13], Shape 2: sub-5 nm all-around gate SOI MuGFET [14] and Shape 3: NiSi-gated SOI MuGFET [15].

The silicon fin dimensions adopted for simulated devices are close to those of references [12,13]. The summary of device dimensions is presented in table 1. Based in the empirical scaling rule from reference [17], derived from the observed subthreshold behavior of MuGFETs, the silicon fin width must be lower than one third of device's channel length in order to avoid SCE. The fin height (H_{fin}), gate oxide (t_{ox}) and buried oxide (t_{box}) thickness are maintained constant for all set of devices while the width of silicon fin top (W_{top}) and bottom (W_{bottom}) are ranged following the previously mentioned scaling rule. Corner effects are assumed to be negligible for the undoped body [1,18,19]. Two groups of transistors with different fin width ranges are created (type 1 and type 2) to study the relationship between fin width and geometry with the channel length (L) shrink (30, 50, 90, 170, 200, 1000 nm). On all cases, the sidewall inclination angles are maintained constant and the channel doping level (N_A) is equal to $1´10^{15}$ cm^{-3}.

An out of scale schematic representation of a regular trapezoidal triple-gate SOI MuGFET is presented in figure 2, with its source, drain, gate, buried oxide and substrate regions discriminated. Selective silicon epitaxial raised source/drain regions are commonly used in order to reduce the total series resistance. However, on the present analysis the series resistance associated to such extensions is neglected. Figure 3 presents the simulated fin cross-section shapes as described in table 1.

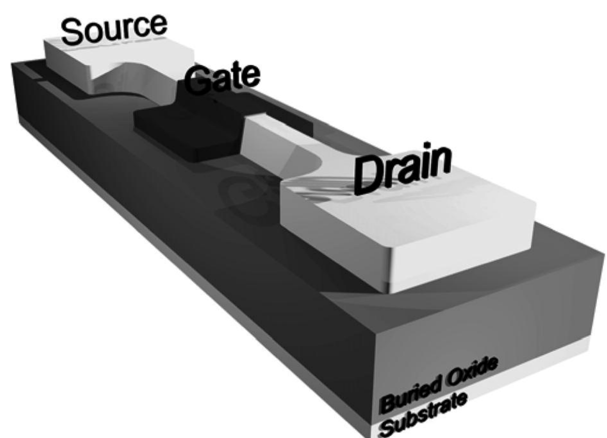

Figure 2. Schematic representation of a regular trapezoidal triple-gate SOI MuGFET.

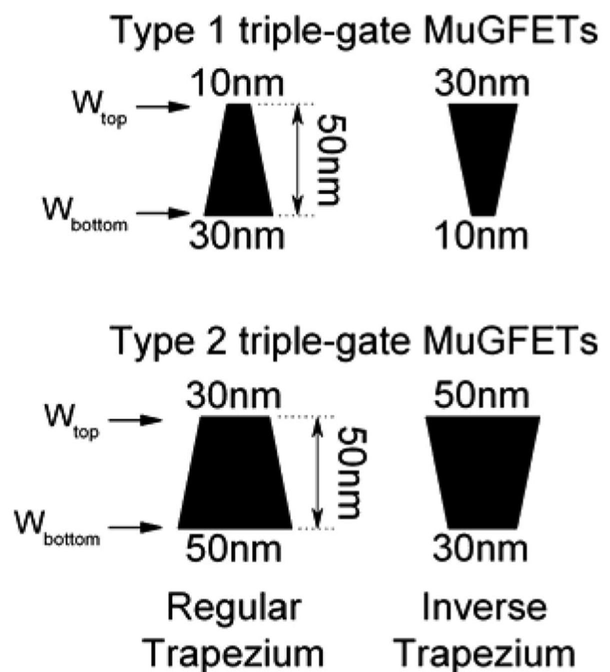

Figure 3. Simulated fin cross-section shapes as described in table 1.

Table I. Important simulated device parameters for triple-gate MuGFETs.

	Type 1 triple-gate MuGFET		Type 2 triple-gate MuGFET	
Parameter [nm]	**Regular Trap.**	**Inverse Trap.**	**Regular Trap.**	**Inverse Trap.**
W_{top}	10	30	30	50
W_{bottom}	30	10	50	30
H_{fin}	50	50	50	50
t_{ox}	2	2	2	2
t_{box}	100	100	100	100
L	30 ~ 1000	30 ~ 1000	30 ~ 1000	30 ~ 1000

The electrical parameters are normalized by a shape factor obtained calculating the total width of the silicon/gate-oxide interface (i.e. unfolding the silicon/gate-oxide interface – W) and dividing this by the channel length (L), as described by equation (1). The Atlas3D device simulator is used, along with Shockley-Read-Hall and Auger recombination models, Fermi-Dirac statistics, parallel and transversal electric field-dependent mobility and Selberherr's impact ionization models [20]. Both linear and saturation's regimes are simulated, adopting drain bias (V_{DS}) of 50 mV and 600 mV respectively, and two gate voltage overdrives of 140 mV and 340 mV ($V_{GT} = V_{GS} - V_{TH}$, being V_{GS} the applied gate voltage and V_{TH} the threshold voltage). The variation of conduction crystallographic plane from top to sidewall on the carrier mobility has not been accounted in simulations. These variations can affect quantitatively the simulation results but not qualitatively as the coupling between the two sidewall gates is not affected by this assumption. Usually, vertical triple-gate n-MuGFET structures are constructed with (110) sidewalls crystallographic orientation and are susceptible to variations if sidewalls inclination angle changes, affecting the effective mobility. However, according to a previous study by B. Goebel *et al* [21], sidewall inclination angles below 15 degrees in the (110) crystallographic orientation have negligible influence on effective mobility, which is the case in this work that have sidewalls inclination angles of ± 11.3 degrees.

$$\frac{W}{L} = \frac{W_{top} + \sqrt{4{H_{Fin}}^2 + \left(W_{Top} - W_{Bottom}\right)^2}}{L} \quad (1)$$

3. METHODS, RESULTS AND DISCUSSION

3.1 Subthreshold Swing and Drain Induced Barrier Lowering

The subthreshold swing (S) and the drain induced barrier lowering (DIBL) [22] are widely used to study devices susceptibility to SCE, as they measure the vulnerability of channel control to the rise of the drain potential. The DIBL parameter is defined as the shift in the threshold voltage divided by the increment in the drain bias. The subthreshold swing was obtained from I_{DS} *vs* V_{GS} curves in the linear region and is presented in figure 4. The drain induced barrier lowering was also obtained from I_{DS} *vs* V_{GS} curve but at two drain biases: V_{DS1} = 50 mV (linear) and V_{DS2} = 600 mV (saturation). The DIBL results are presented in figure 5.

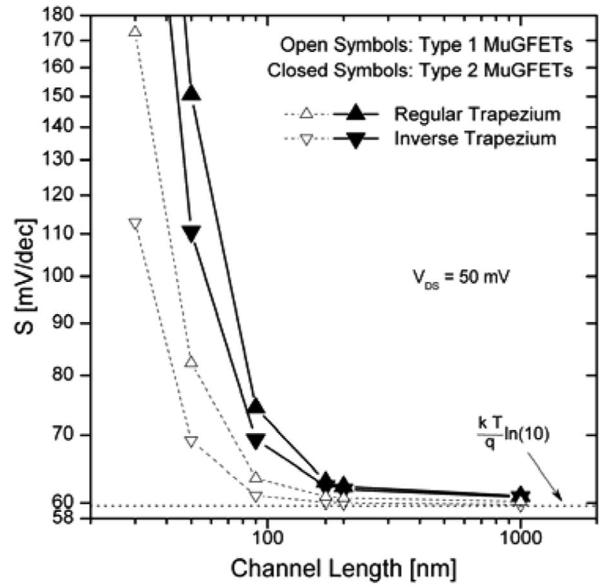

Figure 4. Subthreshold swing as a function of the channel length.

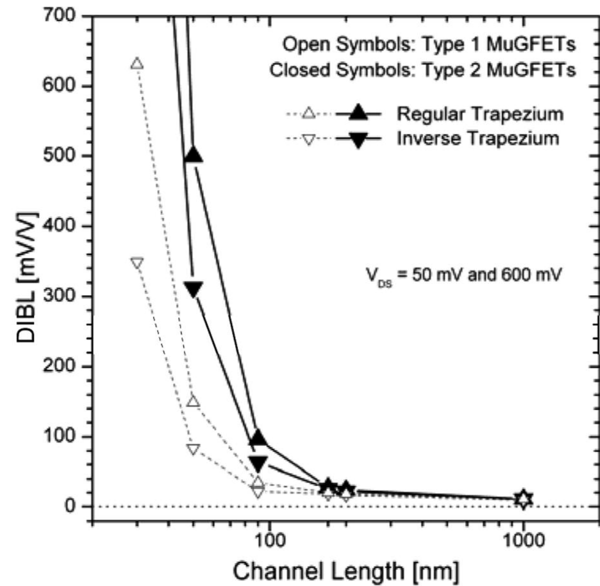

Figure 5. Drain induced barrier lowering (DIBL) as a function of the channel length.

Increasing the fin width at the bottom increases the channel charges dependency to the longitudinal drain electrical field at the same time it reduces their coupling to the gate. On the other side, decreasing the fin width at the bottom reduces its exposition and dependency to the longitudinal electric field at the same time it increases their coupling to the gate. On devices of type 1, the channel geometry starts to influence more the subthreshold swing and DIBL for channel lengths below 90 nm. For devices of type 2, this influence starts way before, at 170

nm. The short channel effects on type 2 devices with less than 90 nm of channel length is heavily worsened by the weak coupling between the gate and the channel, which is dependent of the cross-section geometry (shape and dimension). As the channel length is shrunk, the fin geometry becomes more critical for both parameters. Inverse trapezium fins have enhanced gate coupling to the inversion channels, a behavior partially similar to the presented in Ω-gate devices [1], by taking benefit of reducing the device susceptibility to the drain electric field penetration and reducing the drain-to-channel coupling capacitance. With the further reduction of channel length, values from type 2 devices become too high for certain applications, reaching the point where the empirical scaling rule is broken.

3.2 Threshold Voltage, Transconductance to Drain Current Ratio, I_{ON} and I_{OFF}

The threshold voltage (V_{TH}) presented in figure 6, was obtained making use of the constant current method [23] at the constant drain current of (W/L) x 10^{-7} from the I_{DS} *vs* V_{GS} curves, with a drain bias of V_{DS} = 50 mV. The increase of V_{TH} with the reduction of the silicon fin width is know from literature and an analytical model was proposed by Poiroux *et al* [24]. It departs from the condition that for fully depleted devices the depletion capacitance can become too small compared to the gate oxide capacitance in the way that the carriers in the channel are mainly formed by inversion charges. Based on it, a threshold voltage model for thin multiple gate devices with low doped channel is presented, composed of three terms: work function difference, channel potential and confinement effect contribution. The last term is only significant for fin width below 7 nm. With the reduction of the silicon fin width, the channel potential surpasses the $2{\cdot}\phi_f$ and the concentration of carriers in the channel becomes higher than the one observed for wider fins, leading to the increase of V_{TH}.

The reduction of the channel length causes the threshold voltage roll-off, reducing its value for lengths below the point where the short channel effects start to emerge [1]. The channel middle width region near the bottom of the fin for the regular trapezium is the point with the weakest electrostatic control due to the larger distance of the gate planes which results in the leakiest path of the channel. Better behavior is observed for the inverse trapezium where the weakest electrostatic control is closer to the center of the channel due to the stronger coupling of the gates. The differences in the threshold voltage levels observed between the two MuGFET types and geometries are result of this electrostatic variation with the rise of the potential barrier near the center bottom of the fin as its width is reduced, especially on the inverse trapezium devices. In other words, a better coupling of channel charges to the gate is achieved on thinner inverse trapeziums. As seem before by analyzing DIBL and the subthreshold swing curves, the short channel effects get too strong for type 2 devices, especially on the regular trapezium which may become quite useless for certain applications for channel lengths below 50 nm.

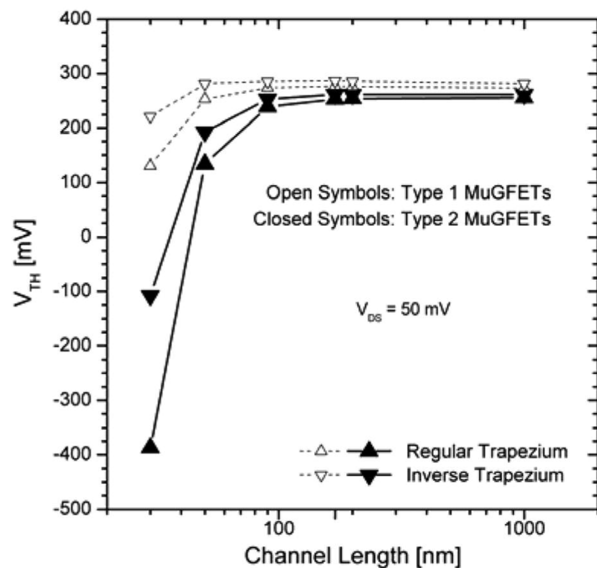

Figure 6. Threshold voltage as a function of the channel length.

The transconductance to drain current ratio (g_m/I_{DS}) is shown in figure 7. When the devices are biased in weak inversion a strong and increasing dependence on the fin geometry and width exists as the channel is shrink. The reduction of the fin bottom width – and the fin width in general also – leads to the better (higher) g_m/I_{DS} ratio, result of the lower subthreshold swing for these devices. Also, this relation with the fin shape and width gets stronger as the channel length is reduced below 170 nm. Moving towards to the strong inverse direction where the mobility starts to

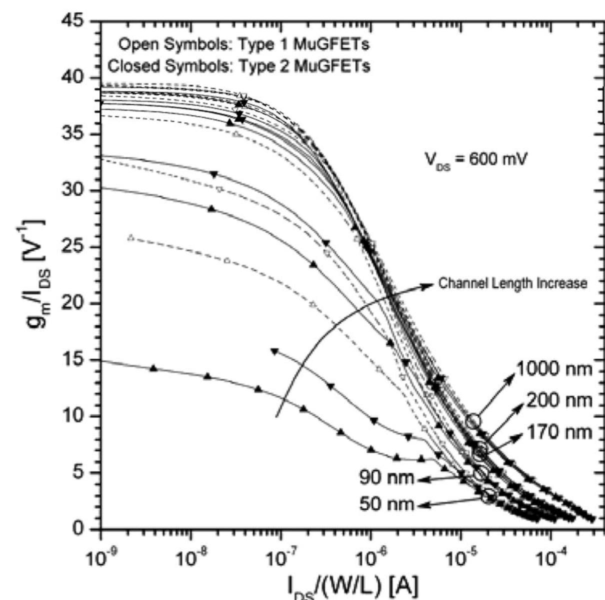

Figure 7. Transconductance to drain current ratio for several channel lengths and fin shapes.

play a dominant role (and also taking with it the SCE), the previous fin geometry trend is overcome and the different devices get grouped by their respective channel lengths. Due to this, an increasing g_m/I_{DS} ratio is obtained in direction to longer channel devices. It is worth to remark from this graph that type 1 and 2 MuGFETs with channel length equal to 50 nm present really poor analog performance, especially at weak inversion.

Figure 8 presents the I_{ON} and I_{OFF} curves for several channel lengths and for the different type of devices. I_{OFF} was obtained from the I_{DS} *vs* V_{GS} curves at V_{GS} = 0 V and I_{ON} at V_{GS} = 1.2 V, both with a drain bias of V_{DS} = 600 mV. The two drain currents I_{ON} and I_{OFF} are normalized by the total width of the silicon/gate-oxide interface (W). The reduction of the channel length emphasized the differences between the two types of devices and fin geometries, with the inverse trapezium type 2 devices presenting the higher drain current level, consequence of the larger cross-section area, lower threshold voltage (especially for short channel length) and smaller series resistance. For type 2 devices, I_{OFF} curves presented an exponential behavior with the channel length reduction until the 200 nm length. Below that the current level suffered a considerable increase and the difference between the fin geometries also increased, with the inverse trapezium presenting the lower values due to the lower gate electrostatic efficiency. In the mean time, I_{OFF} curves for type 1 MuGFETs showed that they are capable of maintaining further their exponential behavior until the 90 nm length, especially the ones with the inverse trapezium geometry. A good balance between I_{ON} and I_{OFF} must be found in the direction of the best case. For both types of devices with channel length between 1 µm and 170 nm this balance is met. For channel lengths of 90 nm, 50 nm and 30 nm, as seem previously, the fin geometry and width become important.

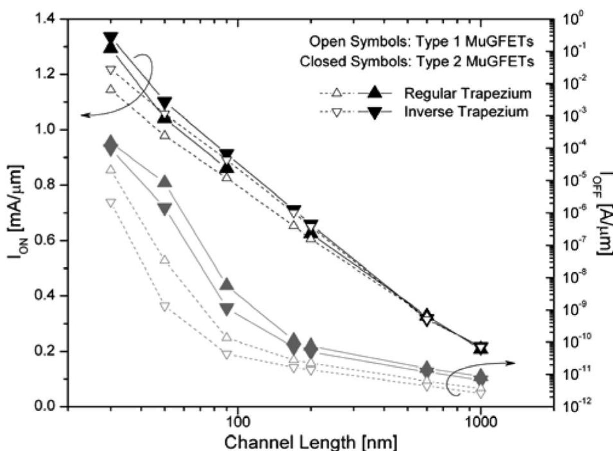

Figure 8. I_{ON} and I_{OFF} currents as a function of the channel length.

3.3 Transconductance

A better understanding of the gate control over channel charges and its relation to the fin geometry and width under different polarization conditions can be achieved through the transconductance (g_m) analysis. Defined as the drain current sensibility to the gate bias variation, the transconductance quantifies the gate control over the active channel charges [25]. The transconductance was obtained from the I_{DS} *vs* V_{GS} curves with a drain bias of V_{DS} = 600 mV at the saturation regime, with two gate voltage overdrives: 140 mV and 340 mV.The transconductance shown in figure 9 is sensible to fin geometry and fin width, as it depends on how strongly the conduction charge is coupled either to the gate or to the substrate. In the inverse trapezium the coupling between the channel charges and the gates (top and sidewalls) is stronger due to the lower angle between the top and lateral gates, leaving a smaller channel fraction uncontrolled by the gate, compared to the regual shape, leading to a better coupling of channel charges to the gate, rather than to the substrate.

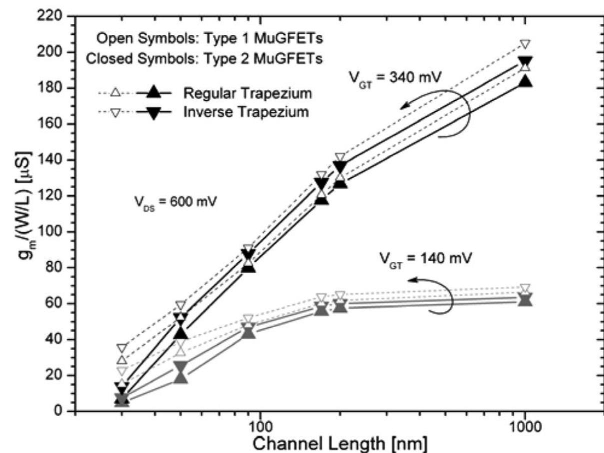

Figure 9. Transconductance as a function of the channel length for the several fin geometries under study.

With the reduction of channel length, the diminishing of the transconductance values for V_{GT} equal to 340 mV occurs at a higher rate than for V_{GT} equal to 140 mV. The g_m sensibility to fin width observed for longer devices is increased with channel length shrink. The curves trend to get more distant from each other below the 90 nm length, reaching the point where the curves from both gate voltage overdrives have closer values. With the increase of the dependence with the fin width, the performance of inverse trapezium type 1 MuGFETs continues to be superior to regular trapezium ones.

3.4 Output Conductance

The penetration of the drain electric field into channel becomes more expressive in four circumstances: the raise of the drain bias, the channel length shrink, the fin width increase and the regular trapezium geometry. The output conductance values (g_d) were acquired from I_{DS} *vs* V_{DS} curves, at drain bias of V_{DS} = 600 mV at the saturation regime, with V_{GS} biased at the gate voltage overdrives of 140 mV and 340 mV.

Following the similar dependence with the fin geometry observed on transconductance, the output conductance sensibility to fin geometry was marginal on channel lengths superior to 200 nm, but still has maintained a higher enhance on performance (i.e. smaller g_d) for type 1 MuGFETs, as can be seen in figure 10.

The reduction of the channel length below 200 nm changes the scenario completely. Both fin geometry and width become of paramount importance with the channel length shrink, as a consequence of the strong increase on the output conductance sensibility to these two factors. Smaller output conductance values observed for thinner fins are justified by the smaller channel susceptibility to drain potential penetration, thanks to the better gate coupling on these devices. So, the thinner the fin is, higher are the electrostatic control and, consequently, the channel immunity against the drain junction bias. For shorter transistors the dependence of the output conductance on channel length becomes stronger than the dependence on longer transistors. This occurs as the drain electric field that penetrates into the channel is proportionally higher on shorten devices when compared to the longer ones.

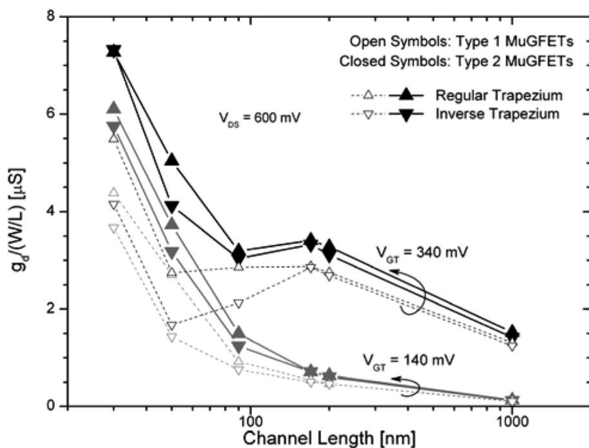

Figure 10. Output conductance as a function of the channel length.

The differences among the various fin geometries and width are highlighted for channel length near 30 nm, forming two distinct groups. One group is composed by type 1 MuGFETs and the other by type 2 MuGFETs. Inside each group, the inverse trapezium devices present the best (lower) values. The gate voltage overdrives showed to be a secondary factor on shorten channel lengths, where the fin geometry importance becomes dominant.

3.5 Intrinsic Voltage Gain

Looking backward to the transconductance and the output conductance results and focusing first on channel lengths superior to 200 nm, both parameters demonstrated a better behavior on thinner inverse trapezium fins. Reducing the channel length below 200 nm showed that both the transconductance and the output conductance parameters have a high sensibility to fin geometry and width. Type 1 devices with inverse trapezium geometry showed better performance over others in both parameters. The gate voltage overdrive influence over the transconductance and the output conductance diminished with the shrink of the channel length, as it got closer to 30 nm. The intrinsic voltage gain (A_V) is obtained by dividing the transconductance by the output conductance. The results for a drain bias V_{DS} = 600 mV and V_{GT} of 140 mV and 340 mV, are presented in figure 11.

Type 1 MuGFETs with inverse trapezium fins have lower output conductance values and higher transconductance values, leading to larger intrinsic voltage gain values when compared to opposite fin geometry. Notice that for devices longer than 200 nm both types of MuGFETs have distinct intrinsic voltage gain values according to the gate voltage overdrive biases. With the reduction of channel length, the gate voltage overdrive influence over the intrinsic voltage gain lowers and the sensibility to fin geometry rises, maintaining the previous trend of inverse trapezium type 1 MuGFETs presenting the best performance and regular trapezium type 2 MuGFETs presenting the worst.

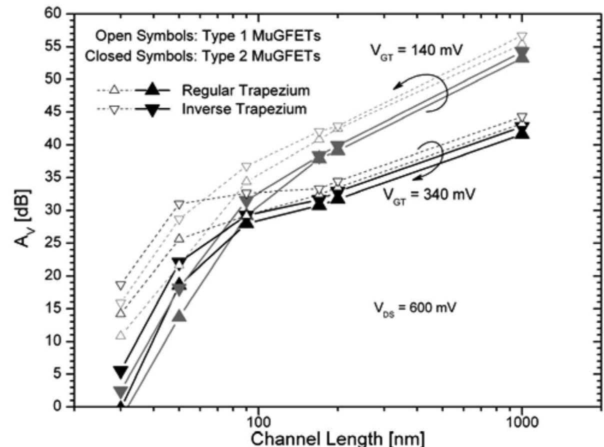

Figure 11. Intrinsic voltage gain as a function of the channel length.

3.6 Unity Gain Frequency

The unit gain frequency (f_T), shown in figure 12, was obtained through equation (2), from the gate-to-source capacitance and the transconductance [26], following the same bias conditions of the intrinsic voltage gain analysis (drain bias of V_{DS} = 600 mV – saturation regime – and V_{GS} biased at gate voltage overdrives of 140 mV and 340 mV), where C_{gs} is the gate-to-source capacitance.

$$f_T = \frac{g_m}{2 \cdot \pi \cdot C_{gs}} \tag{2}$$

The obtained values for the unit gain frequency are pretty close to experimental results published previously, achieving values from 90 GHz to 130 GHz on devices with 30 nm of channel length [26,27]. Walking

from long toward short channel lengths the slope of the unit gain frequency changes for all shapes, but especially for wider devices where it is possible to see some degradation of it below 50 nm. When different gate voltage overdrive values are applied, devices of the same fin geometry and cross-section area trend to merge.

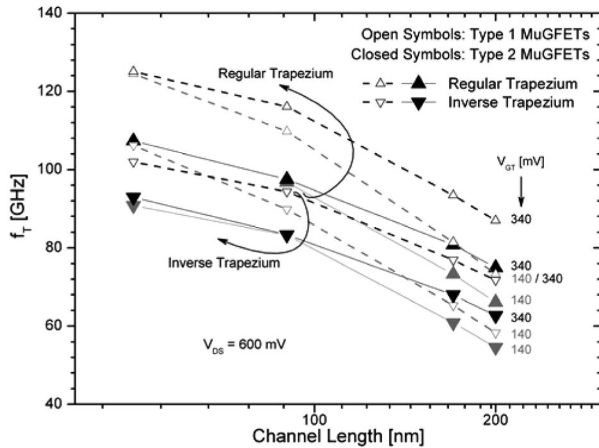

Figure 12. Unity gain frequency as a function of the channel length.

Making use of the total gate capacitance (C_{gg}), calculated as the sum of the gate-to-source, gate-to-drain and gate-to-substrate capacitances according to equation (3) [28], it is possible to state that the observed merge of the unit gain frequency curves occurs as a consequence of the diminishing dependence of total gate capacitance on the gate voltage overdrive, for both sets, as shown in figure 13.

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} \quad (3)$$

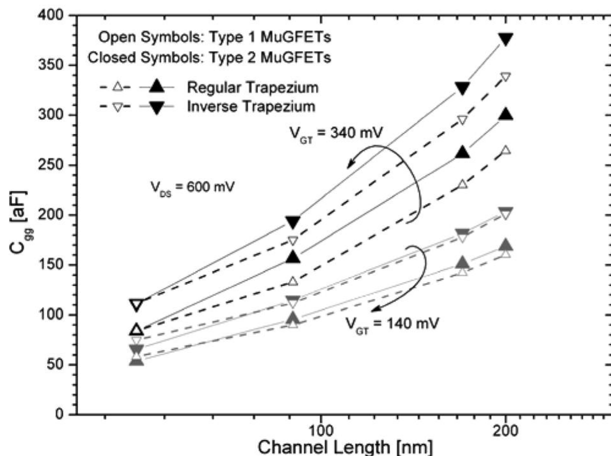

Figure 13. Total gate capacitance as a function of the channel length.

A higher gate-to-source capacitance was obtained for inverse trapezium transistors because the total gate area is higher. This fact has consequences on the unit gain frequency, which got lower values for these devices.

4. CONCLUSIONS

From DC and small-signal AC analysis, the main electric parameters of MuGFETs were related to channel length and fin geometry. Devices with inverse trapezoidal geometries and thin fins have better performance at low frequencies, with higher transconductances and intrinsic voltage gains for all simulated gate lengths and better control of short channel effects. Devices with fin geometry approximated to a regular trapezoidal shape, independently of the channel length, own higher unity gain frequencies because of the smaller gate capacitance. The fin geometry and width can result a positive or negative influence on electrical parameters depending on the channel length. For devices with channel length below 200 nm, the fin geometry and width are critical and consequently the etching definition precision during the fabrication process is of paramount importance.

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