A 65nm CMOS 60 GHz Class F-E Power Amplifier for WPAN applications

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ABSTRACT

This work presents a two-stage 60 GHz Power Amplifier designed in a 65nm CMOS technology dedicated to low cost Wireless Personal Area Network (WPAN) applications. In order to provide a high efficiency operation, the PA is based on a Class E power stage. A Class F driver stage is also designed to provide a square waveform signal to the Class-E power stage. To realize the output networks of both driver and power stage at 60 GHz, distributed elements are used instead of lumped elements. The post-layout simulation results show a saturated output power of 15 dBm with a peak PAE of 26% at 60 GHz. It achieves a gain of 15dB at 60 GHz.

Index Terms: millimeter wave power amplifiers, Class E operation, high efficiency.

I. INTRODUCTION

An unlicensed 7 GHz band around 60GHz is available for uncompressed HD data transfer for indoor WPAN applications, called the V-band. The IEEE 802.15.3C standard occupies this band to support faster and safer link [1]. This application targets a large scale market and a large volume production. One of the important challenges for the implementation of integrated millimeter waves (mmW) communications systems with a low cost technology is the design of efficient and reliable power amplifiers (PAs) on silicon, capable of being competitive against III/V technologies.

The challenge of the mmW CMOS PA design relies on the ability of delivering a maximum of output power (P_{out}) with a maximum PAE. Due to their high efficiency (theoretically up to 100%), Class-E PAs [2] have been explored extensively at radiofrequencies in different semiconductor technologies [3][4][5]. In the same way, the design of Class E PA for mmW applications could lead to reduce the power consumption of the whole transmitters.

The latest results on mmW CMOS power amplifiers (PA) in silicon have shown a peak PAE of 15% at 60GHz [6], with a 2-stage linear power amplifier. To achieve a higher level of PAE at the same frequencies, we had to look at the SiGe Class E performances. Hence, the highest performances in SiGe technology is achieved by a 1-stage Class E power amplifier with a peak PAE of 20,9% [7]. In this paper, the design of a the first Class E Power Amplifier with a Class F driver stage is described in the V-band in a low cost CMOS 65nm technology from STMicroelectronics.

Table I. 65nm CMOS 60 GHz linear PAs State-of-art

Reference	Stages	Supply (V)	Gain (dB)	Psat (dBm)	PAE (%)
[6]	2	1.2	14	12	15
[10]	1	1.2	4.5	9	8.5
[11]	3	1	15.4	11.5	11
[12]	4	1.2	13.7	14.2	8.4
[13]	8 parallels	1.2	14.3	16.6	3.6
	combined	1.8	15.5	18.1	4.9

II. MILLIMETER-WAVE CLASS E POWER STAGE DESIGN

A. Millimeter-wave PA State of the art

The Table I is a resume of performances for linear classes of 60 GHz power amplifier in 65nm CMOS technology in terms of gain, Psat, PAE and supply voltage [6][10][11][12][13]. Most of the PAs reported in the literature are class-A PAs in order to reach high power gain values. Nevertheless, the PAE remains very low, from 3.6% to 15%. With these PAs, high output power can be reached, until 14.2dBm with a four-stages PA [12] to 18.1dBm with a combined architecture [13]. As we target higher efficiencies, we choose to

work on a Class-E PA which is a non-linear class of operation. As no Class-E PA has been reported in the literature at 60GHz, the feasibility of such a class operation has to be demonstrated.

B. Class E PA design

The classical Class-E implementation, depicted in Figure 1, is based on an active MOS transistor device. This transistor acts as a switch. When the switch is ON, the current flows through the device (zero voltage across the switch) and when the switch is OFF, the current flows in and out from the output capacitor (C_{shunt}), thus charging and discharging the capacitor and generates voltage waveform. Hence, the result is a non overlapping voltage and current waveforms.

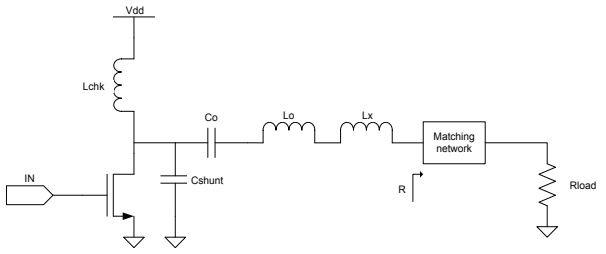

Figure 1. Typical Class E schematic

Table II. Theoretical components formulas [8]

Lo	Lx	Lchk
$L_0 = \frac{1}{\omega_0^2 C_0}$	$L_x = \frac{\pi V_{dd}^2 (\pi^2 - 4)}{2\omega_0 P_{out}(\pi^2 + 4)}$	large
Co	**Cshunt**	**R**
$C_0 = \frac{1}{\omega_0 R Q_L}$	$C_{shunt} = \frac{P_{out}}{\pi \omega_0 V_{dd}^2}$	$R = \frac{8 V_{dd}^2}{P_{out}(\pi^2 + 4)}$

Table III. Theoretical components values

L_O	C_O	C_{shunt}	L_x	L_{chk}	R
1nH	6,5fF	12fF	125pH	large	41Ω

Moreover, the output network is designed to transform the 50-Ω output impedance to a low driving impedance for the class-E structure while providing 2nd harmonic suppression. This output network is composed by inductors and capacitors. Theoretical expressions used to calculate the value of each lumped elements are summarized in Table II.

To determine the passives components values, we had first to define important parameters: output power, frequency and supply voltage. For the 60 GHz WPAN application targeted, the output power specification is a maximum output power equals to 15dBm with a 1.5V supply voltage. Table III summarized the value of each elements regarding to these specifications.

According to the Table III, a 1nH inductance is required to realize L_o inductor. Nevertheless, this inductance resonates before 60 GHz, so we cannot use this inductance value in the output network. As an example, we simulated a 160pH inductance of the 65nm CMOS Design Kit according to the frequency. The simulation results are shown in Fig. 2. Between 1 and 10 GHz, the inductance value is 160pH, as expected. But when the frequency increases, the inductance value increases too. At 60GHz, the inductance value is equal to 250pH.

Therefore, to realize the inductance of the output network, we decide to use, instead of lumped elements, distributed elements with μ-strip (MS) transmission lines (TL). Therefore, to realize the inductance of the output network, we decide to use, instead of lumped elements, distributed elements with μ-strip (MS) transmission lines (TL).

The active device is a low Vt and low power device from STMicroelectronics. To achieve high frequency operation, and gain, we choose to work on a cascode topology instead of a common source topology. The biasing voltage of the common gate device is chosen equal to the supply voltage, as it has to be higher as possible to assure the commutation of this device. To guarantee a high current gain, we use size-optimized transistors of 140 fingers of 1.2μm/finger. Figure 3 presents the schematic of the Class E power stage.

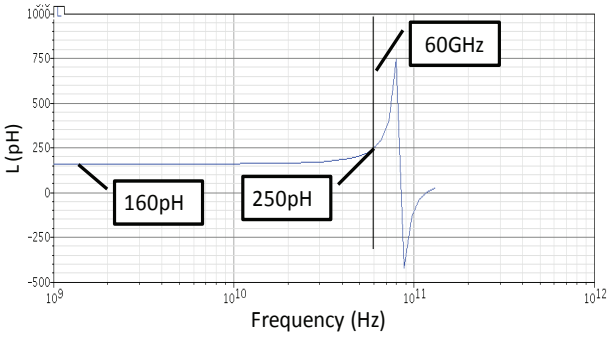

Figure 2. 160pH inductance value simulation

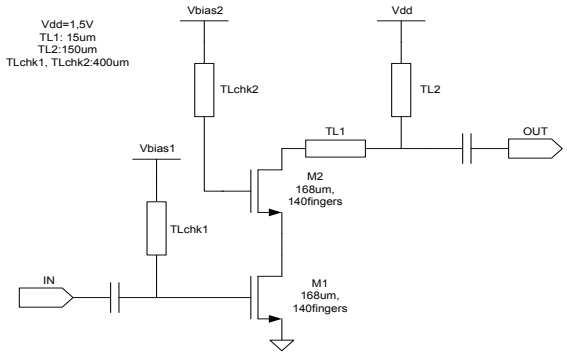

Figure 3. Implementation of Class E Power Stage

C. Class E post layout simulation results

Simulations were performed thanks to ADS framework 2009 update 1 and the 65nm CMOS STMicroelectronics Design Kit. Physics-based BSIM4 model from the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley, is used to accurately reflect the transistor's behavior. In order to ensure the switching mode operation, the input signal is a square-wave signal. The output has been adapted to 50 Ohms. The simulations performed were Transient and Harmonic Balance simulation.

Figure 4 presents the results of the transient simulation with the drain waveforms of the power stage when a square-wave signal is applied on the gate of the transistor. This input signal will be provided by the driver stage. We can note that the Class E acts as a switch with a drain voltage and a drain current in phase opposition.

Large signal parameters are given in Figure 5 where the power gain and output power are depicted according to input power. The Class E power stage presents a saturated output power of 15 dBm and a maximum gain of 8dB. Nevertheless, we can note that, for an output power equals to the saturated output power of 15dBm, the power gain is negative, so a back-off is mandatory. To achieve an output power of 12dBm for a 3dB compression gain, that stage requires an input signal around 7 dBm. Figure 6 presents the Drain Efficiency (DE) of the Class E power stage. Thanks to the switching operation, the drain efficiency reaches 39.6% at the 7dBm-input power. It corresponds to a 31% of power added efficiency (PAE) which is a promising result compared to others 60GHz PA reported in [6]-[10], where the maximum PAE achieved is 15%.

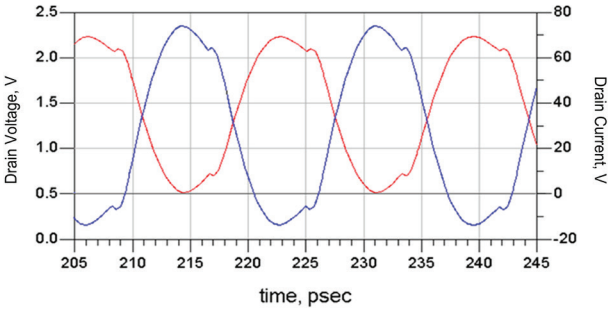

Figure 4. Drain Voltage and Current Class E waveforms

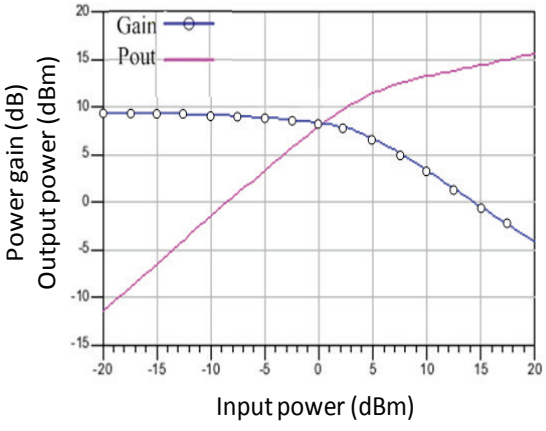

Figure 5. Class E power stage large signal simulations

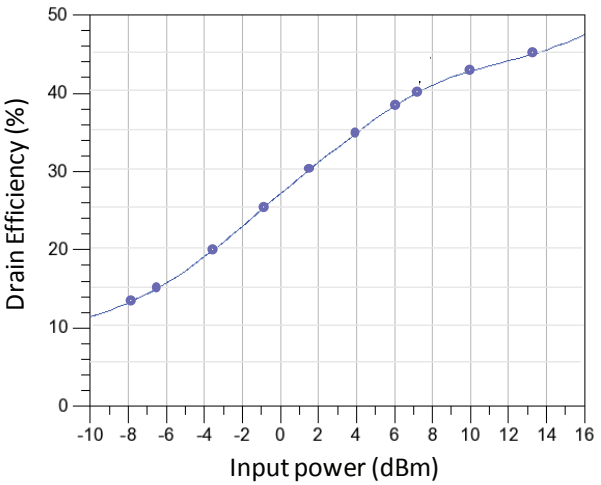

Figure 6. Class E Drain Efficiency

III. MILLIMETER-WAVE CLASS F DRIVER STAGE DESIGN

A. Driver stage Class of operation

To operate the cascode Class-E power stage as a switch optimally, we need to drive the common source transistor into saturation with a square-wave signal. At RF frequencies, in literature we have several options: class-B, C or F [14][15]. In order to realize this waveform at 60GHz, we can study three classes of operation: B, C and F. Classes B and C amplifiers are classified in the sinusoidal class category. Theoretical output

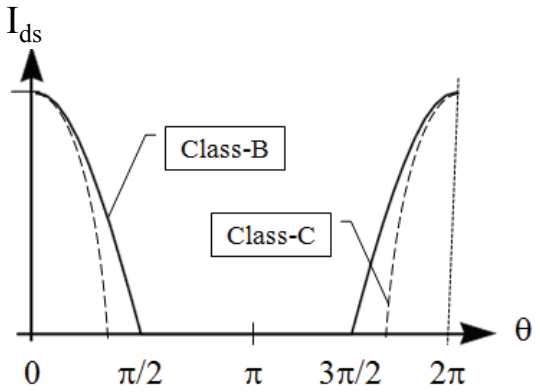

Figure 7. Typical Classes B and C output waveforms

waveforms are illustrated in Fig. 7. The output voltage is a half sinusoid with a conduction angle equals to π for Class-B and less than π for Class-C.

At mmW frequencies, these signals can be used to drive the class-E power stage. Class F amplifiers are in the high-efficiency category with a square waveform output voltage. Theoretical output waveform is illustrated in Fig. 8. The square waveform is provided by adding the odd harmonic amplitudes. In Fig.8, the output signal is realized with the first and third harmonic. Moreover providing the good waveform signal, the driver stage must also take care of the efficiency and deliver to the power stage the 7dBm mandatory to satisfy the output power specifications. So we have to evaluate the power gain that the driver stage can reach.

Hence, we realized simulations of the driver stage according to the biasing point for the three configurations (Fig.9 and 10). For Class-B configuration, the biasing point is equal to the threshold voltage V_{th} and in the Class-C configuration, the biasing point is under V_{th}. Fig. 9 shown power gains reach with these configurations. At 60GHz, the power gain is equal to 2dB and -1dB resp. for Class-B and Class-C biasing point. These values are very low and we can compare them to the power gain in the class-F configuration. In Fig.10, we can see that the power gain is improved at

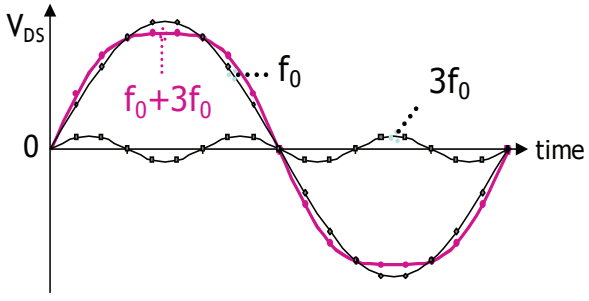

Figure 8. Typical Class-F output waveform

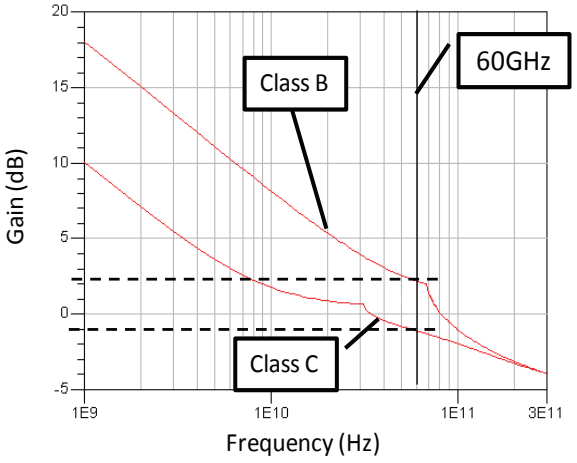

Figure 9. Power gain vs frequency for Class-B and C configuration

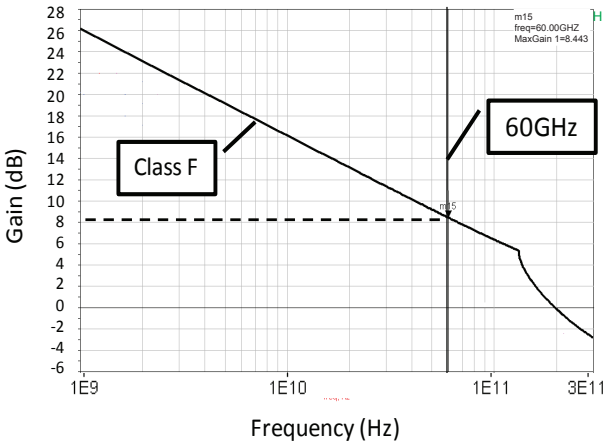

Figure 10. Power gain vs frequency for Class-F configuration

60 GHz, with a value equals to 8dB. Indeed, the class-F biasing point is the same than deep class-AB. So, from the output waveforms and the power gain point of view, we choose to work on the class-F configuration despite of the complexity of the structure (compared to the sinusoidal classes B and C).

B. Class F driver stage design

The main characteristic of Class F amplifier is its output filtering network. In classical sinusoidal classes, the output network is used to realize the matching network. In class-F configuration, the output network is used to provide characteristic impedance at the harmonic frequencies. At the input of the output network, the impedance at the first harmonic is equal to the load resistance R, at the odd harmonic to ∞ and the even harmonic to zero. The network could have more or less orders, according to the number of harmonics took into account. Figure 11 presents typical topology of the Class F power amplifier.

In order to determine the numbers of harmonics we have to deal with, we studied a previous work [6]. Authors shown that, at 60GHz, no more improvement in efficiency can be reached for orders over than three. Note that four times the fundamental frequency is equal to 240GHz, and at this frequency, the gain of transistor is negligible. For that matter, the third har-

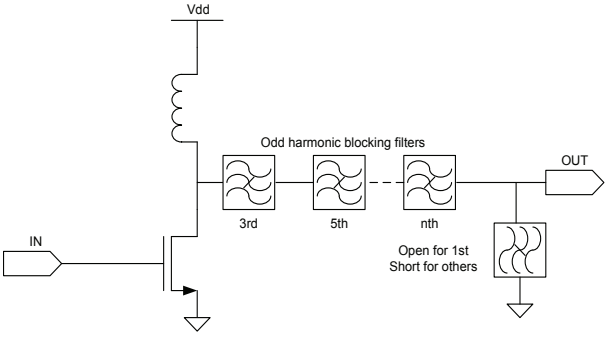

Figure 11. Typical Class F power amplifier

monic will be the last taken into account in the output network of this driver stage. The filters are designed with distributed elements such as transmission lines and quarter-wave lines. The TL2 line is a quarter-wave line at 60GHz, and the TL3 line is a quarter-wave line at the third harmonics 180GHz. The Class-F topology implemented in the 65nm CMOS technology is depicted in Figure 12. The S_{11} parameter shows in Fig.13 for frequencies from 1GHz to 300 GHz confirm the impedance is equal to zero for 120 GHz ($2f_0$) and to ∞ for 180GHz ($3f_0$).

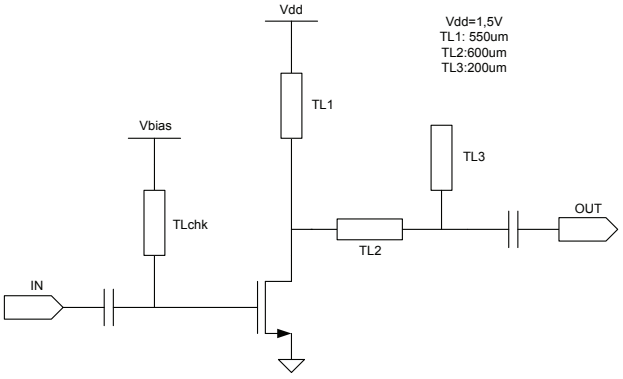

Figure 12. Implementation of Class F driver stage

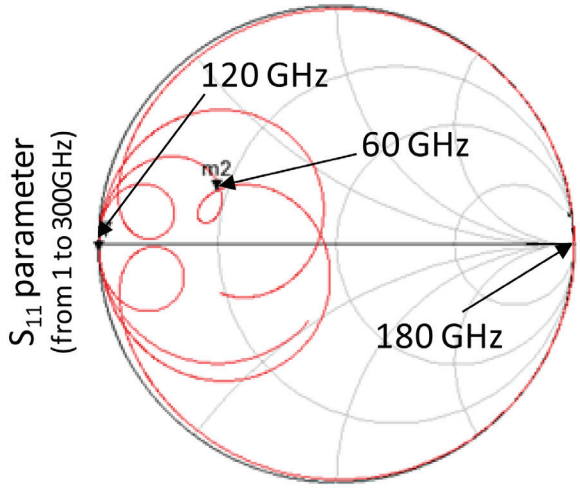

Figure 13. S_{11} parameter of the output Class F network

C. Class F driver stage post layout simulation results

Figure 14 presents the large signal simulations of the driver stage. The input signal is a sinusoidal waveform. The maximum saturated output power is 15dBm and the small-signal power gain is 8dB. In order to take care of linearity, we take an important back-off in the driver stage, to be sure that the driver stage will not saturate before the power stage. Moreover, in the previous section, we noted that to achieve an output power of 12 dBm, an input signal of 7 dBm was required. This output power is achieved with an input

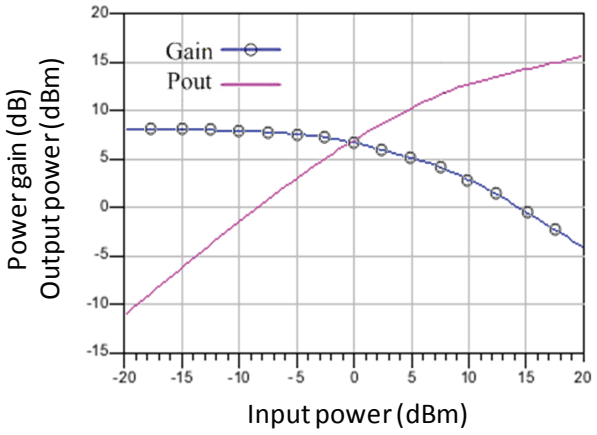

Figure 14. Class F driver large signal simulations

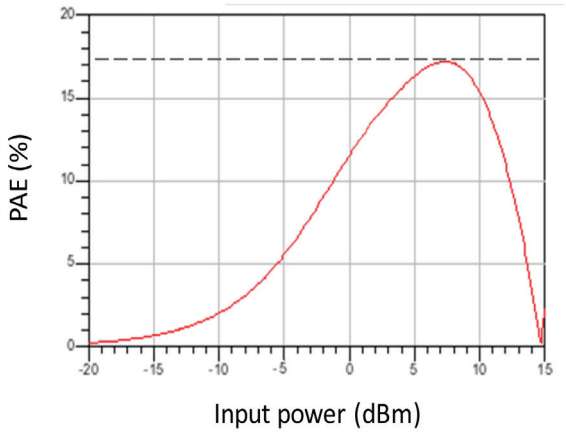

Figure 15. Class F PAE

signal equals 0 dBm. PAE according to input power is depicted in Figure 15. At 60 GHz, the maximum PAE of the Class F driver stage is 17%. For an input power of 0dBm, the PAE reaches 12%.

IV. TWO-STAGE PA POST LAYOUT SIMULATION RESULTS

A. Full Power Amplifier Simulation Results

After the study of each stage independently, we realized the final PA with the class F driver stage and the Class E power stage. The die of the two-stage PA is shown in Figure 16. The size is 1240μm*960μm and the total area is 1.19mm², including pads for input, output, supplies and ground. Figure 17 presents the large signal simulation of the two-stage PA. The saturated output power achieves 15dBm and the maximum gain is 15 dB. Regarding to our specifications, a 12 dBm output power can be reached with a 0.5dBm input power. These values are in good agreement with the stages studied previously. Then, the efficiency, both drain efficiency and power added efficiency, of the two-stage amplifier

is depicted in Figure 18. The maximum PAE and drain efficiency reaches 26% and 34% respectively.

The overall PAE is lower than the Class E PAE alone (31%), due to the PAE of the class F driver stage which is lower (17%). Nevertheless, the driver is required to shape the signal applied to the Class E input. We can compare these results to the recent state of the art in the Table IV. We can note the improvement of PAE between the linear PA and the Class E PA in this table. In the linear PA, the PAE maximum is equal to 15% whereas we achieved 26%. Furthermore, a power gain of 15dB allows us reaching a high Figure Of Merit (FOM).

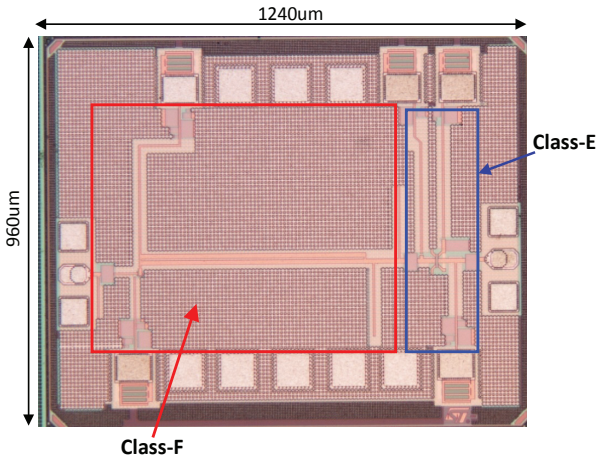

Figure 16. Class FE PA photograph

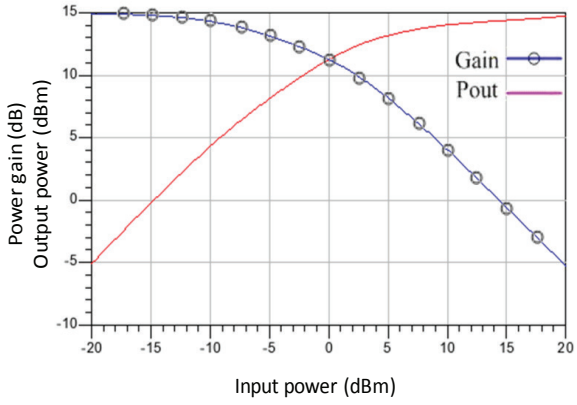

Figure 17. Power Amplifier large signal simulation

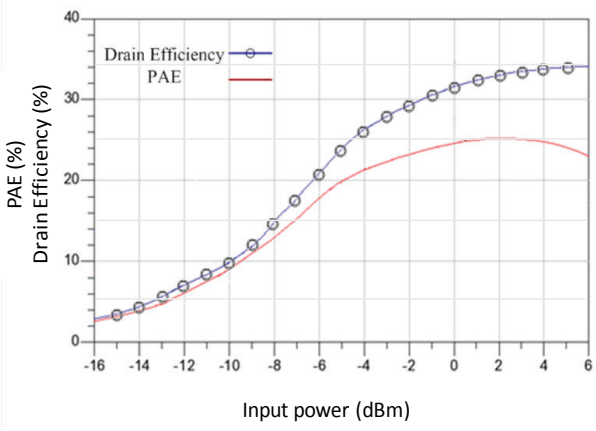

Figure 18. Drain Efficiency and PAE of the power amplifier

Table IV. 60 GHz CMOS 65nm Linear PA versus Class E PA

	Ref.	Techno	Stage	Supply	Gain (dB)	Psat (dBm)	PAE (%)	Pdc (mW)	FOM (W*GHz^2 *10^4)
Linear Class A/AB	[10]	65nm CMOS	1	1.2V	4.5	9	8.5	27.6	7
	[11]		3	1V	15.4	11.5	11	43.5	193
	[12]		4	1.2V	13.7	14.2	8.4	300	174
	[6]		2	1.2V	14	12	15	65	237
	[13]		8	1.2V	14.3	16.6	3.6	732	159
	[13]		8	1.8V	15.5	18.1	4.9	1504	404
Class E	[7]	SiGe 130nm	1	1.2V	4.2	11.5	20.9	27	28
	This work	65nm CMOS	2	1.5V	15	15	26	75	936

The FoM definition, defined by ITRS 2006, is given in (1). The unit is W*GHz^2 *10^4.

$$FoM_{PA} = P_{out} \cdot G \cdot PAE \cdot f^2 \quad (1)$$

Nevertheless, we have to remind that our results are not measurements results but post layout simulation results, that is to say that we took into account all the parasitic (resistors and capacitors) due to the lines, the interconnections, vias, pads, and so on.

These good results can be compared to the SiGe Class E reported previously in the literature. The PAE is the Class-E PA in SiGe technology is equal to 20.9%, this value is still lower than our CMOS PA.

V. CONCLUSION

In this work, we have demonstrated the feasibility of a CMOS 65nm two-stage high efficiency power amplifier. For that matter, a Class E power amplifier has been studied and designed. To realize the output network at 60GHz, distributed elements are used instead of classical lumped elements used in class-E operation. In order to drive the Class E, several driver stage have been studied. We compared different classes of operation B, C and F. Regarding to the power gain, the class F has been selected and developed. To the best of our knowledge, this work is the first one on designing a Class FE in CMOS technology for mmW applications. Post Layout Simulations were performed at 60 GHz.

The PA exhibits a power gain of 15dB and a maximum saturated output power of 15 dBm. The peak PAE is 26% and the drain efficiency achieves 34%.

This study shows promising results for Class F-E power amplifier at 60 GHz, compared to recent mmW power amplifiers reported in literature.

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