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Design Of An Improved And Robust Asynchronous Wrapper (Aw) For FPGA Applications D. L. Oliveira, L. A. Faria and E. Lussari









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FOREWORD

In this issue of JICS some of the papers on this issue have been selected from the presented at SBCCI2012 (25th Symposium on Integrated Circuits and Systems Design), which has been held in Brasília, Brazil, in 2012. Also selected contributions from SPL2012 (VIII Southern Programmable Logic Conference) have been included. Among the contributions presented at these conferences, only a few best rated were selected by the JICS Editorial Board and have been invited to submit an extended version to the Journal. These extended papers have passed through the usual reviewing process before acceptance. In addition to the best papers presented at the mentioned conferences, spontaneous submissions passed through the usual reviewing process and have been accepted as regular papers.

We would like to thank the authors for their effort in preparing these high quality papers, as well as the reviewers for their valuable contribution on paper evaluation and selection, which guarantees the scientific level of this issue. We sincerely hope that JICS readers will enjoy these contributions.

We also would like to thank the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq) for the financial support for this JICS Issue.

Marcelo Antonio Pavanello

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