Detection of Transient Faults in Nanometer Technologies by using Modular Built-In Current Sensors

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ABSTRACT

Soft error resilience is an increasingly important requirement of integrated circuits realized in CMOS nanometer technologies. Among the several approaches, Bulk Built-in Current Sensors (BBICS) offer a promising solution as they are able to detect particle strikes immediately after its occurrence. Based on this idea we demonstrate a novel modular BBICS (mBBICS) that tackles the main problems of these integrated sensors – area, leakage, and robustness. Simulations based on a predictive nanometer technology indicate competitive response times for high performance applications at the cost of 25 % area overhead and very low power penalty. Thereby, all simulated particle strikes that lead to transient faults could be detected. Additionally, reliability analysis proved the robustness of the proposed mBBICS against wide variations of temperature and process parameters.

Index Terms: Built-in current sensors, concurrent detection, fault tolerance, reliability, security, soft errors, transient faults.

I. INTRODUCTION

CMOS is furthermore the most widespread technology for integrated designs as no feasible alternative is in sight to date and in the near future. Driving forces of this leadership are the high miniaturization capability and the reliability of CMOS. Against the background of nanotechnology though, reliability concerns are arising with an alarming pace. The shrinking of technology sizes result in circuits that are more susceptible to several permanent or transient error sources like oxide breakdown [1], parameter variations [2] or radiation [3]. In case of the latter, energetic particle can inject electrical charge into sensitive regions of the semiconductor devices and, thus, lead to soft errors. Until the early 2000's, researches on this kind of errors focused mostly on memories and application oriented on avionics and aerospace environment. In current nanometer technologies though, soft error resilience is also required for the combinational parts of the circuits and for ground level applications. The latter is driven by the decreasing critical charge required to generate soft errors in integrated circuits.

In recent years, several concurrent error detection and/or correction techniques have been proposed to mitigate the effects of soft errors. This includes the use of debug resources from the scan path [4], the combination of error detecting codes with carry-save arithmetic [5], and selective redundancy [6]. In contrast to the before mentioned approaches which focus on gate and system level, Bulk Built-In Current Sensors (BBICS) offer a promising solution on transistor level to detect particle strikes immediately after its occurrence [7]. The advantages of this technique are zero delay penalty and fast error detection. On the downside, existing BBICS are prone to temperature and parameter variations and/or require a considerable amount of area [8]. Further, several known BBICS implementations increase the leakage power dissipation of the monitored circuits.

The aim of this work is to present a new modular BBICS (mBBICS) which operates reliably under wide temperature and process variations, has reasonable area requirements, and has low impact on power dissipation.

The rest of the paper is organized as follows: section 2 gives basic information about the content of this work. Section 3 describes the concept of the proposed sensor while section 4 is related to simulation results and discusses the findings. Finally, section 5 draws the conclusion.

II. PRELIMINARIES

This section presents preliminary information regarding soft errors, Bulk Built-In Current Sensors (BBICS) and leakage currents in nanometer technologies.

A. Transient Faults in Integrated Circuits

Transient voltage variations during the lifetime of combinational or sequential circuits are defined as transient faults. The first harmful effects of transient faults are soft errors by inverting stored results of system operations (i.e. bit-flips).

Due to the transistor shrinking and the growing communication of confidential data, soft errors can happen today even at ground level by means of perturbation events arisen from environmental or intentional sources. Examples of environment events are alpha particles released by radioactive impurities and more importantly neutrons from cosmic rays [7]. On the other hand, intentional perturbation events are usually produced by optical sources such as flashlights or laser beams [8] that can maliciously induce transient effects on secure circuits like smartcards to retrieve their secret information.

Soft errors and transient faults are also known respectively as single event upsets (SEU) and single event transients (SET) in fault-tolerance-related fields or even as consequences of attacks based on fault injection in security applications.

For electrical simulation purpose, a transient fault in CMOS circuits is modeled by injecting a double exponential current pulse I_{fault} at the sensitive node. Thereby, the shape of the pulse is approximated by the following equation [9]:

$$I_{fault} = \frac{Q_f}{t_f - t_r}\left(e^{\frac{-t}{t_f}} - e^{\frac{-t}{t_r}}\right) \quad (1)$$

in which Q_f is the charge collected due to the particle strike, t_f means the decay time of the current pulse, and t_r labels the time constant for initially establishing the ion track.

B. BICS Detecting Transient Faults

Built-in current sensors (BICS) were initially proposed as a mechanism for detecting large increases in the current IDDQ consumed by a CMOS circuit during its quiescent state, i.e. when the circuit is not switching. The mechanism allows thus testing CMOS circuits against permanent faults [10][11]. Further, BICS were also adapted for detecting transient faults in memory cells (i.e. bit-flips) [12][13][14]. Recently, efforts were made for monitoring transient faults in combinational logic as well [15]. All these techniques connect BICS to the power lines (VDD and GND) of the monitored circuit in order to distinguish anomalous transient currents from normal currents. The today's problem is that the amplitude of transient currents induced by radiation effects or fault attacks can have the same order of currents normally generated by switching activities in combinational logic circuits. Hence, schemes monitoring power lines are very limited for detecting just small range of transient faults.

On the other hand, a wide range of transient faults is detectable whether BICS are connected to the bulks of the monitored circuit's transistors; such a smart idea was introduced for the first time in [7] [8]. Fig. 1 (a) and (b) illustrate Bulk BICS (BBICS) identifying anomalous transient currents I_{fault} that flow through the junction between a bulk and a reversely biased drain of a disturbed transistor (MOSFETs "off" in Fig. 2). BBICS indeed take advantage of two facts: (1) In fault-free scenarios (i.e. $I_{fault} = 0$) the bulk-to-drain (or drain-to-bulk) current I_B is negligible even if the MOSFET is switching in function of new input stimuli; (2) During transient-fault scenarios, I_{fault} is much higher than the leakage current flowing through the junction. The range of detectable transient faults is easily adjustable by calibrating the size of the transistors that constitute the BBICS. Thus, circuits can be designed that are able to latch a flag if abnormal currents in a predefined range are detected via the BBICS.

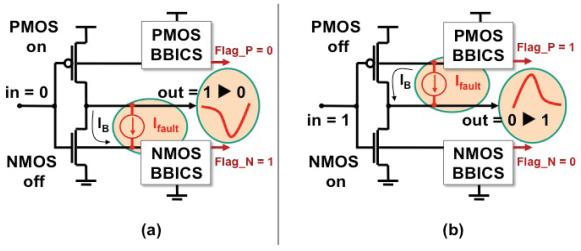

Figure 1. The two classic cases of transient faults in a CMOS inverter perturbed by an anomalous current Ifault.

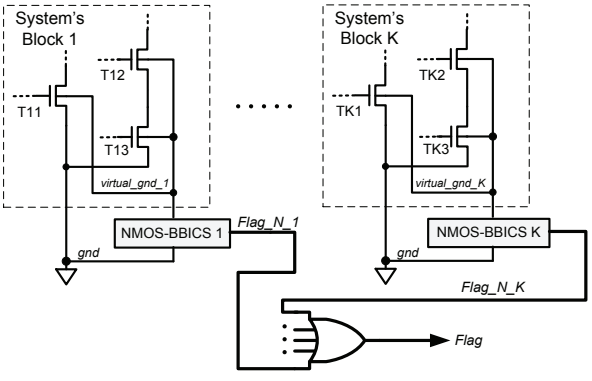

Figure 2. The BBICS-based strategy (only NMOS) monitoring blocks of a system.

Note in Fig. 1 that the connections between monitored circuit (e.g. inverter) and PMOS and NMOS BBICS blocks are done by using metal – from the body-ties of each monitored transistor (i.e. transistor bulks of the inverter) up to the inputs of the BBICS circuitries. Thereby, peaks of anomalous transient currents (i.e. transient faults) are almost not attenuated [18], ensuring thus enough signals for BBICS performing an efficient detection. The only small attenuation is a function of the local distance between the struck zone of the monitored transistor and its body-tie.

Fig. 2 summarizes the strategy for protecting system's blocks against transient faults in pull-down network by using BBICS. Equivalent strategy must be taken for detecting transient faults in pull-up network as well. Note that in such a strategy the connection between the monitored circuit (e.g. system's block 1) and the BBICS's circuitry (e.g. NMOS-BBICS 1) is done via metal – from the body-ties of each monitored transistor (e.g. T11, T12, and T13) up to the input of the BBICS's circuitry. Thereby, the peak of the anomalous transient current (i.e. the transient fault) is almost not attenuated, ensuring thus an efficient detection. In fact, this very small attenuation is a function of the local distance between the struck zone of the monitored transistor and its body-tie.

It should be noted that a BBICS detects all single event transients, including soft errors that are masked by the logic and do not lead to a transition fault [7]. These false detections are unfavorable though, its impact on the design performance is bearable as it results only in a small amount of additional clock cycles.

C. Leakage

Ideally, CMOS cells draw no current or rather dissipate no power when idle. Unfortunately, this is not true for real cells realized in nanometer technologies. A major impact originates from sub-threshold leakage current I_{sub} which is the current between source and drain when the transistor is in theory cut off. A commonly used approximation of I_{sub} is [16]:

$$I_{sub} = a_1 \frac{W}{L} e^{\left(\frac{q}{nk_BT}\left[V_{gs} - v_{th}\right]\right)} \quad (2)$$

in which a_1 is a technology factor, W means the transistor gate width, L labels the transistor gate length, q corresponds to the charge of an electron, n means the sub-threshold swing coefficient, k_B is Boltzmann's constant, T labels the operating temperature, V_{gs} is the gate-source voltage, and v_{th} labels the threshold voltage. The latter can be modeled with [16]:

$$v_{th} = v_{th0} + \gamma a_2 V_{sb} - \eta a_3 V_{ds} \quad (3)$$

in which v_{th0} is the zero-bias threshold voltage, γ is the body-bias coefficient, a_2 and a_3 label technology constants, η corresponds to the Drain Induced Barrier Lowering (DIBL) coefficient, V_{sb} labels the source-bulk voltage, and V_{ds} is the drain-source voltage.

III. MODULAR BBICS

In this section, the underlying assumptions as well as the proposed sensor structure is presented.

A. Origination of the approach

Existing BBICS are capable of detecting smallest bulk currents with low response times. Moreover, the approach is much more efficient for dealing with transient faults of long duration and multiple faults without impact on the system's operating frequency. However, common problems are high area effort as well as strong susceptibility to parameter and temperature variations. Further, most available BBICS create an offset on the bulk voltage and, thus, decreases V_{sb} [8][17]. Following from eq. 3, this results in lower threshold voltage and, consequently, in considerably higher sub-threshold leakage (see eq. 2).

Based on these observations, we investigated on solutions for reducing the sensor area, increasing the sensor robustness, and avoiding any voltage offset on the bulk at normal operation (i.e. in fault-free scenarios). Thereby, we identified sharing of functionality between different BBICS as possible solution to reduce the required area overhead. Further, we decided to connect the bulk via a high ohmic transistor in on-state with VDD or GND, respectively, as proposed in [18]. Last but not least, we searched for a positive feedback structure to increase stability and decrease the sensor response time.

Next, the basic structure and the mode of operation of the proposed modular BBICS, in the following named as mBBICS, is presented. The considerations are related to the sensor for the NMOS bulk. The PMOS version, whose behavior is complementary, is omitted for the sake of simplicity.

B. Basic Structure

Fig. 3 depicts the basic structure of the proposed mBBICS which can be divided in two kinds of components: head and tail. Thereby, several heads which are connected to separate bulks share one tail.

A **head** connects via transistor Nh1 the bulk of the Block Under Test (BUT) with GND. The transistor which has a small W/L ratio is on-state. The bulk is also connected with the gate input of transistor Nh2 whose drain connects to the common signal $head_{NMOS}$ of several heads.

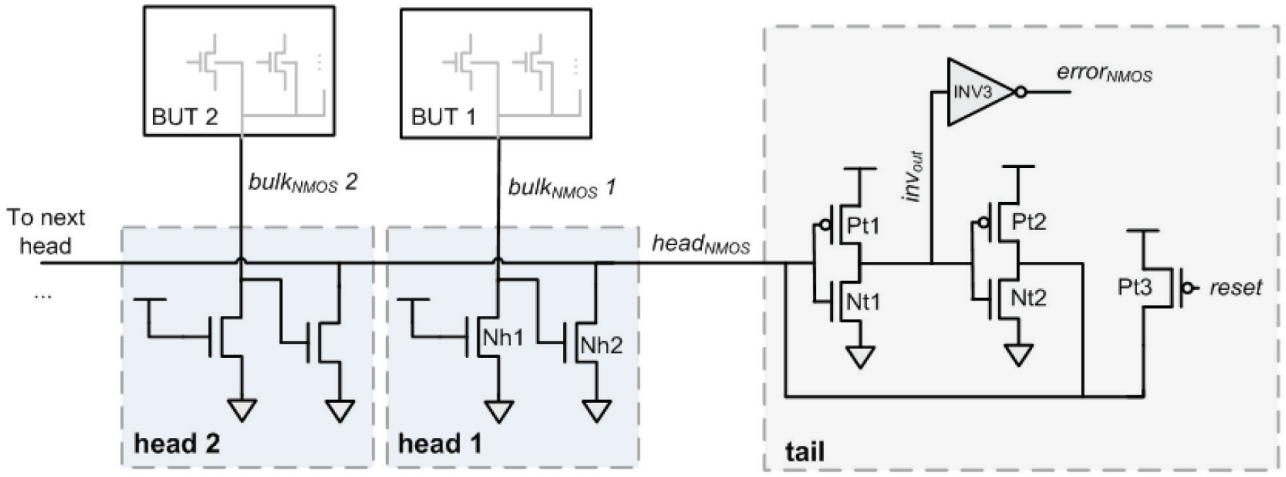

Figure 3: Structure of the proposed mBBICS (version for NMOS bulk)

A **tail** which is similar to an asynchronous latch consists of an inverter realized via the transistors Pt1 and Nt1 whose input is connected with $head_{NMOS}$. Its output inv_{out} feeds the gates of the devices Pt2 and Nt2, as well as the input of the inverter INV3. The output of the latter is the error signal $error_{NMOS}$. Further, the output of the inverter formed by Pt2 and Nt2 connects to $head_{NMOS}$ which is also connected to VDD via transistor Pt3 whose gate is controlled by the signal *reset*.

C. Mode of Operation

In normal operation, i.e. no particle strike occurs, the bulk is at GND level (at ⓪ in Fig. 4). Further, the net $head_{NMOS}$ has VDD potential and the devices Nh2 in the head modules are in off-state. In case of a particle strike within the BUT, a current flows through transistor Nh1 in the related head module. This results in a voltage drop over Nh1 based on its channel resistance. Consequently, the bulk level increases (at ① in Fig. 4) and Nh2 starts to conduct leading to a reduction of the $head_{NMOS}$ voltage level (at ② in Fig. 4).

In the tail block, the decrease of the level of $head_{NMOS}$ activates the inverter formed by Pt1 and Nt1, whereby the state of signal inv_{out} starts to change from GND to VDD (at ③ in Fig. 4). As consequence, transistor Pt2 changes from on-state to off-state, and Nt2 vice versa, which in turn decreases the level of $head_{NMOS}$ and, thus, forces the change of inv_{out} to VDD level. This positive feedback stops when inv_{out} reaches VDD level while $head_{NMOS}$ is at GND level. At the same time, the error signal $error_{NMOS}$ changes to GND level (at ④ in Fig. 4), which can be processed by higher instances as a flag indicating the occurrence of a transient fault. Consequently, the mBBICS has to be reset after such a process by changing Pt3 shortly into on-state (at ⑤ Fig. 4) and, thus, setting the level of $head_{NMOS}$ back to VDD level. It has to be observed that when a flag of fault is latched and during the reset of the mBBICS no new transient fault can be detected.

It should be observed that based on the described positive feedback and adequate sizing, which will be explained in the next subsection, it is not required that the head circuit reduces the signal $head_{NMOS}$ below VDD/2. Thus, variations of the head circuit characteristics have lower impact on the functionality of the mBBICS.

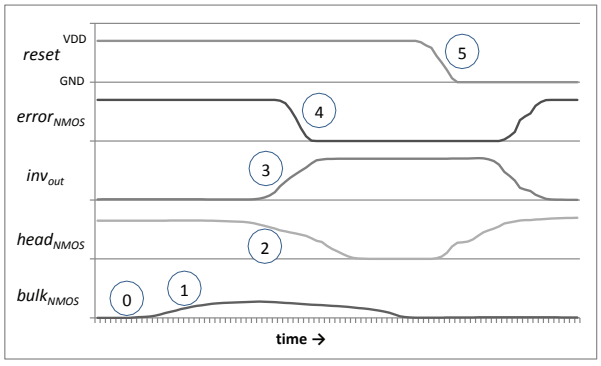

Figure 4. Voltage curves of a mBBICS (NMOS version) detecting a transient fault.

D. Sizing

The devices Nh1in the head modules must have a low *W/L* ratio (i.e. *L* is longer than *W*) to guarantee sufficient on-resistance. In contrast, the devices Nh2 must be sized with a great *W/L* ratio to assure that already minor changes of its gate-source voltage V_{gs_Nh2} result in considerably drain-source current I_{ds_Nh2} that changes the level of $head_{NMOS}$. As long as Nh2 is in its sub-threshold region, i.e. V_{gs_Nh2} is smaller than the threshold voltage of Nh2, I_{ds_Nh2} is equal to the sub-threshold leakage (see eq. 2). Hereby, the sensor profits from the high sub-threshold leakage of integrated circuits realized in nanometer technologies.

The devices Nt1 and Pt1 in the head module must be sized to support a GND-to-VDD change of

the net inv_{out}. Hence, Pt1 should have a high *W/L* ratio and Nt1 a small one. In a first guess, the transistors Pt2 and Nt2 of the following inverter should be sized to support a VDD-to-GND transition of the signal $head_{NMOS}$. This is true for Pt2. However, during our analysis of the mBBICS behavior in nanometer technologies we could observe that the leakage through Nt2 is critical as it is discharging the node $head_{NMOS}$. Therefore, Nt2 should be minimum sized, or even with a greater gate length which considerably reduces the leakage (see also eq. 1). Device Pt3 as well as the inverter can be minimum sized.

Table I. Transistor ratios for the applied mBBICS whereas the 1st number indicates the width factor and the 2nd the length factor (the omitted inverter INV3 is minimum sized). The device's dimension results from the product of the factor with the size of the technology node.

NMOS		PMOS	
Name	Ratio	Name	Ratio
Nh1	1/10	Ph1	1/11
Nh2	10/1.1	Ph2	14/1.15
Pt1	4/1	Pt1	1/10
Nt1	1/4	Nt1	10/1
Pt2	1/10	Pt2	1/2
Nt2	1/2	Nt2	1/20
Pt3	1/1	Nt3	1/1

IV. RESULTS AND DISCUSSION

This section presents the attained findings and discusses its implications.

A. Simulation Environment

All simulations are based on predictive 16 nm technology models using a VDD of 0.7 V [21][22]. Each Block Under Test (BUT) consists of six chains of ten inverters, whereas each inverter is sized with a driving strength of two. The bulk of all NMOS devices of a BUT is connected to one head circuit. In contrast, the bulk of the PMOS devices of each BUT is monitored by two head circuits whereas each head is connected to the bulk of the half of the PMOS transistors. This configuration assures equal capacitive load of the monitored PMOS and NMOS bulk. The transistor ratios of the modules of each mBBICS type are listed in Table I.

A particle strike was simulated by a current pulse based on eq. 1 at the output node of the 5th inverter of the first chain, in the following named sensitive node. All simulation were executed with a rise time t_r of 1 ps.

B. Nominal Case

At first, we determined the susceptibility of the BUT to particle strikes. Therefore, the collected charge Q_f and the decay time t_f (see also eq. 1) were varied; and the voltage peaks at the sensitive node and at the output node of the inverter chain were measured. Then, we defined a transient fault TF as a transient voltage peak that crosses VDD/2 at both these nodes.

Next, we estimated the mBBICS capability to detect TF if the parameters of the applied technology have its nominal values. Based on initial approximations of expected currents and capacitive loads we chose an mBBICS configuration with 6 heads and one tail circuit for the PMOS and NMOS version as reference implementation. The simulations were executed for the same Q_f and t_f values as in the analysis of the BUT susceptibility. The results, including the response time t_{resp}, are shown in Table II whereas ○× – marks that no TF and no detection occurred, ○✓– marks that no TF but a detection occurred, ✶× marks that a TF but no detection occurred, and ✶✓ – marks that a TF and a detection occurred. It can be seen that all transient faults could be detected by the mBBICS. However, for the highest charge a false detection happened for the NMOS as well the PMOS mBBICS. This case is unfavorable, though, as stated before its impact on the design performance is tolerable. Further follows that the maximum response time is 452 ps for the PMOS mBBICS and 430 ps for the NMOS version.

In the following step we analyzed the response time of the NMOS and PMOS mBBICS in function of the number of heads. Thereby, the simulations were executed for the case Q_f = 2 fC, t_f = 5 ps which was determined as lower border for the occurrence of a transient fault. The results as well as the area overhead are depicted in Fig. 5. The response time varies for the NMOS mBBICS between 157 ps and 598 ps while t_{resp} of the PMOS version is between 240 ps for and 734 ps. Thereby, the response time increases with rising number of heads which is based on the increasing capacitive load of the nets $head_{NMOS}$ and $head_{PMOS}$. Further follows that the maximum supported number of head circuits is 20 for the NMOS mBBICS and 22 for the PMOS version. A higher number leads to false detection without any particle strike. The reason for these false detections is the sub-threshold leakage of the Nh2 transistors in the head circuits. The area overhead starts with 49 % for mBBICS with only one head circuit and settles at around 21 % for the maximum supported number of heads. Thereby, for mBBICS with six heads the area overhead reduced already to 25 %. The results indicate that the previously chosen number of six heads offers a good compromise between response time and area offset.

Table II. Detection capability of proposed mBBICS in 16nm technology (6 heads, ○× no TF, no detection; ○✓ no TF, detection, ✶✓ TF, detection) and response time t_{resp}

Q_f	t_f	PMOS	t_{resp}	NMOS	t_{resp}
1 fC	5 ps	○×	-	○×	-
2 fC	5 ps	✶✓	452 ps	✶✓	430 ps
3 fC	5 ps	✶✓	136 ps	✶✓	76 ps
4 fC	5 ps	✶✓	89 ps	✶✓	50 ps
1 fC	10 ps	○×	-	○×	-
2 fC	10 ps	✶✓	270 ps	✶✓	210 ps
3 fC	10 ps	✶✓	78 ps	✶✓	62 ps
4 fC	10 ps	✶✓	55 ps	✶✓	43 ps
1 fC	20 ps	○×	-	○×	-
2 fC	**20 ps**	○✓	**210 ps**	○✓	**175 ps**
3 fC	20 ps	✶✓	81 ps	✶✓	70 ps
4 fC	20 ps	✶✓	55 ps	✶✓	50 ps

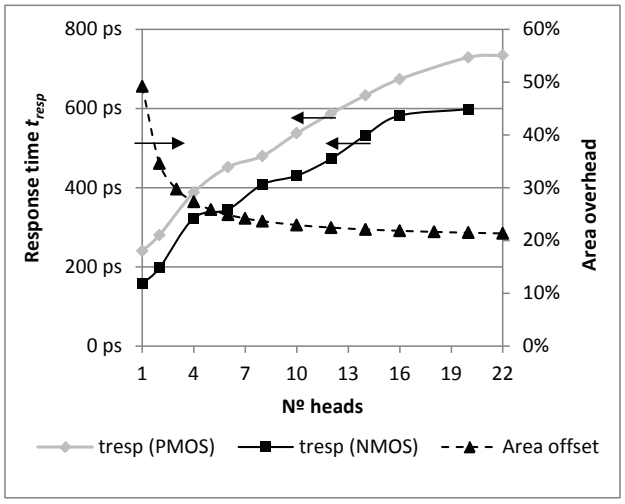

Figure 5. Response time t_{resp} and area offset for NMOS and PMOS mBBICS in function of the number of heads.

Next, we analyzed the influence of capacitive load of the signals $bulk_{NMOS}$ and $bulk_{PMOS}$ on the response time of the sensor. Therefore, we varied the amount of monitored minimum inverters, and thus the capacitive load of the bulk signal. Further, we determined the response times as well as the maximum voltage of the signal $bulk_{NMOS}$ and the minimum voltage of the signal $bulk_{PMOS}$, respectively, for a collected charge of Q_f = 4 fC, a decay time of t_f = 20 ps, and six heads. As in the analysis before, the bulk of the PMOS devices was monitored by two heads per chain. The results depicted in Fig. 6 indicate the expected increase of the response time t_{resp} with rising amount of monitored devices. This effect is mainly based on the decreasing absolute gate-source voltages V_{gs_Nh2} and V_{gs_Ph2} of Nh2 and Ph2, respectively, which is defined by the bulk voltage of the monitored devices (see also Fig. 3). Hence, with increasing capacitive load on the signals $bulk_{NMOS}$ and $bulk_{PMOS}$ the drain-source currents I_{ds_Nh2} and I_{ds_Ph2} of Nh2 and Ph2 are reduced and, consequently, the sensor response times increase.

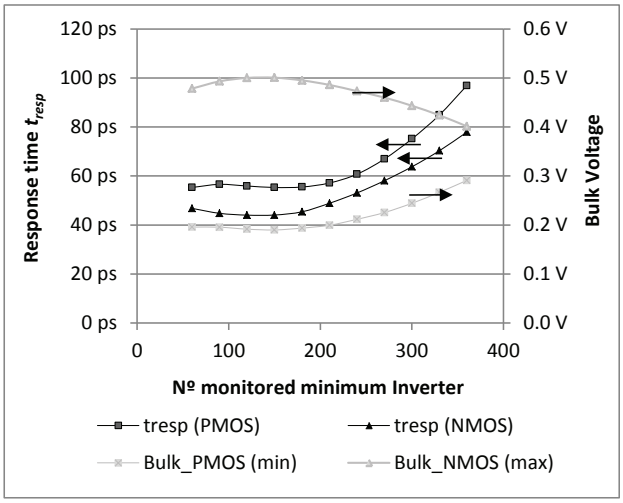

Figure 6. Sensor response time t_{resp} and bulk voltage in function of amnount of monitored minimum inverter (inverter driving strength is 1, 6 heads, Q_f = 4 fC, t_f = 20 ps).

In the last step, we determined the impact of the mBBICS on delay and power dissipation in normal operation, i.e. no particle strikes. We estimated the maximum delay of the inverter chains with and without connected mBBICS and could observe no differences. Next, we measured the dynamic power dissipation of the inverter chains for an input signal frequency of 2 GHz. For our reference implementation with 6 heads we could determine a power increase of 0.25 %. Thereby, the average bulk voltage varied only in the range of μV. Hence, it can be concluded that the power increase is solely based on the leakage power dissipation of the mBBICS. Finally, we compared the power dissipation in standby mode and estimated an increase of 3.5 % which is also only based on the leakage of the mBBICS.

C. Robustness Analysis

Robustness is a critical requirement for integrated sensors as the impact of environmental and technology parameter variations is continuously increasing. Thereby, the main influence on the sensor performance comes from temperature and process variations.

For the first robustness analysis we analyzed the response time as well as the functionality of the mBBICS in function of the temperature. All simulations were executed for the reference configuration with 6 heads, a collected charge of Q_f = 2 fC and a decay time of t_f = 5 ps. The results are depicted in Fig. 7. We could observe that for temperatures below -15ºC (PMOS mBBICS) and 0ºC (NMOS mBBICS), respectively, the transient fault could not be detected. Further, the simulations showed that for temperatures above 45ºC (PMOS mBBICS) and 60ºC (NMOS mBBICS), respectively, false detection occur. Hence, both mBBICS versions work in a range of 60 ºC. The response time in that range varies for the PMOS mBBICS between

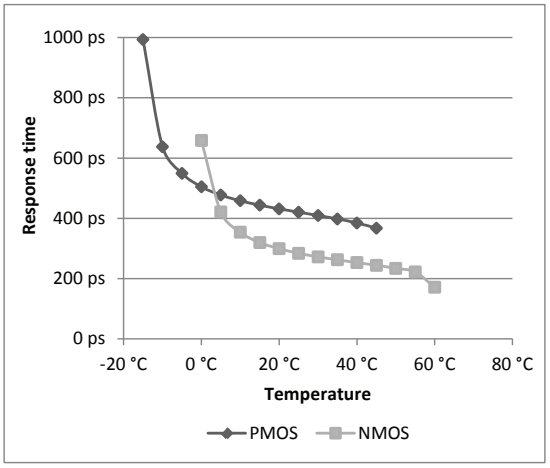

Figure 7. Response time in function of temperature (6 heads, Q_f = 2fC, t_f = 5 ps).

994 ps to 368 ps, and for the NMOS mBBICS between 659 ps and 171 ps. The response time decreases with rising temperature as higher temperatures lead to higher sub-threshold leakage I_{sub} [19]. Hence, the nodes $head_{NMOS}$ and $head_{PMOS}$ can change faster its voltage level. This increase of I_{sub} explains also the false detections at high temperatures.

In the following analysis MonteCarlo simulations were performed utilizing a normal distribution for the varied technology parameters. The expected values μ and the standard deviations σ for the modified BSIMv4 parameters are depicted in Table III [16]. It should be noted that especially the parameters affecting the threshold voltage v_{th}, like V_{th0}, *K1* and *NDEP*, may have the highest impact on the sensitivity of the sensor. For each configuration the recommended amount of 50 MonteCarlo simulations were executed [20].

Table III. Expected values (μ) and the standard deviations (σ) of normally distributed process parameters for MonteCarlo Simulations

Parameter	NMOS		PMOS	
	μ	σ	μ	σ
L_{int} (nm)	1.45	0.0483	1.45	0.0483
V_{th0} (V)	0.47965	1.6E-2	-0.43121	-1.4E-2
K1	0.4	0.013	0.4	0.013
μ_0 ($m^2V^{-1}s^{-1}$)	0.03	1E-3	0.006	2E-4
NDEP (cm^{-3})	7.0E18	2.3E19	5.5E18	1.8E19
xj (m)	5.0E-9	2.5E-10	5.0E-9	2.5E-10

At first, for the reference mBBICS configuration of 6 heads, we determined the functionality and maximum response time in function of the collected charge. The results are depicted in Fig. 8 and indicate a maximum response time of 1091 ps (PMOS mBBICS)

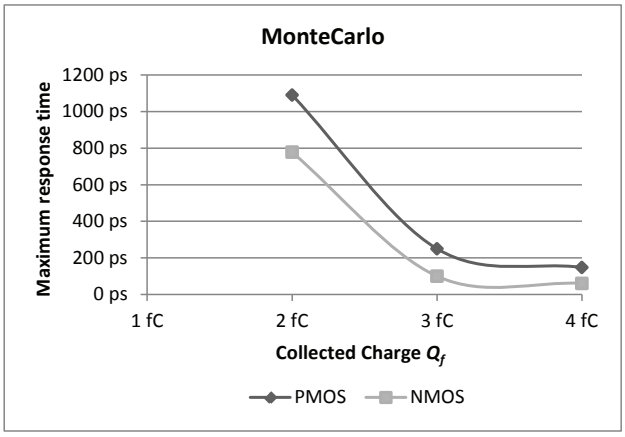

Figure 8. Maximum response time in function of collected charge Q_f (6 heads, t_f= 5 ps, 50 MonteCarlo simulations).

and 778 ps (NMOS mBBICS), both for the collected charge of 2 fC. Further, we could notice in all simulations that the transient faults could be detected, and in fault-free scenarios no case of false detection occurred. For a collected charge of Q_f = 1 fC, the NMOS mBBICS showed no false detection while the PMOS mBBICS had 6.

It should be noted that the variations of the threshold voltage v_{th} of the devices Nh1, Nh2 as well as Pt1, Pt2, Nt1 and Nt2 (see also Fig. 3) has the

Finally, the functionality and maximum response time for greater amount of chains were determined. Thereby, we could observe that up to 8 heads both mBBICS types never presented false detections when no particle strike occurred. The maximum response time increased to 1418 ps (PMOS) and 1384 ps (NMOS).

D. Scaling Analysis

An essential characteristic of integrated circuits is its scaling behavior, i.e. the change of circuit parameters due to scaling of technology sizes. Therefore, we implemented the mBBICS structure and Blocks Under Test (BUT) by using several predictive technologies [21][22] (16 nm, 22 nm, 32 nm, and 45 nm). The transistor dimensions are based on Table I with the sole exception of transistor Ph2 for the 32 nm version, which is made with the ratio of 14/1.05. The supply voltages are set to 0.8 V for the 22-nm technology, and to 0.9 V for the 32 nm and 45 nm technologies. All simulations were executed for the reference configuration with 6 heads and varying collected charge Q_f and decay time t_f, whereas the same values as for the sensor realized in 16 nm were applied. In a first attempt we analyzed the susceptibility of the BUT to particle strikes. Next, we compared the detection capability and the response time of the sensors.

Table IV. Comparison of detection capability of proposed mBBICS in 22-nm and 32 nm technologies (6 heads, ○× no TF, no detection; ○✓ no TF, detection, ✶✓ TF, detection)

Q_f	t_f	22 nm		32 nm	
		PMOS	NMOS	PMOS	NMOS
1 fC	5 ps	○×	○×	○×	○×
2 fC	5 ps	✶✓	○✓	○×	○×
3 fC	5 ps	✶✓	✶✓	✶✓	○✓
4 fC	5 ps	✶✓	✶✓	✶✓	✶✓
1 fC	10 ps	○×	○×	○×	○×
2 fC	10 ps	✶✓	○✓	✶✓	✶✓
3 fC	10 ps	✶✓	✶✓	✶✓	✶✓
4 fC	10 ps	✶✓	✶✓	✶✓	✶✓
1 fC	20 ps	○×	○×	○×	○×
2 fC	20 ps	✶✓	○✓	✶✓	✶✓
3 fC	20 ps	✶✓	✶✓	✶✓	✶✓
4 fC	20 ps	✶✓	✶✓	✶✓	✶✓

From the results shown in Table IV follows that the proposed mBBICS designed in 22 nm and 32 nm technologies could detect all transient faults. In four cases, though, the NMOS version had false detection. The comparison of the response times t_{resp} for a collected charge of Q_f = 4 fC and the technology nodes 16 nm, 22 nm, and 32 nm is depicted in Fig. 9. The results indicate at a decay time t_f of 5 ps an increase of t_{resp} of more than factor 2 for the 32 nm NMOS version and an increase of 23 % for the 22 nm NMOS version. For longer t_f the differences of the response times reduce to 6 % (16 nm vs. 22 nm) and 23 % (16 nm vs. 32 nm), respectively. A similar behavior can be observed for the PMOS versions.

In contrast to the other versions, the mBBICS based on the 45 nm technology could not detect any transient fault. A closer analysis revealed that this misbehavior is due to the higher threshold voltage V_{th} of the 45 nm technology devices and the insufficient increase of the voltage $bulk_{xMOS}$ in case of a particle strike. Fig. 10 and Fig. 11 illustrate this by comparing the behavior of NMOS mBBICS sensors designed in 16 nm and 45 nm technologies. From Fig. 10 follows that the voltage $bulk_{NMOS}$ of the 45 nm version does not reach the level of threshold voltage of ca. 0.45 V in case of a particle strike. Thus, the drain-source current I_{ds_Nh2} of the device Nh2 is not sufficient to discharge the signal $head_{NMOS}$, which is essential for detection of transition faults (see Fig. 10 and Fig. 11). A solution could be the reduction of the amount of monitored devices. However, only a decrease by more than 60 % of that amount leads to a sensor that is able to detect all transient faults. Thus, it can be concluded that the application of mBBICS is not recommended for this 45 nm technology since the resulting area offset due to the mBBICS would be almost 75 %.

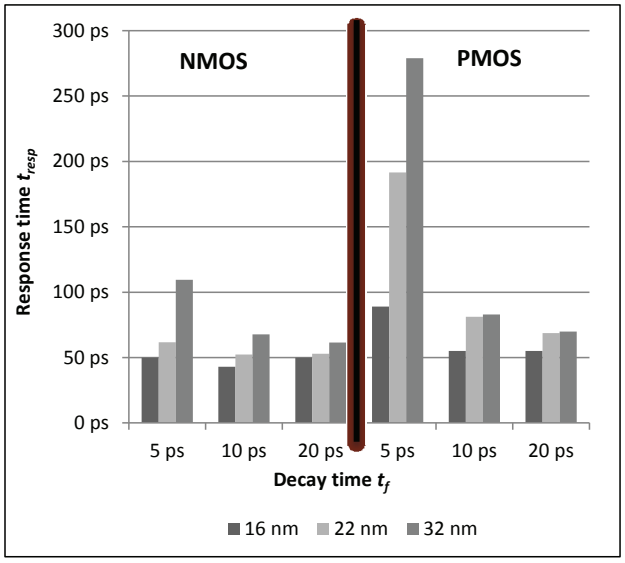

Figure 9. Comparison of response time t_{resp} of NMOS and PMOS mBBICS for technology nodes 16 nm, 22 nm and 32 nm in function of decay time t_f (6 heads, Q_f = 4 fC).

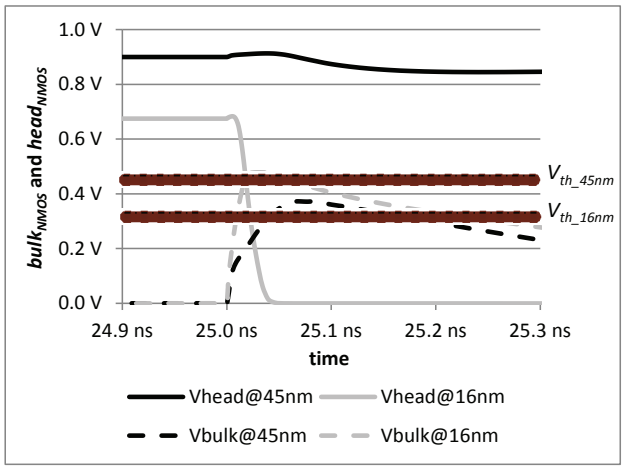

Figure 10. V_{bulk} and V_{head} during particle strike in NMOS mBBICS realized in 16 nm and 45 nm technologies (6 heads, Q_f = 4 fC, tf = 20 ps).

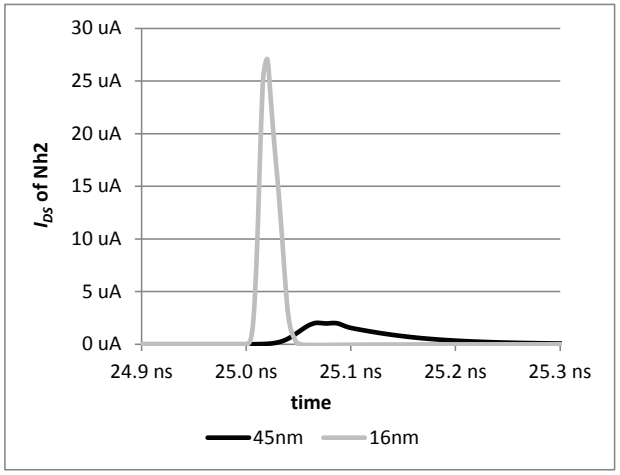

Figure 11. Drain-source current of Nh2 in NMOS mBBICS realized in 16 nm and 45 nm technologies during particle strike (6 heads, Q_f = 4 fC, t_f = 20 ps).

V. CONCLUSIONS

Bulk Built-In Current Sensors (BBICS) offer a promising solution to cope with soft error problems in current nanometer technologies. However, this kind of sensors suffers from its susceptibility to temperature and parameter variations, as well as area and power increase. The proposed modular BBICS applies functional block sharing and positive feedback to mitigate these problems. Simulations with a predictive 16 nm technology indicate that the proposed sensor can detect all injected transition faults with response times below 500 ps for the nominal case, and 1 ns under wide process and temperature variations. This could be achieved a very low increase in power dissipation and with an area offset of 25 %, which is low compared to other techniques focusing on transition fault detection.

Future works will concentrate on the realization of BBICS in an actual nanometer technology and the analysis of the influence of ground bounce based on layout data.

ACKNOWLEDGEMENTS

This work was supported by PRPq/UFMG, FAPEMIG, and DISSE/CNPq.

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