A Novel Pseudo NMOS Integrated CC -ISFET Device for Water Quality Monitoring

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ABSTRACT

The paper presents a performance analysis of Novel CMOS Integrated Pseudo NMOS CC –ISFET (PNCC-ISFET) having zero static power dissipation. The main focus is on simulation of power and performance analysis along with the comparison with existing devices, which are used for water quality monitoring. This approach can improve calibration of device to a fairly wide range without the use of a high speed digital processor. The conventional devices generally used, consume high power and are not stable for long term monitoring. The conventional devices have a drawback of low value of slew rate, high power consumption, and non linear characteristics. In the proposed design(PNCC-ISFET) due to zero static power, low value of load capacitance on input signals, faster switching, use of fewer transistors and higher circuit density the device exhibits a better slew rate, piece-wise linear characteristic, and is seen consuming low power of the order of 30mW. The functionality of the circuit is tested using Tanner simulator version 15 for a 70nm CMOS process model. The proposed circuit reduces total power consumption per cycle, increases speed of operation, is fairly linear and simple to implement. This device has a simple architecture, and hence is very suitable for water quality monitoring applications.

Index Terms: Calibration; Simulation; Monitoring; Ion Sensitive Field Effect Transistor; Simulation; Frequency compensation and Low power

I. INTRODUCTION

Water is vital for all known forms of life. With the expansion of industrial production and increase in the population every year, wastewater produced by industry discharged into rivers and lakes due to which the quality of water is degraded. Hence, it is most urgent to take effective measure to monitor and protect the water resources. The supervision of water quality is generally done by taking and analysing some sample liquid in the laboratory. This method is very expensive, tedious and it can take several weeks to get tests result. Many research works have contributed to design quality measuring devices [1-3]. But it's always a challenge to select a more precise and accurate device for monitoring the quality of water. In Today's scenario very complex functions are realized. Also, there is a growing demand for high density VLSI circuit's which result in scaling of V_{dd} and an exponential increase of leakage or static power in deep sub-micron technology. Therefore reducing static power consumption of portable devices for water quality monitoring applications is highly desirable for a long term monitoring. As the size of the transistor decreases (i.e Technology) the transistors density per unit chip increases. Due to scaling of the device and large integration of the transistors on the single chip leads to increase in temperature and higher power consumption [2]. This increase in temperature will increase the overall cooling cost and complicated packaging techniques.

The total power consumption in high performance digital circuits is mainly due to leakage currents. Leakage power makes up to 40% of the total power consumption in today's high performance monitoring circuits. Hence, leakage power reduction is very necessary for a low power design. The leakage power dissipation is given by (1).

$$P_{static} = I_{leak} * V_{dd} \quad (1)$$

Where I_{leak} is the leakage current when the transistor OFF and V_{dd} is the supply voltage. The leakage current consists of following components

(i) Gate leakage
(ii) Sub threshold leakage
(iii) Reverse biased junction leakage
(iv) Gate induced drain leakage.

Out of these, sub-threshold leakage and gate-leakage currents are dominant. The sub threshold leakage current of a MOS device is given by (2) and (3).

$$I_{sub}=I_0 \exp [(V_{gs}-V_t) /(n V_T)]$$

$$[1- \exp (-V_{ds}/V_T)] \quad (2)$$

$$I_0=\mu_{eff} Cox (W/L) V_T^2 \quad (3)$$

Where W and L are width and length of the channel respectively, V_t is the threshold voltage, μ_{eff} is the electron/hole mobility, C_{ox} is the gate oxide capacitance per unit area, n is the sub-threshold swing coefficient, V_T is the thermal voltage, V_{gs} is the transistor gate to source voltage and V_{ds} is the drain to source voltage.

II. ISFET

An ISFET is an ion sensitive field effect transistor which has a property of measuring ion concentrations in solutions. When the ion concentration (such as H^+) changes, the current through the transistor will change accordingly. Here, the solution is used as the gate electrode. A voltage between substrate and oxide surface arises due to ion's sheath. The ISFET has the similar structure as that of the MOSFET except that the poly gate of MOSFET is removed from the silicon surface and is replaced with a reference electrode inserted inside the solution, which is directly in contact with the hydrogen ion (H+) sensitive gate electrode [3] The Sub circuit block of ISFET macro model is shown in Figure 1.

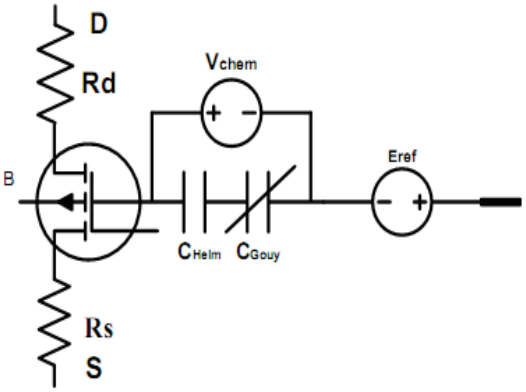

Figure 1: Sub circuit block of ISFET macro model.

At the interface between gate insulator and the solution, there is an electric potential difference that depends on the concentration of H+ ion of the solution, or otherwise pH value. The variation of this potential caused by the pH variation will lead to modulation of the drain current. As a result, the I_d - V_{gs} transfer characteristic of the ISFET, working in triode region is similar with that of MOSFET:

$$I_{ds}=\frac{\mu C_{ox} W}{L}\left[(V_{gs}-V_{th\_isfet})\, V_{DS}-\frac{1}{2}(V_{ds})^2\right] \quad (4)$$

The threshold voltage is only different in case of MOSFET. In ISFET, defining the metal connection of the reference electrode as a remote gate, the threshold voltage is given by:

$$V_{th\,(ISFET)} = E_{Ref} + \Delta\phi^{1j} - \Psi_{eol} + \chi^{sol} + \frac{-\phi_s}{q} - \frac{Q_{ox}+Q_{ss}}{C_{ox}} + \gamma\{2\varphi£\}^{1/2} + 2\phi_£ \quad (5)$$

Where E_{Ref} is potential of reference electrode, $\Delta\phi^{1j}$ is the potential drop between the reference electrode and the solution, which typically has a value of 3mV [4]. Ψ_{eol} is the potential which is pH-independent; it can be viewed as a common-mode input signal for an ISFET interface circuit in any pH buffer solution and can be nullified during system calibration and measurement procedures with a typical value of 50 mV [5]. χ^{sol} is the surface dipole potential of the solvent being independent of pH., the terms in the parentheses are almost same as that of MOSFET threshold voltage except the gate metal function $\phi_£$. The other terms in above equation are a group of chemical potential, among which the only chemical input parameter shown has to be a function of solution pH value. This chemical dependent characteristic has already been explained by the Hal and Eijkel's theory which is elaborated using the generally accepted site binding model and the Gouy-Chapman-Stern model. Conventional water quality monitoring devices are made up of voltage mode circuits (VMC) based on op-amps and OTA's(operational trans conductance amplifier). These applications suffer from low band widths (BW's) arising due to stray and circuit capacitances. Also the need for low voltage, low power circuits make these devices not suitable for water quality monitoring. [6]. However, with the advancement in VLSI devices new analog current mode devices are developed which are very useful in the water quality monitoring application These circuits have a significant advantage of low power, low voltages and can operate over wide dynamic range. These circuits have large bandwidths, greater linearity and simple circuitry which consume low power. Current feedback op-amps (CFOAs), operational floating conveyors (OFCs) and current conveyors (CCs) etc. are popular CMC configurations and the most widely used device among them is second generation current conveyor CC-II. Hence, Pseudo NMOS based CC-II is designed to perform as the heart of water quality monitoring device.

III. CURRENT CONVEYOR

Current Conveyor (CC-II) has proved to be a versatile analog building block that can be used to implement numerous analog processing applications;

it was introduced by Sedra and Smith [7]. The current conveyor is a grounded three-port network represented by the black box as shown in Figure 2. The general Current Conveyor (CC) can be represented by the following input-output matrix relation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

When a = 1, the first generation current conveyor (commonly denoted CCI) is obtained. For a = 0, we obtain the second generation current conveyor (commonly denoted CCII). For a = -1 we obtain the third generation current conveyor (commonly denoted CCIII). Usually, b = ±1. The sign of the parameter b determines the conveyor current transfer polarity. Positive b indicates that the CC has a positive current transfer ratio and is denoted by CCI+, CCII+ or CCIII+ while negative b means that it has a negative current transfer ratio and is denoted by CCI-, CCII-or CCIII-.

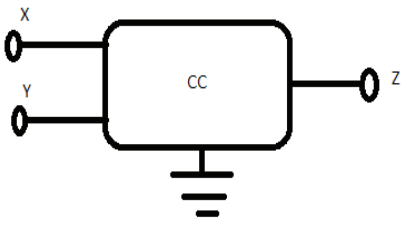

Figure 2: Block diagram of current conveyor

A well known basic building block is the second generation current conveyor (CCII). Second generation current conveyors are widely used by analog designers. An important attribute of current conveyor is its ability to convey current between two terminals (X and Z) at vastly different impedance levels.

IV. PSEUDO-NMOS LOGIC

Pseudo-NMOS logic is a ratioed logic which uses a grounded PMOS load as a Pull up and an NMOS driver circuit as pull-down network that realizes the logic function. The main advantage of this logic is that it uses only N+ 1 transistors as compared to 2N transistors for CMOS also, this logic have less load capacitance on input signals, faster switching, higher circuit density. In Pseudo NMOS logic the high output voltage level for any gate is V_{dd} and the low output voltage level is not 0 volt [8]. The only one main drawback of this logic is very high static power consumption as there exists a direct path between V_{dd} and ground through the PMOS transistor. In order to make low output voltage as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down devices. But to increase the speed particularly when driving many other gates the PMOS transistor size has to be made larger. Therefore there is always a trade-off between the parameters such as noise margin, static power dissipation and propagation delay.

Various methods used for decreasing static power in Pseudo NMOS logic are reverse body bias (RBB) and transistor stacking.

A. Reverse body bias

This is an effective approach to reduce leakage power. In this method, when the circuit enters the standby mode, reverse body bias is applied to increase the threshold voltage V_T of the transistors and this decreases the sub-threshold leakage current. V_T is related to the reverse bias voltage between the source and body V_{sb} by the following Eq. (6).

$$V_T = V_{To} + \gamma \left(\sqrt{(2\Phi_f + |V_{sb}|)}\right) - \sqrt{2\Phi_f} \qquad (6)$$

Where V_{To} is the zero bias V_T for V_{sb} = 0 volt, ϕ_f is a physical parameter and γ is a fabrication process parameter. Modification of V_T can be achieved by changing $|V_{sb}|$. This method can be either applied at the full chip level or at a finer granularity. The advantage of this method is that it can be implemented without incurring any delay penalty. The key issue is that the range of threshold adjustment is limited, which in turn limits the amount of leakage reduction.

B. Transistor stacking method

Transistor stack is a leakage reduction technique that works both in active and stand bye mode. It is based on the observation that two OFF state transistors connected in series cause significantly less leakage than a single device. This effect is known as the "Stacking Effect". When two or more transistors that are switched OFF are stacked on top of each other, then they dissipate less leakage power than a single transistor that is turned OFF. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage.

V. DEVICE DESCRIPTION AND ANALYSIS

For the integrated sensor, the measurement circuit tracks the threshold voltage (or the flat-band voltage) of the ISFET as the electrolyte pH is varied. A practical solution to integrate the sensor with electron-

ics is to view the ISFET sensor as a circuit component in an integrated circuit rather than as an add on sensor whose output signal is further processed. In this paper, the ISFET is used as one of the input transistors in the differential stage of the current conveyor as shown in Figure 3. The circuit functions as follows: when the ISFET-Current Conveyor is configured as a voltage follower, the output voltage (V_o) is equal to the input voltage (V_{in}); any difference in threshold voltages and bias currents between the two input transistors at the differential input stage will also appear at the output. The distinct advantages of Pseudo NMOS is less load capacitance on input signals, faster switching due to fewer transistors, higher circuit density which motivate us to implement this novel design. The only disadvantage of Pseudo NMOS logic is that pull up is always ON due to which there is significant static power dissipation. There are several methods already discussed above to reduce the static power dissipation but there is no method which completely avoids this drawback. In this novel design the circuit has zero static power dissipation. The given circuit is designed in Pseudo NMOS technology in which gate of PMOS is grounded. There is one NMOS just above the grounded PMOS which acts as a switch and ON only when input is applied, otherwise OFF. Since the circuit is only ON when the input signal is applied hence there is no direct path from V_{dd} to ground which prevent the circuit from the static power dissipation.

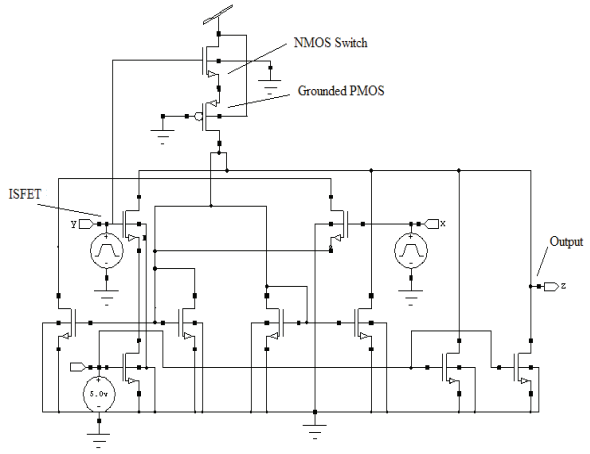

Figure 3: Circuit diagram of Pseudo NMOS CC-ISFET.

A. Transient analysis

Transient analysis of the PNCC-ISFET is observed on Tanner tool Version 15 and it is found that the output is fairly linear with respect to input with the passage of time as shown in Figure 4 below.

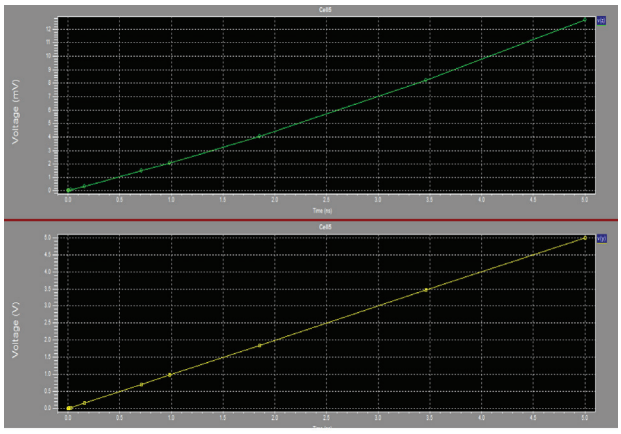

Figure 4: Transient analysis of PNCC-ISFET.

B. Mathematical Regression Analysis

The Regression statistics including multiple R, R square Adjusted R square and Standard error obtained during experiment is shown in Table 1.

Table1. Regression Statistics

Regression Statistics	
Multiple R	0.998428255
R Square	0.99685898
Adjusted R Square	0.996662667
Standard Error	0.08121496
Observations	18

On plotting a linear trend line between V_y and V_z the coefficient of determination R^2 is found to be 99.7% with standard error of 0.081 shown in Figure 5. The coefficient of determination R^2 is useful because it gives the proportion of the variance (fluctuation) of one variable that is predictable from the other variable. It is a measure that allows us to determine how certain one can be in making predictions from a certain model. The coefficient of determination is a measure of how well the regression line represents the data. If the regression line passes exactly through every point on the scatter plot, it would be easy to explain all the variations.

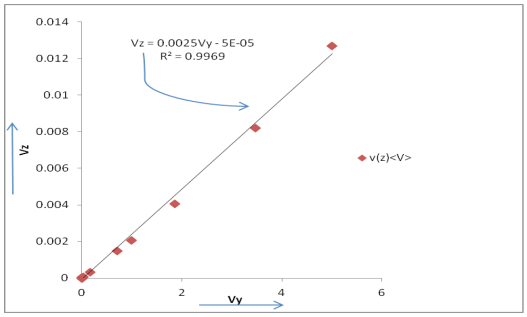

Figure 5. Trend line between Vy and Vz obtained from SPICE model readings with coefficient of determination R^2

C. Residual plot

A residual plot between output and input shows that for a regression model to be good fit when residues are random. There should be no recognizable pattern. Good regression models give uncorrelated residuals. The residual Plot for the device is plotted and shown in given Figure 6.

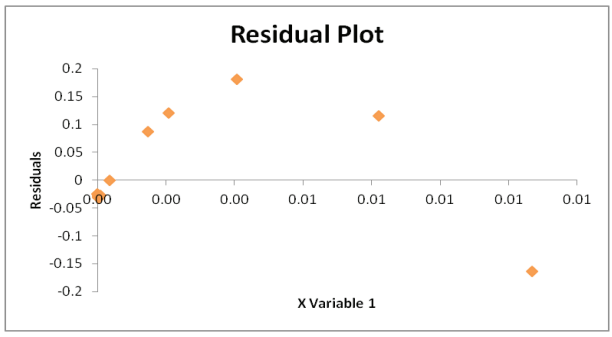

Figure 6. Residual Plot of PNCC-ISFET

D. Normal Probability Plot

The normal probability plot is a special case of the probability plot. The points on this plot form a nearly linear pattern, which indicates that the normal distribution is a good model for this data set. The normal Probability plot for the device is plotted and shown in Figure 7.

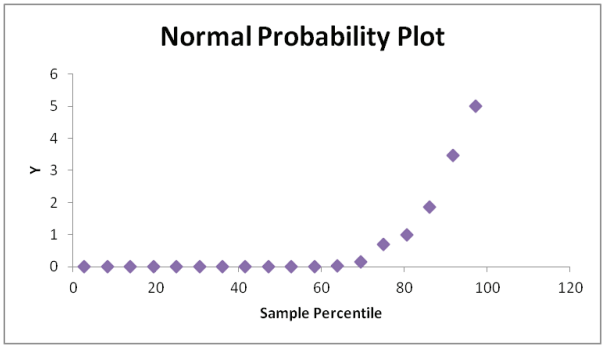

Figure 7. Normal Probability Plot of PNCC-ISFET

VI. RESULT ANALYSIS

The various results obtained are summarized in this section. Figure 8 and 9 shows component count and the power consumption comparisons.

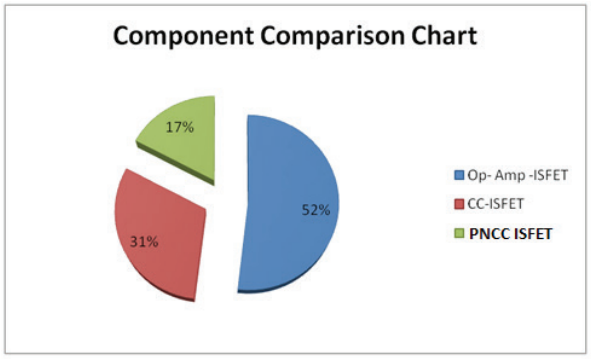

Figure 8. Component Comparison Chart

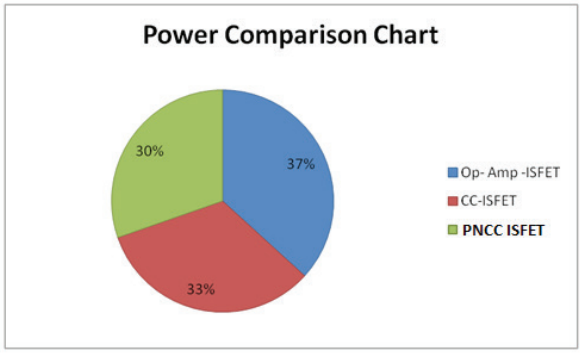

Figure 9. Power Comparison Chart

Table 2. Comparative analysis with existing devices

Parameters	Op- Amp – ISFET [9]	CC-ISFET [10]	PPCC-ISFET
Technology	CMOS	CMOS	Pseudo PMOS
Power supply	5V-0V	5V-0V	5V-0V
No. of Mosfets	27	16	9
Capacitor	2	2	1
Current Source	4	3	0
NMOS	17	10	8
PMOS	10	6	1
Resistor	5	5	0
Voltage Source	4	2	1
Max power (W)	3.63e-002	3.57e-002	3.00e-002
Min power (W)	2.13e-005	0.13e-005	0.00e+000
Stability analysis	Closed loop Stable	Closed loop Stable	Closed loop Stable

On comparing new design with the existing designs as shown in Table 2 we arrive at the following results:

a) Number of MOSFET's used are 27 in [9] and 16 in [10] for the conventional devices where as only 9 transistors are used in new proposed device. The new proposed device deploys only 17% of components as compared to 52% in [9] and 31% in [10].
b) The new proposed device consumes almost zero static power.
c) No capacitor and resistor is used in the new technique.

d) Number of current sources deployed is zero in the new proposed device.
e) Number of n-MOS and p-MOS transistors required for simulation of this device are 8 and 1 only.
f) Voltage sources required for proper operation of the de-vices mentioned in table 3 are 4 in [9] and 2 in [10] for con-ventional devices and 1 in new device.

As we know, volumetric efficiency measures the performance of function per unit volume. In this age of electronics, this is desirable since advanced designs need to cram increasing functionality into smaller packages. The concept of volumetric efficiency appears in the design and application of capacitors, where the "CV product" is a figure of merit calculated by multiplying the capacitance (C) by the maximum voltage rating (V) divided by the volume. From this table, we can figure out that there is significant saving in terms of components. Hence, we come to a conclusion that the circuit proposed here, meets all our requirements in terms of component saving, miniaturization and power efficiency.

VII. CONCLUSION

In this novel design, a new device employing PNCC-ISFET is proposed. PNCC introduced a convenient building block that provides a simplified approach to the design of linear analog systems. It also consumes considerably low power. There is significant improvement in the slew rate. The output observed is highly linear as it is evident from Figure 4. A significant advantage of the proposed design is it's simple architecture, and low component count. Therefore it is very suitable for water quality monitoring applications. This study may be extended for further improvements in terms of power and size, besides the wiring and layout characteristics level.

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