Nanowire Tunnel Field Effect Transistors at High Temperature

Márcio D. V. Martino[1], Felipe S. Neves[1], Paula G. D. Agopian[1], João A. Martino[1], Rita Rooyackers[2] and Cor Claeys[2,3]

[1]LSI/PSI/USP – University of Sao Paulo, Brazil
[2]Imec, Kapeldreef 75, B-3001 Leuven, Belgium
[3]E.E. Dept, KULeuven, Leuven, Belgium
email: martino@lsi.usp.br

ABSTRACT

The aim of this work is to study how the performance of nanowire tunnel field effect transistors (TFETs) is influenced by temperature variation. First of all, simulated energy band diagrams were presented to justify its fundamental working principle and this analysis was compared to experimental data obtained for temperature ranging from 300 to 420 K. This methodology was performed for different nanowire diameters and bias conditions, leading to a deep investigation of parameters such as the ratio of on-state and off-state current (I_{ON}/I_{OFF}) and the subthreshold slope (S). Three different transport mechanisms (band-to-band tunneling, Shockley-Read-Hall generation/recombination and trap-assisted tunneling) were highlighted to explain the temperature influence on the drain current. As the final step, subthreshold slope values for each configuration were compared to the room temperature. Therefore, it was observed that larger nanowire diameters and lower temperatures tended to increase I_{ON}/I_{OFF} ratio. Meanwhile, it was clear that band-to-band tunneling prevailed for higher gate voltage bias, resulting in a much slighter temperature effect on the drain current.

Index Terms: Tunnel FETs, Nanowire, Temperature

I. INTRODUCTION

The continuous MOSFET devices scaling led to the most recent technology nodes, in which transistors present dimensions of tens of nanometers. This very famous evolution turned some behaviors such as short-channel effects and leakage currents, often neglected in the past, in important roadblocks for the most recent devices. Considering also that the supply voltage has not been scaled down accordingly, power dissipation became a major issue [1].

The use of new materials has been proposed, but these approaches still face the limit of carrier diffusion over a thermal barrier. After all, this transport mechanism models result in a minimum slope of 60mV/decade at room temperature, or generally ln(10).k.T/q [2].

Consequently, devices with different operation principles have been focused on recent studies, taking into consideration the need of reducing the threshold and the supply voltage. For instance, the concept of Tunnel field effect transistors (TFETs) has been proposed as an alternative to overcome the previously mentioned concerns [3] and will be highlighted in this work.

These devices present a structure with Si-based gated p-i-n diode and are biased in a way that the main current is due to band-to-band tunneling controlled by the gate. For that reason, it is expected that these devices will present reduced values of subthreshold swing and lower short-channel effects. It is also worth remembering that standard CMOS processing techniques are still allowed, since there is a patent correspondence to SOI MOSFET structures. This work in particular will focus on 3D devices, based on vertical nanowires [4].

On the other hand, it is important to remember that this proposal must face two main issues, i.e., the comparatively low values of on-state current and the intrinsic ambipolarity. Sophisticated fabrication techniques and physical features optimizations are among the most recent proposals to tackle these concerns [5, 6].

To sum up, the aim of this work is to highlight TFET nanowires with slight physical dimensions differences, studying the temperature impact on key parameters such as the subthreshold slope and the I_{ON}/I_{OFF} ratio.

II. DEVICE CHARACTERISTICS

The performance of tunnel FETs will be analyzed based on experimental data obtained with devices fabricated in imec (Leuven, Belgium). HP4156C was used to perform electrical characterization for transistors with different values of quantity of wires, spacing between wires and nanowire diameter.

Simulations were executed with the objective of justifying its working principle and comparing the relevance of each transport mechanism under varying bias conditions.

A nanowire p-i-n structure was designed in the simulator, highlighting N-type transistors. Following the standard proposed by other reports, drain was set as the 1.10^{20} cm^{-3} n+ doped zone, channel as the lowly doped region (5.10^{15} cm^{-3}) and source as the 5.10^{19} cm^{-3} p+ doped zone. A P-type TFET device could be easily simulated by changing p+ and n+ doping with each other.

Simulated devices were modeled with total channel length, gate length and gate/drain underlap of 200 nm, 150 nm and 100 nm, respectively. There was a gate/source overlap of 30 nm and an EOT (equivalent gate oxide thickness) of 1.6 nm. Channel and drain were composed by Silicon and source by $Si_{0.8}Ge_{0.2}$. Figure 1 exhibits the simulated structure and its mentioned dimensions.

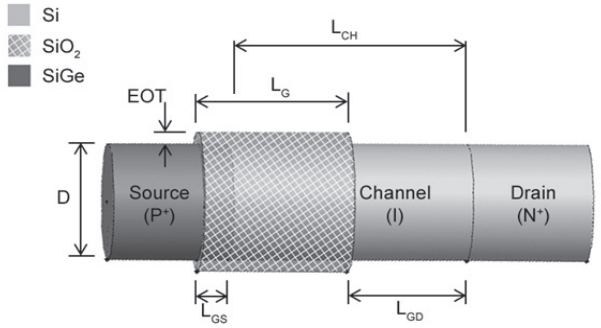

Figure 1. Schematic structure of the simulated TFET devices.

L_{CH} = total channel length
L_G = gate length
L_{GD} = gate/drain underlap
L_{GS} = gate/source overlap

Lastly, all the numerical 3D simulations were performed by using Sentaurus [7]. Convergence and accuracy were taken into consideration when the mesh in the tunneling zone was defined.

III. METHODOLOGY

As previously mentioned, quantitative analyses will be based on parameters such as the subthreshold slope (S), directly related to the suitability in scaled down dimensions, and the on-state and off-state current ratio (I_{ON}/I_{OFF}).

The subthreshold swing was obtained from the curves of the drain current as a function of the gate voltage (I_{DS} x V_{GS}). Its numerical value could be extracted from the derivative of ($\log I_D$ x $V_{GS})^{-1}$ curve, with gate voltage varying from -0.4 to +2 V.

Meanwhile, the drain voltage (V_{DS}) was set to 0.9 V in order to guarantee relevant values of tunneling current. Subsequently, I_{ON}/I_{OFF} ratio was calculated considering the same I_{DS} x V_{GS} plots and defining I_{ON} as the drain current for V_{GS} = +2 V and I_{OFF} as the drain current for V_{GS} = 0 V.

This procedure was repeated for devices with different diameters (ranging from 83 to 213 nm) and under different temperatures (ranging from 300 to 420 K) and the results have been compared witch each other so that the optimized conditions were identified.

IV. SIMULATED RESULTS AND DISCUSSION

Figure 2 shows the simulated curve of the drain current as a function of the gate voltage, indicating also the most relevant transport mechanisms in each region of the graph. Figure 3 presents the energy band diagram along source, channel and drain, keeping drain voltage constant as 0.9V.

By analyzing the simulated band diagrams, it is possible to observe that there is no band gap narrowing when the gate voltage is lower 0.5 V (Figure 3A). As a result, the band-to-band tunneling can be neglected and the leakage current (I_{OFF}) is composed by junction leakage current and Shockley-Read-Hall (SRH) recombination mechanism [9, 10].

Increasing gate voltage for values close to 0.5 V (Figure 3B), there is a narrowing in the difference between the valence band maximum and the conduction band minimum, leading to a trap-assisted-tunneling (TAT). This mechanism was simulated considering the traps at the band gap center (ETRAP = 0 eV) and causes a very steep increase in the drain current. This makes possible subthreshold swing values below 60 mV/decade at room temperature, reaching 40 mV/decade in the curve presented in Figure 2.

Meanwhile, band-to-band tunneling becomes relevant when the gate voltage gets closer to 1.0 V (Figure 3C), when trap-assisted tunneling is still important (TAT + BTBT).

Finally, when the maximum of the drain valence band becomes higher than the minimum of the channel conduction band (Figure 3D), there is a strong bandgap narrowing. Therefore, higher values of V_{GS} make BTBT prevail over all the other mentioned mechanisms.

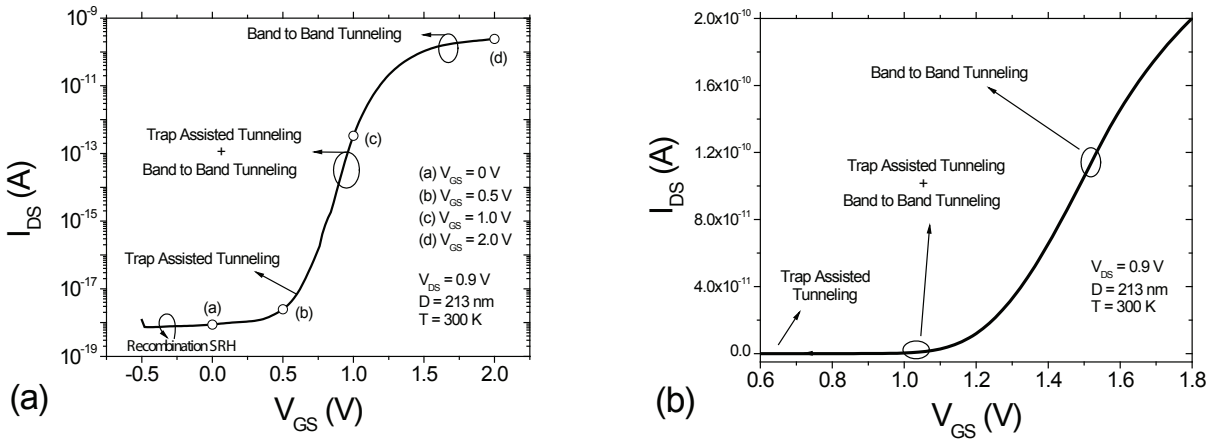

Figure 2. Schematic I_{DS} as a function of V_{GS} curve, indicating the predominant transport mechanism in each V_{GS} bias. I_{DS} is represented in logarithmic (a) and in linear (b) scale.

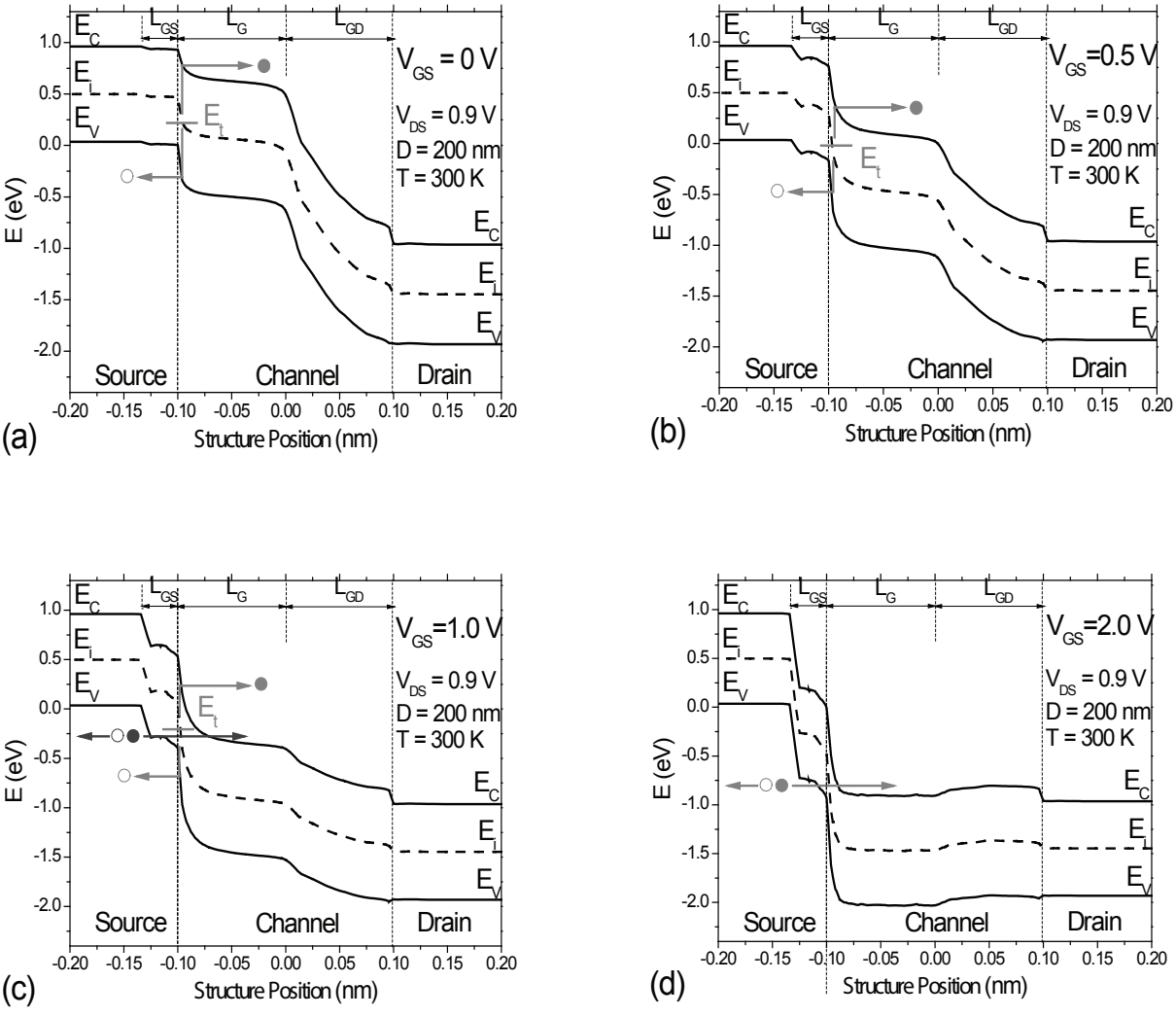

Figure 3. Enegy bandgap diagram for V_{GS}=0V (a) V_{GS}=0.5V (b) V_{GS}=1V (c) V_{GS}=2V (d).

V. EXPERIMENTAL RESULTS AND DISCUSSION

A. Influence of the TFET dimensions on the subthreshold swing and I_{ON}/I_{OFF}

As described in the Methodology section, experimental data will focus on the variation of the drain current with different gate voltages, drain voltages, nanowire diameters and temperature. The value of I_{ON}/I_{OFF} ratio will be used to establish a comparative analysis on the devices suitability.

Figure 4 presents the results for transistors with nanowire diameter of 98, 160 and 213 nm.

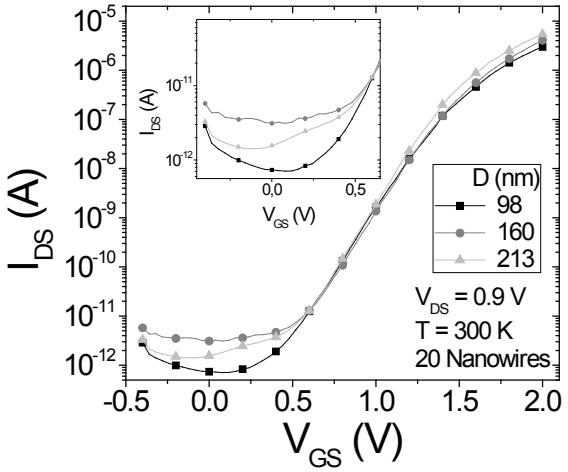

Figure 4. I_{DS} as a function of V_{GS} curves for devices with different diameters at room temperature.

The obtained curves exhibit the TFETs behavior that was previously explained and supported by the band diagrams for different bias conditions. Comparing I_{ON} (drain current for V_{GS} = 2 V) for these devices, it was noticed an increase of on-state current for higher values of diameter.

Focusing on the off-state region, it is possible to notice that the leakage current raises when the diameter increases. It is interesting to notice a strange shape on the drain current for devices with 98 nm diameter, suggesting a significant influence of trap interface under this condition [8].

B. Influence of the temperature on the subthreshold swing and I_{ON}/I_{OFF}

Figure 5 represents the temperature impact on I_{DS} x V_{GS} curves, plotting the results for diameters of 98 and 213 nm. The drain voltage was once more set to 0.9 V.

At first, it is evident that higher temperatures tend to deteriorate subthreshold slope. This effect may be explained by the difference between the I_{ON} and I_{OFF} temperature susceptibility. I_{OFF} is strongly affected by the increase in recombination rate and in thermal reverse leakage current. On the other hand, I_{ON} remains almost unaltered, since it is impacted only by the slight band-to-band tunneling variation caused by bandgap narrowing.

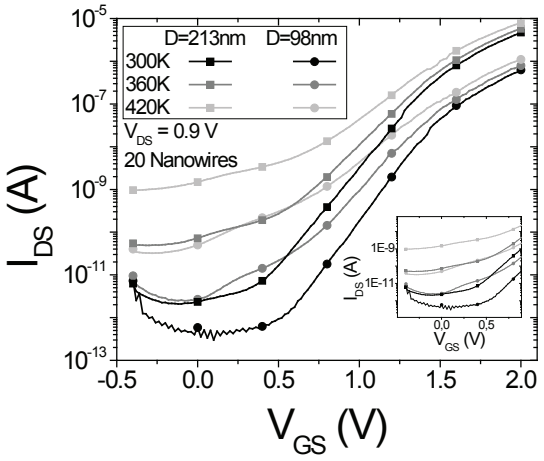

Figure 5. I_{DS} as a function of V_{GS} curves for devices with diameter of 98nm and 213nm varying the temperature from 300K to 420K.

Figure 6 presents the I_{ON}/I_{OFF} ratio for devices with 3 different diameter dimensions under temperature ranging from 300 to 420 K. All the devices revealed the same temperature dependence, with a lower current ratio for largest diameters. This behavior is due to the leakage current higher susceptibility to temperature variation and to the junction area. Besides, on-state region is less affected by the temperature, leading to a worse I_{ON}/I_{OFF} ratio and a consequent inferior performance for digital applications at high temperatures.

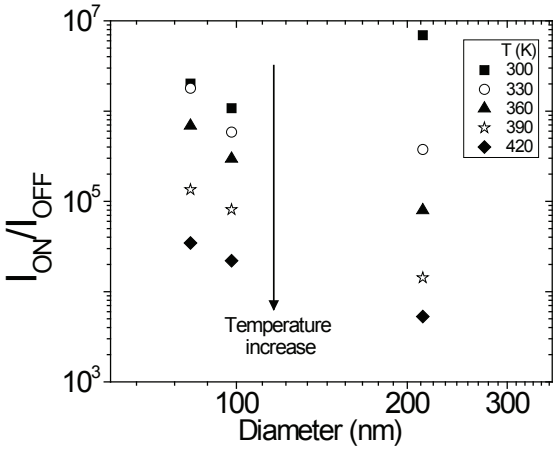

Figure 6. I_{ON}/I_{OFF} ratio as a function of nanowire diameter for different temperatures (from 300K to 420K).

It is quite interesting to observe that, in spite of the original objective focused on digital applications with a higher switching speed, Figure 7 illustrates that this devices may be considered even for analog designs. This conclusion was reached noticing the drain current plateau

obtained for higher values of drain voltages under three different gate voltage bias (0.9, 1.3 and 1.7 V).

On the topic of temperature influence, once more there is a different drain current susceptibility depending on the most relevant transport mechanism in each situation. Analyzing data presented in Figure 7, it is clear that the temperature impact is much more relevant for V_{GS} = 0.9 V, when TAT prevails. For V_{GS} = 1.3 V, the bigger influence of BTBT component makes the drain current less dependent. Finally, for V_{GS} = 1.7 V, the temperature influence get even smaller, since the band-to-band tunneling becomes the most important mechanism.

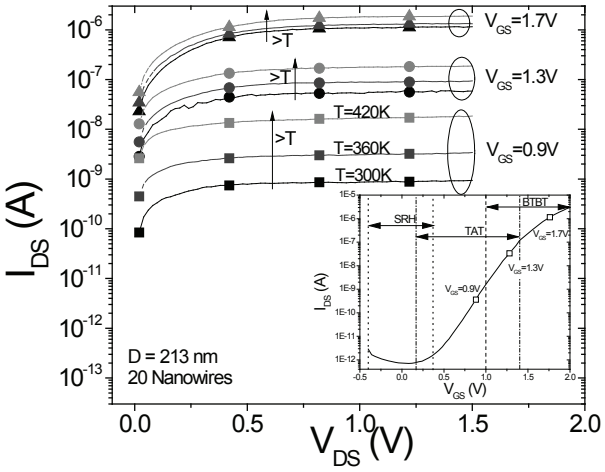

Figure 7. I_{DS} as a function of V_{DS} for different VGS bias and different temperatures.

As a final analysis, Figure 8 presents I_{DS} x V_{DS} curves for devices with different bias conditions and dimensions. It is possible to notice once more that the drain current raises when the diameter increases. Besides, there is a clear increase in the drain current for higher gate voltages, with an approximately constant shift for the 3 different analyzed dimensions.

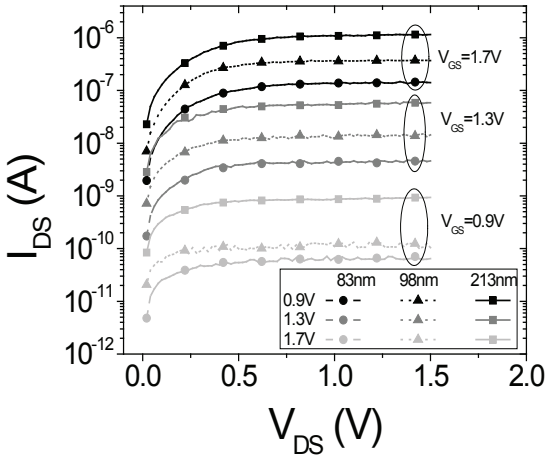

Figure 8. I_{DS} as a function of V_{DS} for different nanowire diameters and different gate bias at room temperature.

VI. CONCLUSION

This work presented a study of the temperature influence on nanowire tunneling field effect transistors. Curves reporting the drain current as a function of the gate voltage have been presented in linear and logarithmic scale, with the purpose of illustrating previously explained TFET working principle.

Although recently proposed structures have not reached theoretical limits yet, these curves still can be used to analyze the trends of this technology, which is expected to allow sub-60mV/dec values of subthreshold swing at room temperature.

This way, drain current curves for devices with different dimensions were analyzed in order to explain the effect of temperature variation on each transport mechanism.

Energy band diagrams were obtained from the simulations and could indicate the bias conditions under which the drain current was composed mainly by band-to-band tunneling, Shockley-Read-Hall recombination/ generation or trap-assisted tunneling.

After that, the experimental section presented results for devices with nanowire diameter ranging from 83 to 213 nm and exposed to temperature varying from 300 to 420 K. A quantitative analysis was performed based on the values of subthreshold slope and I_{ON}/I_{OFF} ratio. It was observed that higher temperatures causes a worst behavior in terms of these 2 parameters, since I_{OFF}, composed mainly by SRH, raised much more than I_{ON}, composed mainly by BTBT.

Considering all the results, it is possible to conclude that the advantages offered by nanowire tunneling field effect transistors are maximized for lower temperatures, even though the susceptibility to the temperature becomes more relevant. Therefore, this work highlighted the performance of TFET devices, proposed as a promising alternative for standard CMOS technology, with possible application in future digital and analog designs.

ACKNOWLEDGMENT

Felipe Neves Souza, Paula Ghedini Der Agopian and Joao Antonio Martino thank CNPq, CAPES and FAPESP for the financial support during the execution of this work. Part of the work has been performed within the frame of the CNPq-FWO Brazil-Flanders cooperation agreement and was supported by the IMEC's Logic Device Program and its core partners.

REFERENCES

[1] Daniele Leonelli, Anne Vandooren, Rita Rooyackers, Anne S. Verhulst, Stefan De Gendt, Marc M. Heyns and Guido Groeseneken, "*Performance Enhancement in Multi Gate Tunnel-*

ing Field Effect Transistors by Scaling the Fin-Width", Japanese Journal of Applied Physics, 49, issues 4, 2010, 04DC10.

[2] Costin Anghel, Andrei Vladimirescu and Amara Amara, "*Design of Silicon Double Gate Tunnel FETs with Ultra Low Ambipolar Currents"*, EUROSOI 2011, 1, 2011, pp. 74-73.

[3] Hsuan-Hsu Chen, Jyi-Tsong Lin, Kuan-Yu Lu, Yi-Chuen Eng and Po-Hsieh Lin, "A New Type of CMOS Inverter with Lubistor Load and TFET Driver for Sub-20 nm Technology Generation", Solid-State and Integrated Circuit Technology – ICSICT, 2010, pp. 93-95.

[4] Tejas Krishnamohan, Donghyun Kim, Shyam Raghunathan and Krishna Saraswat, "*Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and <60mV/dec Subthreshold Slope"*, IEDM Tech. Dig., 2008, pp. 1-3.

[5] Costin Anghel, Prathyusha Chilagani, Amara Amara and Andrei Vladimirescu, "*Tunnel field effect transistor with increased ON current, low-k spacer and high-k dielectric"*, Applied Physics Letters, 96, issue 12, 2010, 122104.

[6] Anne S. Verhulst, William G. Vandenberghe, Karen Maex and Guido Groeseneken, "*Tunnel field-effect transistor without gate-drain overlap"*, Applied Physics Letters, 91, issue 5, 2007, 053102.

[7] Sentaurus Device User guide, Version F-2011.09, September, 2011.

[8] F. S. Neves, P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys, *"Influence of interface trap density on vertical NW-TFETs with different source composition",* EuroSOI 2013, 1, 2013, pp. 1-2.

[9] M. D. V. Martino, P. G. D. Agopian, S. G. Santos Filho and J. A. Martino, "*Temperature Influence on Tunnel Field Effect Transistors (TFETs) with Low Ambipolar Currents"*, SBMicro 2011, v.39, 2011, pp. 77-84.

[10] M. D. V. Martino, P. G. D. Agopian, S. G. Santos Filho and J. A. Martino, "*Temperature Impact on Double Gate nTFET Ambipolar Behavior"*, ISDRS, 2011, pp. 1-2.