A CMOS Bandgap Reference Circuit with a Temperature Coefficient Adjustment Block

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ABSTRACT

A bandgap reference voltage source with a temperature coefficient adjustment block was proposed. The bandgap topology employs current summation and the circuit was designed through metaheuristic algorithms in a 0.35-mm CMOS technology. Simulations with typical parameters show that the designed circuit has temperature coefficient of 15 ppm/^{0}C, line regulation of 263 ppm/V, and current consumption of 2.71 uA in 1.0 V power supply. An additional 3-bit temperature adjustment block allowed keeping the temperature coefficient values lower than 26.6 ppm/^{0}C for 90% of the circuits, without interfering with the reference voltage output or line regulation values.

Index Terms: CMOS, analog circuits, voltage reference, bandgap, metaheuristics.

I. INTRODUCTION

Reference voltage sources are circuits that should provide a voltage signal that is precise and stable with variations of temperature, power supply, and also of process parameters. Being used in several analog and digital circuits, the demands for reference sources with lower temperature and power supply sensitivity, lower power supply voltage, lower power consumption, and smaller area are increasing every year.

The temperature stability can be attained through a weighted summation of a PTAT signal (Proportional to Absolute Temperature) and a CTAT signal (Complementary to Absolute Temperature). With convenient weights, the PTAT and CTAT signal variations will cancel one another, providing a temperature-stable voltage.

When the CTAT signal is the base-emitter voltage of a bipolar transistor (V_{BE}), or any signal derived from it, the reference voltage source is called a bandgap reference source or simply bandgap.

For more than forty years, bandgap circuits have been implemented by the sum of the V_{BE} voltage and a PTAT voltage [1]. In this case, when the weights are well adjusted, the obtained output voltage is nearly 1.21 V (the bandgap voltage of the silicon extrapolated to 300 K). Although such conventional bandgap reference sources provide satisfactory stability, the output voltage value is a problem for low voltage system implementations. To overcome this difficulty, in [2] was proposed a new bandgap circuit where the summation is performed on currents instead of voltages, and one of the currents is proportional to V_{BE}.

In [3] is proposed a circuit topology of a bandgap reference source that employs current summation. This topology has simple design characteristics, supports low voltage power supplies, and provides satisfactory stability, power consumption, and area.

In this work the bandgap topology of [3] is applied and the circuit design is done through metaheuristic algorithms [4]. Additionally, a temperature coefficient adjustment block is employed in order to improve the reference source characteristics.

The following sections present: the explanation of the implemented topology and its analysis, in section II; the design of the reference source through metaheuristic algorithms, in section III; the TCA block, analysis and design, in section IV; the complete circuit, the layout, final results, and comparison with circuits from literature, in section V; finally, the conclusion concerning the employed modifications and results, in section VI.

II. REFERENCE SOURCE TOPOLOGY AND ANALYSIS

In this section, it is initially presented a simplified circuit to explain the voltage source operation and extract its main equations. After that, it is presented the complete bandgap.

A. Simple topology

The circuit topology for the reference voltage source is presented at Fig. 1. In this circuit we can distinguish three blocks with different functions. The first block, composed by the transistors M_{P1}, M_{P2}, M_{N1}, and M_{N2} and the resistor R_3, is a current source responsible for generating the PTAT current I_1 [5]. In this block the use of operational amplifier is avoided in order to keep the power supply voltage low and the topology simpler. The second, composed by transistors M_{P3} and Q_1, is responsible for generating the CTAT voltage V_E. Finally, the last block, composed by transistor M_{P4} and resistors R_1 and R_2, is responsible for the weighted summation of the PTAT current I_4, a mirrored copy of I_1, and a CTAT current derived from V_E (I_5) to generate the temperature compensated output voltage.

To better understand the blocks and the circuit operation we will formulate the output voltage expression (V_R). When the transistors M_{N1} and M_{N2} are operating in weak inversion, the I_1 current of the degenerated current mirror can be expressed by the following equation ([5], [6]):

$$I_1(T) = \frac{1}{R_3}\frac{kT}{q}\ln(MN) \quad (1)$$

where *1:M* is the relation between the (W/L)s of the transistors M_{P1} and M_{P2} (Fig. 1); *1:N* is the relation between the (W/L)s of the transistors M_{N2} and M_{N1}; T is the absolute temperature; k is the Boltzmann's constant; and q is the magnitude of the electron electrical charge.

The output voltage can be found considering the summation of the currents towards the output node, V_R. The following expression results from the summation:

$$I_4 + \frac{V_E - V_R}{R_2} - \frac{V_R}{R_1} = 0$$

Combining the two earlier expressions, it is possible to isolate the output voltage V_R

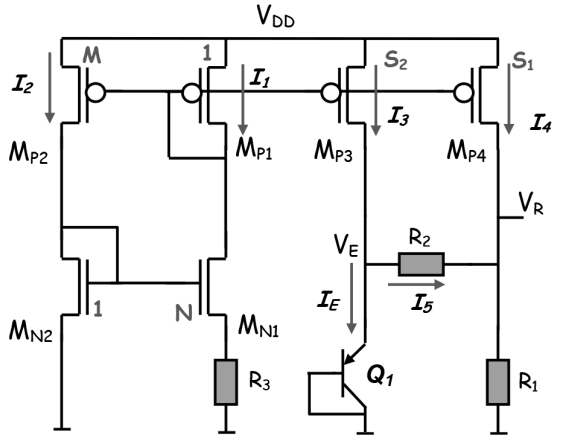

Figure 1. Simple reference voltage source topology [3]

$$V_R = \frac{R_1}{R_1+R_2}(V_E + I_4R_2) = \frac{R_1}{R_1+R_2}\left(V_E + S_1\frac{kT}{q}\frac{R_2}{R_3}\ln(MN)\right) \quad (2)$$

where *1:S_1* is the relation between the (W/L)s of the transistors M_{P1} and M_{P4} (Fig. 1).

This equation shows that the output voltage is proportional to the CTAT voltage V_E plus the PTAT voltage I_4R_2, although only currents have been summed. Notice that in this topology, for any temperature, the I_b current flowing through the bipolar transistors must be higher than zero. In any other case the circuit will not work properly.

A more complete expression for V_R can be derived if we substitute V_E, the Q_1 emitter-base voltage, by an expression presenting its temperature dependence [7]

$$V_E(T) = T\left(\frac{V_{EB}(T_R)}{T_R} - \frac{V_G(T_R)}{T_R} + \frac{V_G(T)}{T}\right) + (4-\eta)\frac{kT}{q}\ln\left(\frac{T_R}{T}\right) + \frac{kT}{q}\ln\left(\frac{I_C(T)}{I_C(T_R)}\right) \quad (3)$$

where T_R is a reference temperature, V_G is the bandgap voltage of the silicon, V_{EB} is the Q_1 emitter–base voltage, I_C is the Q_1 collector current, and η is a constant related with the mobility temperature dependence, which is proportional to $T^{-\eta}$.

Considering $I_3 >> I_5$, the approximation (where *1:S_2* is the relation between the (W/L)s of the transistors M_{P1} and M_{P3}) can be used to achieve a new expression for the output voltage, now assigning the temperature dependence. From (1), (2) and (3), we find:

$$V_R(T) = \frac{R_1}{R_1+R_2}\left(T\left(\frac{V_{EB}(T_R)}{T_R} - \frac{V_G(T_R)}{T_R} + \frac{V_G(T)}{T}\right) + (3-\eta)\frac{kT}{q}\ln\left(\frac{T_R}{T}\right) + S_1\frac{kT}{q}\frac{R_2}{R_3}\ln(MN)\right)$$

In this circuit, in pursuance of the temperature compensation at T_R, the values of R_2 and R_3 should be adjusted to attain the condition:

$$\left.\frac{\partial V_R(T)}{\partial T}\right|_{T=T_R} = 0$$

Also, to reach a desired output voltage, the value of R_1 should be adjusted.

Approximated relations can be derived if V_G is expressed as linearly dependent of temperature ($V_G = V_{G0} + \epsilon T$, where V_{G0} is the extrapolated bandgap voltage of silicon) [7]. In this case, the condition $\left.\frac{\partial V_R(T)}{\partial T}\right|_{T=T_R} = 0$ will demand that

$$S_1\frac{R_2}{R_3}\frac{KkT_R}{q}\ln(MN) = V_{G0} - V_{EB}(T_R) + (3-\eta)\frac{kT_R}{q} \approx V_{G0} - V_{EB}(T_R)$$

or, applying (1)

$$S_1 I_1(T_R) R_2 = V_{G0} - V_{EB}(T_R) \quad (4)$$

In consequence, the output voltage will be

$$V_R(T_R) = \frac{R_1}{R_1+R_2}\left(V_{G0} + (3-\eta)\frac{kT}{q}\right) \approx \frac{R_1}{R_1+R_2} V_{G0} \quad (5)$$

The equations (1), (4) and (5) provide relations for computing the values of the resistors R_1, R_2, and R_3, once the values of I_1, M, N, S_1, S_2, and V_R are chosen.

Since the total current consumption of the circuit is $I_1(1+ M + S_1 + S_2)$ as seen in Fig. 1, we can estimate the power consumption at temperature T_R using (4)

$$\text{power consump.} = \frac{V_{G0} - V_{EB}(T_R)}{R_2 S_1}(1 + M + S_2 + S_1) V_{DD}$$

The previous equation shows us that the value of R_2, and also of R_1 and R_3 since they all are correlated, determines the circuit's power consumption.

The dependence of the output voltage on the power supply voltage does not appear on the presented relations, but it can be derived with the help of (2). When channel modulations are taken into account, the PTAT current I_1 has, in fact, a slightly power supply dependence. Equation (2) shows that the output voltage is function of V_E and I_4 and they both are functions of I_1. Hence, the output voltage is also a function of the power supply. Considering that V_E is a logarithmic function of the emitter current and , the variation of the output voltage can be approximated by

$$\Delta V_R \cong \frac{R_1}{R_1+R_2}\left(\frac{kT}{q}\frac{\Delta I_3}{I_3} + \Delta I_4 R_2\right) = \frac{R_1}{R_1+R_2}\left(\frac{kT}{q} + S_1 I_1 R_2\right)\frac{\Delta I_1}{I_1}$$

where DV_R, ΔI_1, ΔI_3 and ΔI_4 are the output voltage and I_1, I_3, and I_4 current variations due to the power supply.

Using (4) and (5) with this later equation, we can derive the expression

$$\frac{\Delta V_R}{V_R} \cong \left(\frac{kT}{q}\frac{1}{V_{G0}} + \frac{V_{G0} - V_{EB}(T_R)}{V_{G0}}\right)\frac{\Delta I_1}{I_1} \cong 0.5\frac{\Delta I_1}{I_1}$$

According to this result, to attain small line regulation values it is necessary to keep the PTAT current as stable as possible.

B. Modified topology

With the purpose of improving the topology some modification done in [3] are also applied here. The modifications include the addition of cascode transistors to the current mirrors (M_{N3}, M_{P3}, M_{P8}, and M_{P9}, Fig. 2), in order to reduce the sensitivity of the output voltage with the power supply. Biasing circuits were also added to generate adequate gate voltage to the new transistors and to ensure that the current mirrors operate properly with low voltages (M_{N5} and M_{P4}; M_{N4} and M_{P5}, Fig. 2) [8]. The relations derived on the last section are still valid for this new circuit.

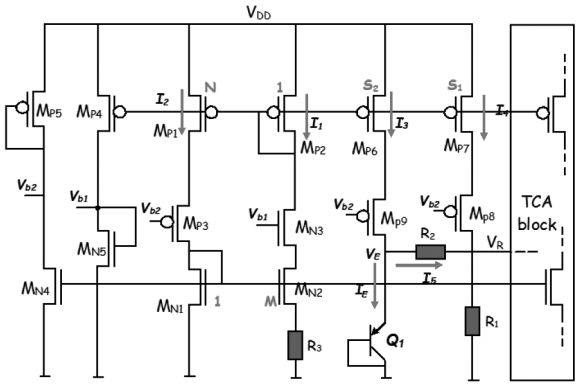

Figure 2. Modified reference voltage source topology. The Temperature Coefficient Adjustment block (TCA block) position is also indicated

III. REFERENCE SOURCE DESIGN AND SIMULATION RESULTS

A. Circuit design

The modified topology was designed in the AMS (AustriaMicroSystems) 0.35-mm CMOS technology (with four metal levels and a high resistive polysilicon layer). In this technology, the typical values of V_{TH0} are 0.5 V for NMOS transistor and -0.7 V for PMOS transistor, and the worst speed values of V_{TH0} are 0.6 V and -0.8 V.

Circuit devices dimensions were determined by a metaheuristic algorithm [4]. This algorithm was the genetic algorithm (GA) which has been executed 10 times. For each execution, it was employed 8 populations of 50 individuals and processed 200 generations.

The GA fitness function was based on electrical simulation results. From the simulations were found the output voltage, the temperature coefficient, the line regulation, and the power consumption,. The circuit score was computed from these values and an area estimation. The simulations were run on ELDO simulator with the technology typical model (BSIM3v3).

The target of the GA was a circuit with reference voltage of 0.5 V (±10% of error), temperature coefficient lower than 30 ppm/ºC for -10ºC to 90ºC, line regulation lower than 350 ppm/V for power supply from 1.0 V to 2.5 V, the lowest current consumption, and the smallest area. Fig. 3 depicts the GA optimization process.

The dimensions of the best circuit among those found in the GA executions, as well the dimension limits used in the GA, are presented in the TABLE I.

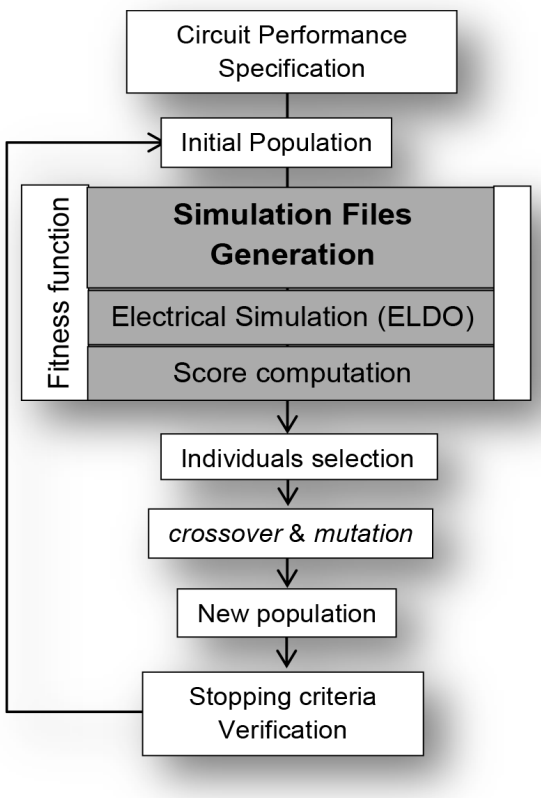

Figure 3. Schematic of the circuit design optimization

Table I. Dimensions Of The Designed Circuit Determined By A Metaheuristic Algorithm (Ga) And Their Value Range

Parameter	*Width (W)* (µm)	*GA W range [min, max]* (µm)	*Length (L)* (µm)	*GA L range [min,max]* (µm)
M_{P1}	260 (N=3)	[3, 300]	5.7	[1, 20]
M_{P2}	87	[1, 100]	5.7	[1, 20]
M_{P3}	260 (N=3)	[3, 300]	1.6	[1, 20]
M_{P4}	71	[1, 100]	5.7	[1, 20]
M_{P5}	4.6	[1, 30]	29.5	[1, 30]
M_{P6}	174 (S_2[b] =2)	[2, 200]	5.7	[1, 20]
M_{P7}	435 (S_1[b]=5)	[5, 500]	5.7	[1, 20]
M_{P8}	435 (S_1[b]=5)	[5, 500]	1.6	[1, 20]
M_{P9}	174 (S_2[b]=2)	[2, 200]	1.6	[1, 20]
M_{N1}	121	[1, 200]	12.5	[1, 20]
M_{N2}	121 (M=1)	[1, 200]	12.5	[1, 20]
M_{N3}	121 (M=1)	[1, 200]	3.9	[1, 20]
M_{N4}	27.3	[1, 40]	12.5	[1, 20]
M_{N5}	3.4	[1, 40]	28.2	[1, 30]
R_1[a]	4.0	[4, 4]	1408	[700, 1600]
R_2[a]	4.0	[4, 4]	1585	[700, 1600]
R_3[a]	4.0	[4, 4]	454	[300, 1000]

a. The resistors R_1, R_2 and R_3 have approximately 422.4 kΩ, 475.6 kΩ, and 136.2 kΩ. Their GA range were approximately [210 kΩ, 480 kΩ], [210 kΩ, 480 kΩ], and [90 kΩ, 300 kΩ], respectively.
b. The GA range for these parameters was an integer between 1 and 6.

B. Reference source results

ELDO simulations with the typical model were performed in the designed circuit to obtain the TC, RL and power consumption. To calculate the TC, a temperature range from -10ºC to 90ºC was used and to calculate the LR, a power supply range from 1.0 V to 2.5 V.

In Fig. 4 is shown the graph of the Output Voltage versus Temperature for seven different power supply voltages (from 1.0 V to 2.5 V with 0.25 V increment). Among these curves, the best TC achieved was 15 ppm/ºC for 1.0 V and the worst was 16 ppm/ºC for 2.5 V.

In Fig. 5 is shown the graph of the Output Voltage versus Power Supply Voltage for ten different temperatures (from -10ºC to 90ºC with 10ºC increment). Among these curves, the best RL achieved was 200 ppm/V for 30ºC and the worst was 400 ppm/V for -10ºC. Notice that the curves of Fig. 5 behave similarly due to the low circuit LR value, which ensures a TC value almost independent of the power supply.

In Fig.6 is shown the Output Voltage versus Power Supply to verify the circuit operation. A 2.76 µA current consumption at 27ºC was achieved.

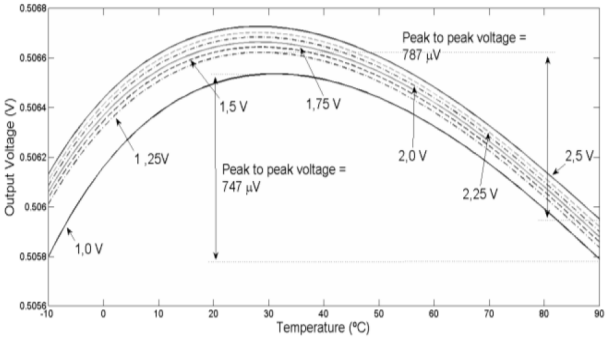

Figure 4. Curves of the Output Voltage (V) versus Temperature (ºC) for different power supply voltages (from -10 V to 90 V with increments of 10 ºC) for the typical model

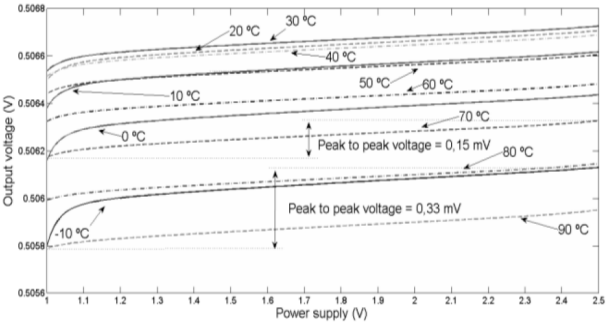

Figure 5. Curves of the Output Voltage (V) versus Power Supply Voltage (V) for different temperatures (from 1.0 V to 2.5 V with increments of 0.25 V) fot the typical model

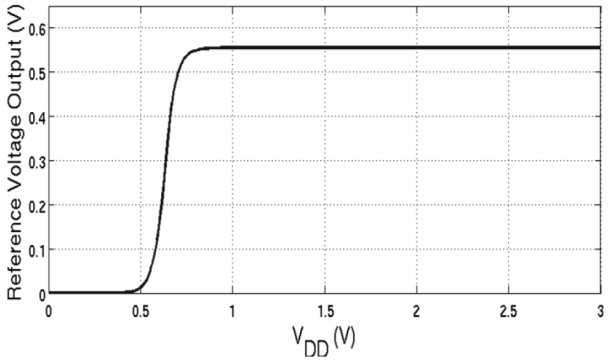

Figure 6. Graph of the Output Voltage (V) versus Power Supply Voltage V_{DD} (V)

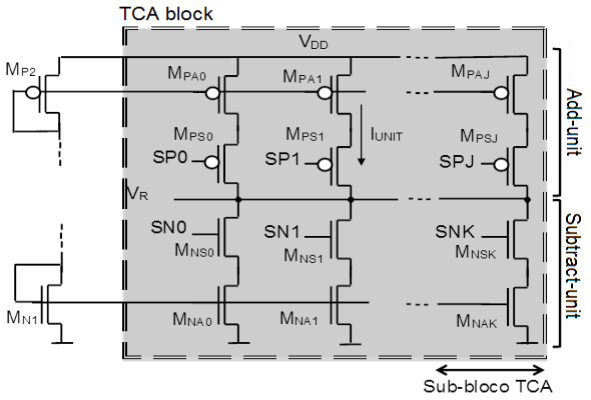

Figure 7. Topology of the Temperature Coefficient Adjustment block (TCA block), responsible for adding or subtracting current from the output V_R

IV. TEMPERATURE COEFFICIENT ADJUSTMENT BLOCK (TCA)

The temperature coefficient minimization depends on some relations among the circuit device parameters, relations pointed out by equation (4). Since not all implemented circuits will keep the correct relations, the TC parameter will suffer variations from circuit to circuit. An extra block has been added to the reference source to improve the TC and decrease the number of circuits being rejected due to unsatisfactory TC value. This block, named Temperature Coefficient Adjustment block, or just TCA block, reduces the TC by controlled addition/subtraction of adjustment currents toward the output node V_R.

The TCA block basically changes the PTAT current in the weighted summation, allowing a fine adjustment of the temperature coefficient. The final result can be interpreted as an addition of an extra term α in (4),

$$(S_1 + \alpha)I_1(T_R)R_2 = V_{G0} - V_{EB}(T_R)$$

This term compensates any discrepancies between the real fabricated values of S_1 and R_2 and the values that satisfy (4), minimizing the TC.

In the TCA block, the adjustment current, αI_1, will vary from I_{MIM} to I_{MAX}, values empirically determined, in (2b-1)-equally spaced steps. Figure 7 depicts the TCA block (its connection with the reference source is depicted in Fig. 2). It is composed by (b-1) Add-current units and b Subtract-current units. The Add-unit is composed by a mirror transistor, M_{PAi}, and a switch transistor, M_{PSi}, which is responsible for turning the current on or off. The Subtract-unit is composed by a mirror transistor, M_{NAi}, and a switch transistor, M_{NSi}.

To control the adjustment current value an additional circuit is designed. This circuit, based on control input values, will select which current-units will be on or off. TCA blocks with 2, 4, 8, 16 or 32 adjustment currents will ask for 1, 2, 3, 4 or 5 control inputs, respectively, and will be called 1, 2, 3, 4, or 5-bits TCA.

In the case of TCA block application, for each fabricated circuit the control inputs should be configured to guarantee the minimum TC. Actually, the process of deciding the best TCA configuration could be cumbersome.

A. Determination of I_{MIN}, I_{MAX} and the number adjustment currents (2b)

To determine the I_{MIN} and I_{MAX} values an ideal 6-bit TCA block, with the α value varying from -1.5 to 1.5, was simulated with the designed voltage source. A Monte Carlo run was performed and the TC values were investigated for each sample. It was observed that for almost all samples, the TC value was minimized when the α value was at the interval [0.14, 0.14]. In consequence, the chosen α_{MIN} and α_{MAX} values were -0.14 and 0.14, respectively. Since the value of PTAT current (I_1) is 0.7 μA at 27ºC, the equivalent adjustment current should vary from -0.1 to 0.1 μA.

In order to find the number of bits necessary to the TCA block, Fig. 8 was built through Monte Carlo simulations and TC measurements from -10 ºC to 90 ºC with power supply of 1.0 V. The graphic shows the

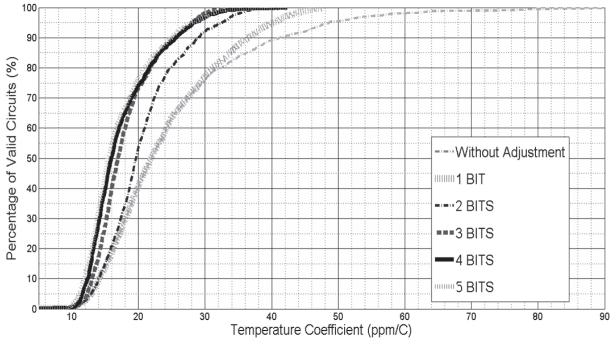

Figure 8. Percentage of valid circuits agains temperature coefficient (ppm/ºC). It is shown circuits without TCAt and with 1, 2, 3, 4 and 5-bits TCA

percentage of valid circuits versus the maximum TC accepted (ppm/ºC). Valid circuits are the circuits with TC value lower than the x axis value. The results of reference sources without and with the TCA block (with 1, 2, 3, 4 and 5 bits) are drawn.

As expected, the augmentation of the number of bits in the TCA block increases the percentage of valid circuits for any TC specification, but the improvement is insignificant for elevated number of bits. The number of bits increase, on the other hand, will cause the increase of the layout complexity, the area, the power consumption, and of the effort to find the best TCA configuration for the fabricated circuits.

Based on the Fig. 8 and the previous paragraph comments, 3-bits TCA were used.

B. Design of the TCA block

A 3-bit TCA block needs 3 Add-units and 4 Subtract-units. In order to extract or add currents from -0.1 to 0.1 μA the chosen transistor dimensions are shown in TABLE II.

Three control inputs, S_0, S_1, and S_2, are used to manage the switch transistors M_{PSi} and M_{NSi}. A digital block was developed to decode the control input signals to the 7 transistor gate voltages, according to TABLE III.

To confirm the TCA block operation improvement, the Fig. 9 is presented. The histogram of the figure depicts the Number of Circuits versus TC value for implementations without and with the 3-bit TCA block. The histogram was obtained with a 1000-run Monte Carlo simulation and 1.0 V power supply. The TC histogram of the circuit without TCA has 24 ppm/ºC mean and 10-ppm/ºC standard deviation, while the histogram of the circuit with TCA block has 18 ppm/ºC mean and 4.8-ppm/V standard deviation (after the TCA correct configuration to be adjusted). The improvement can be observed in both statistics, the mean and the standard deviation

Table II. Dimensions of The Projected 3-Bit Tca Block

Parameter	Width (W) (µm)	Length (L) (µm)
M_{PAi}	4.5	10.0
M_{NAi}	3.9	6.8
M_{PSi}	4.5	0.35
M_{NSi}	3.9	0.35

Table III. Table To Decode The 3 Control Inputs Into 7 Switch Gate Vontages Of The Tca Block

Control input (V_{DD})			Switches of the TCA block (V_{DD})						
S_2	S_1	S_0	M_{PS2}	M_{PS1}	M_{PS0}	M_{NS3}	M_{NS2}	M_{NS1}	M_{NS0}
0	0	0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
0	0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	0
0	1.0	0	1.0	1.0	1.0	1.0	1.0	0	0
0	1.0	1.0	1.0	1.0	1.0	1.0	0	0	0
1.0	0	0	1.0	1.0	1.0	0	0	0	0
1.0	0	1.0	1.0	1.0	0	0	0	0	0
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1.0	1.0	1.0	0	0	0	0	0	0	0

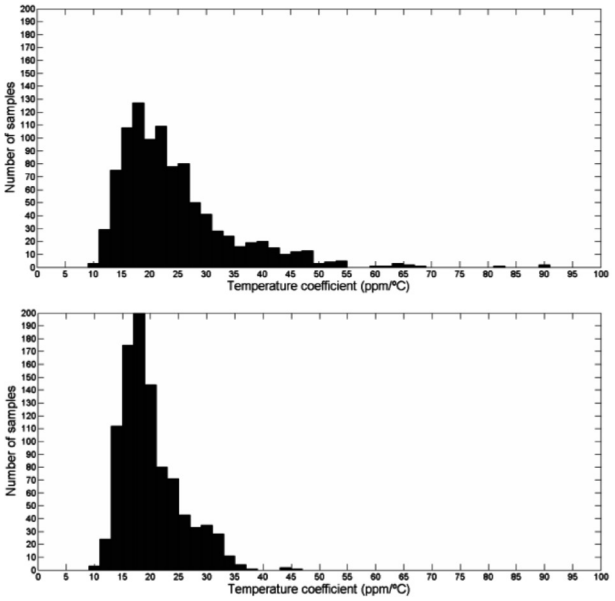

Figure 9. Histogram of the Temperature Coefficient (ppm/ºC) of the circuit without (on the top) and with (on the bottom) the 3-bit TCA block, for 1000 samples Monte Carlo simulation

C. Influence of the TCA on the reference voltage and line regulation

Since the TCA block alters the current flowing through the resistor R_1, it is important to verify the effect of this block over the LR and the reference voltage values.

The histogram of Fig. 10 depicts the Number of Circuits versus RL value for implementations without and with the 3-bit TCA block. The histogram was obtained with a 5000-run Monte Carlo simulation at 27ºC temperature. The RL histogram of the circuit without TCA block has 429 ppm/V mean and 208 ppm/V standard deviation, while the RL histogram of the circuit with TCA block has 428 ppm/V mean and 200 ppm/V standard deviation (after the TCA configuration to be adjusted). The influence of the TCA block on RL is irrelevant.

The histogram of Fig. 11 depicts the Number of Circuits versus Output Voltage for implementations without and with a 3-bit TCA block. The histogram was obtained with a 1000-run Monte Carlo simulation and 1.0- V power supply. The output voltage histograms of the circuit without and with the TCA block have the same 0.55 V mean and 7.0 mV standard de-

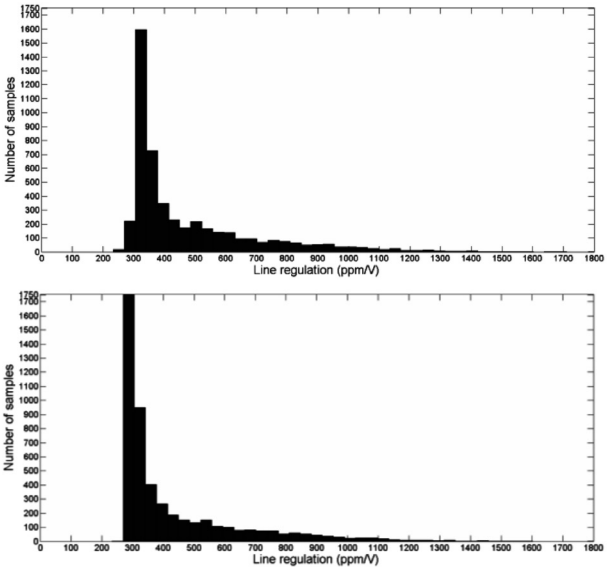

Figure 10. Histogram of the Line Regulation (ppm/V) of the circuit without (on the top) and with (on the bottom) the 3-bit TCA block, for 5000 samples

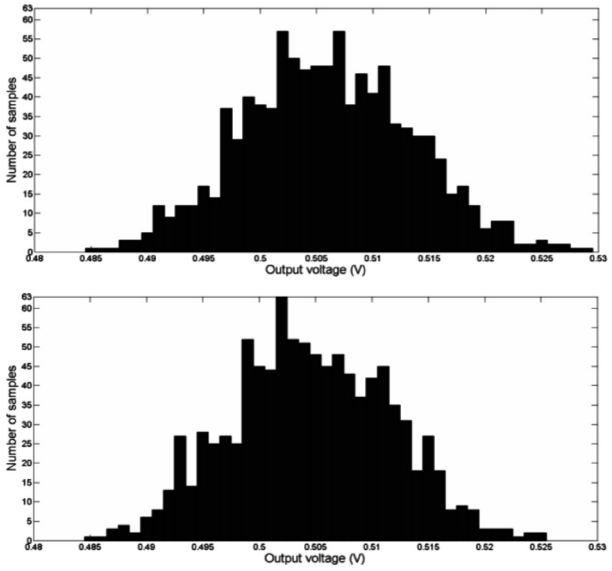

Figure 11. Histogram of the Output Voltage (V) of the circuit withou (on the top) and with (on the bottom) the 3-bit TCA block, for 1000 samples

viation (after the TCA configuration to be adjusted). The small influence of the TCA block on the reference voltage is explained by the fact that the adjustment current is much lower than the current I_4.

D. Choosing the TCA block configuration on a real circuit

With the fabrication of the circuit, the TCA blocks should be configured to achieve the minimal TC. One method for this is to test each possible configuration in several temperatures, measuring the output voltage, and, after that, to pick up the configuration with the minimum TC. Despite of the correctness of this method, it would require a long procedure time for real circuits. A simplified method is proposed: to test the TCA configurations only for the extreme temperatures, -10ºC and 90ºC for instance, and to pick up the configuration with the smallest output voltage difference for the two points.

The graphic of Fig. 12 shows us the percentage of valid circuits versus the maximum TC accepted for two TCA block configurations: in one case, 100 temperature points are measured to compute the TC value, and the adopted configuration is the one which gives the smaller TC (100-point method); in the other case, it is applied the simplified configuration method. We can see that the simplified method will reach almost the same results of the troublesome 100-point method. Evidently the simplified method is advantageous.

V. COMPLETE CIRCUIT AND RESULTS

A. Start-up circuit

The current source used in this work needs a start-up circuit in order to initiate its operation. Due to the applied cascode transistors, M_{P3} and M_{N3}, the start-up should be more complex than start-up circuits applied in conventional current sources [9, 10, 11, 12]. Shown in the Fig. 13, the start-up circuit applied is for-

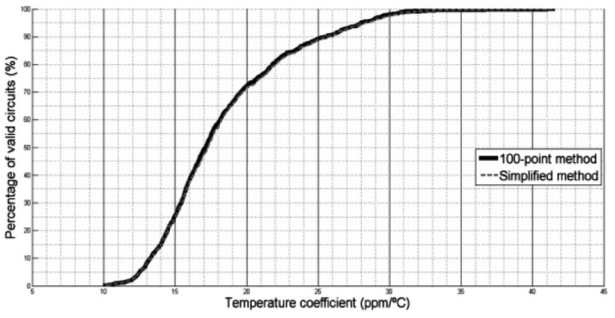

Figure 12. Percentage of valid circuits versus Temperature Coefficient (ppm/ºC) for the 100-point method and the simplified method

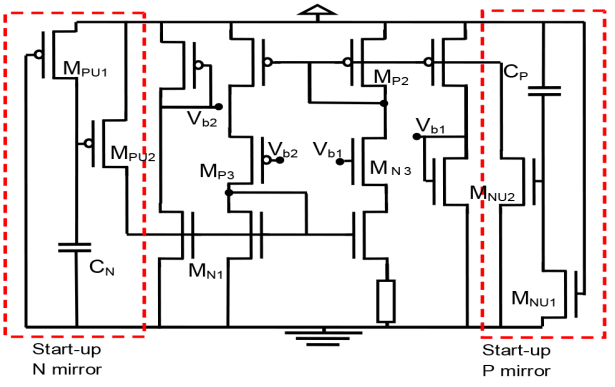

Figure 13. Start-up circuit for the bandgap

med by two parts working in parallel: one part, M_{PU1}, M_{PU2}, and C_N, is responsible for starting the NMOS current mirror; the other, M_{NU1}, M_{NU2}, and C_p, is responsible for starting the PMOS current mirror.

B. Layout and results

The layout of the circuit is show in Fig. 14. Simulations were performed using the typical, worst-speed, and worst-power model to analyze the TC, RL, power consumption, and start-up time of the complete circuit (after the TCA configuration to be adjusted). The final circuit achieved a 15 ppm/ºC TC (1,0 V power supply), 263 ppm/V LR (27ºC), and 2.73 mW (1,0 V power supply and 27ºC) with typical model; 36 ppm/ºC TC (1,0 V), 967 ppm/V LR (27ºC), and 2.24 mW (1,0 V and 27ºC) with the worst speed model; and 89 ppm/ºC TC (1,0 V), 343 ppm/V LR (27ºC), and 3.53 mW (1,0 V and 27ºC) with the worst-power model, as shown in Fig. 15, Fig.16, and Fig. 17.

A 1000-sample transient Monte Carlo simulation was done to find the start-up time, as shown in Fig.18. The worst case start-up time takes 0.77 s.

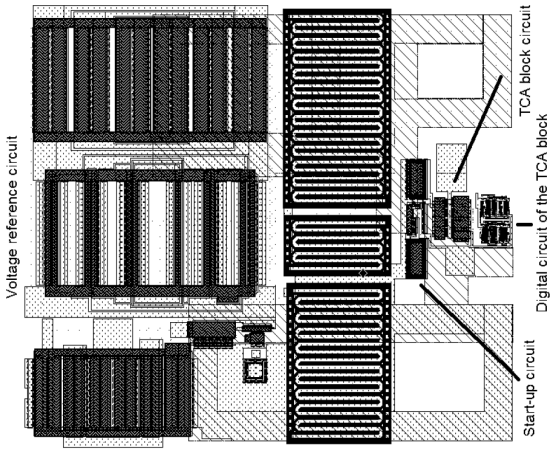

Figure 14. Layout of the circuit (345 µm x 332 µm)

C. Comparison with circuits from literature

The overall results of the designed circuit are shown in TABLE IV, as well as the results for some circuits available in the literature.

The proposed circuit has a TC comparable to the others from literature, a low LR under a low power supply, and a low current consumption, which can be reduced if increased the resistor's dimensions. Notice that the only circuit that presents a LR lower than 260 ppm/ºC is the circuit proposed in [10]. This circuit is implemented with voltage summation and, in consequence, the generated reference voltage does not depend directly on a PTAT current variable with the power supply.

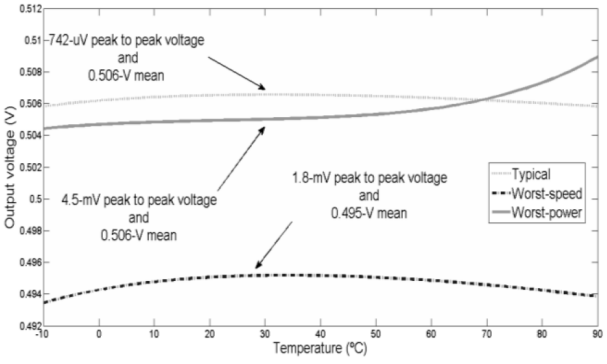

Figure 15. Curve of Output Voltage (V) versus Temperature (ºC) for the typical, worst-speed, and worst-power models

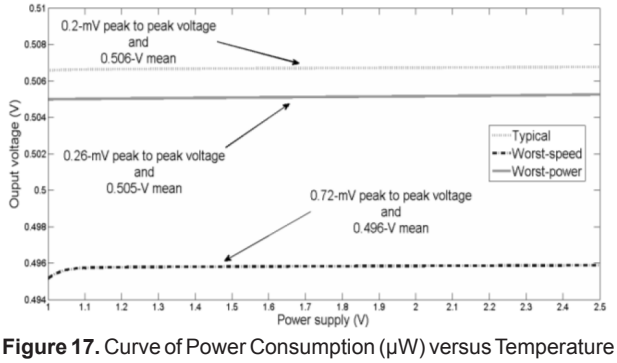

Figure 17. Curve of Power Consumption (µW) versus Temperature (ºC) for the typical, worst-speed, and worst-power models

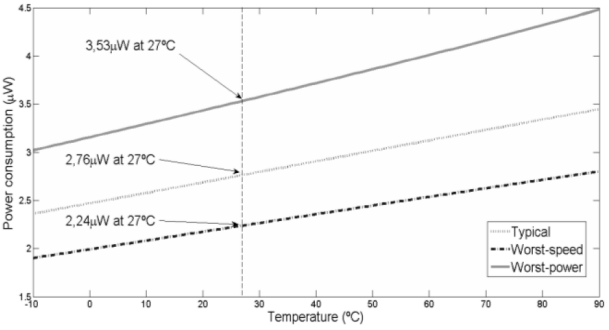

Figure 16. Curve of Output Voltage (V) versus Power Supply (ºC) for the typical, worst-speed, and worst-power models

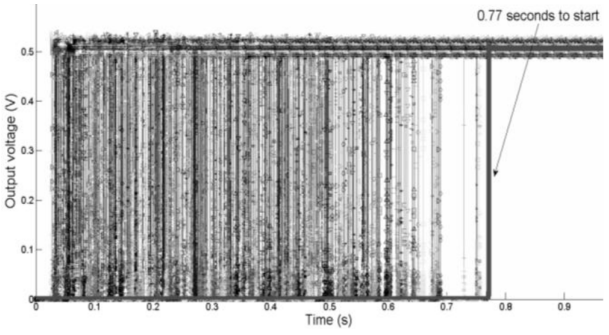

Figure 18. Curve of output voltage (V) against time (s) of 1000 samples of Monte Carlo simulation

Table IV. Characteristics of The Designed Reference Source Circuit and of Some Literature Circuits

Reference	This work	[3]	[13]	[9]	[10]	[11]	[12]	[14]	[15]
CMOS Process	0.35-mm	0.35-mm	0.25-mm	0.35-mm	0.35-mm	0.4-mm	0.6-mm	0.35-mm	0.18-mm
Temperature Range (ºC)	-10 to 90	-10 to 90	0 to 100	-25 to 100	-20 to 80	27 to 125	0 to 100	0 to 80	-20 to 120
Reference Voltage (V)	0.55	0.51	0.536	0.176	0.745	0.518	0.309	0.168	0.221
Current Consumption (µA)	2.71 (40 ºC)	6.17 (40 ºC)	50	2.7 (27 ºC)	0,2 (27 ºC)	2.2	9.7	2.4 (80º)	3.9 (27ºC)
Temperature Coefficient (ppm/ºC)	27[a]	21	19.5	38	7.0	117	36.9	25	194
Line Regulation (ppm/V)	263 (1 to 2.5 V, 40ºC)	3.3k (1 to 2.5 V, 27ºC)	-	23k	20	2145	830 (25 ºC)	9524	9050
Minimum Power Supply (V)	1	0.8 (|VT0|=0.5V)	0.9	0.94	1.4	2.2	1.4	1.5	0.9
Area (mm^2)	0.11	0.042	0.108	0.0223	0.052	0.1	0.055	0.08	0.0238

a. With a 3-bit temperature coefficient adjustment block for 90% of the circuits

VI. CONCLUSIONS

In this work, the topology of [3] is applied and the design is done through a metaheuristic algorithm, incorporating a temperature coefficient adjustment block (TCA block). This block proved to be an important feature to obtain a reduced TC, the main goal of reference source circuits. The block also does not degrade the voltage reference or the RL of the circuit. The applied 3-bit TCA block allowed a maximum TC of 26.6 ppm/ºC for 90% of the circuits, with an insignificant current increase. Additionally, a simple method for TCA configuration was proposed.

The final achievement is a circuit with 0.55 V reference voltage, 15 ppm/ºC average TC, 263 ppm/V average LR, and 2.71 μA average current consumption with power supply of 1,0 V on a 0.35-μm CMOS technology. Such good results were due, in part, to the GA algorithm employed in the design, which has proved to be a powerful tool for designs.

REFERENCES

[1] K.E. Kuijk, “A Precision Reference Voltage Source,” IEEE J. Solid State Circuits, vol. 8, pp. 222-226, June 1973.

[2] H. Banba, H.Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, “A CMOS bandgap beference circuit with sub-1-V operation,” IEEE J. Solid State Circuits, vol. 34, pp. 670-674, May 1999.

[3] J. Navarro and E. Ishibe, “A simple CMOS bandgap reference circuit with sub 1-V operation.” In: proc International Symposium on Circuits and Systems, Rio de Janeiro, pp. 2289-2292, May 2011.

[4] E.-G Talbi, “Metaheuristics From Design to Implementation,“ Hoboken: John Wiley & Sons, Inc. 2009.

[5] E. Vittoz and J. Fellrath, “CMOS Analog Integrated Circuits Based on Weak Inversion Operation,“ IEEE J. Solid-State Circuits, vol. 12, pp. 224-231, June 1977.

[6] G.C. Tzanateas, C.A.T. Salama, and Y.P. Tsividis, “A CMOS bandgap voltage reference,” IEEE J. Solid State Circuits, vol. 14, pp. 655-657, June 1979.

[7] Y.P. Tsividis, “Accurate analysis of temperature effects in Ic/VBE characteristics with application to bandgap reference sources,” IEEE J. Solid State Circuits, vol. 15, pp. 1076-1084, Dec. 1980.

[8] S. Yan and E. Sánchez-Sinencio, “Low voltage analog circuit design techniques: a tutorial,” IEICE Trans. Fundamentals, vol. E83-A, pp. 179-196, Feb. 2000.

[9] J. Mateus, E. Roa, H. Hernandez, and W.V. Noije, “A 2.7uA Sub1-V Voltage Reference,” In: Proc. Symposium on Integrated Circuits and Systems Desing, Gramado, Brazil, pp. 81-84, September 1–4, 2000.

[10] K. Ueno, T. Hirose, T. Asai, and T. Amemiya, “A 300 nW, 15 ppm/ºC, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs,“ IEEE J. Solid-State Circuits, vol. 44, pp. 2047-2054, July 2009.

[11] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, “A CMOS Bandgap Reference Circuit with Sub-1-V Operation. “ IEEE J. Solid-State Circuits, vol. 34, pp. 670-674, May 1999.

[12] K.N. Leung and P.K. Mok, “A CMOS Voltage Reference Based on Weighted ΔVGS for CMOS Low-Dropout Linear Regulators,” IEEE J. Solid-State Circuits, vol. 38, pp. 146-150, Jan. 2003.

[13] M.-D. Ker and J.-S. Chen, “New curvature-compensation technique for CMOS bandgap reference with sub-1-V operation,” IEEE Trans. Circuits Syst. II, Expr. Briefs, vol. 53, pp. 667-671, Aug. 2006.

[14] G.D. Vita and G. Iannaccone, “An Ultra-Low-Power, Temperature Compensated Voltage Reference Generator.” In. Proc. IEEE 2005 Custom Integrated Circuits Conference (pp. 751-754). San Jose, CA, USA: IEEE.

[15] P.-H. Huang, H. Lin, and Y.-T. Lin, “A Simple Subthreshold CMOS Voltage Reference Circuit with Channel- Length Modulation Compensation,” IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 53, pp. 882-885, Sep. 2006.