Observation of the Two-Sided Read Window on UTBOX SOI 1T-DRAM: Measurement Setup, Numerical and Empirical Results

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ABSTRACT

This paper presents the concept and implementation of a complete 1T-DRAM memory characterization setup and analyzes the read windows of decananometer UTBOX SOI 1T-DRAM memory devices focusing on the mechanisms involved as a function of the applied gate voltage during the read operation. It will be demonstrated both experimentally and by simulation that a novel two-sided read window is possible where the two main effects present, GIDL and parasitic BJT, can be effectively accounted for in two different zones.

Index Terms:1T-FBRAM; UTBOX SOI; read window; sense margin;

I. INTRODUCTION

1T-DRAM or single transistor dynamic random access memory is a device capable of retaining information in a single transistor without the need of an additional capacitor. Since the introduction of 1T-DRAM on a Silicon-on-Sapphire substrate by Fujitsu in 1978 [1], the technology has not been the focus of many studies until the last decade [2], when single transistor memories regained steam due to, among other factors, the difficulty of creating small and well-performing capacitors for conventional DRAM [3] and the opportunity of boosting a smaller footprint per bit, as well as having a single process integrating both memory and logic.

In that sense, if 1T-DRAM is to replace the conventional 1T/1C DRAM, the bit tail of the retention time distribution should be higher than 64ms [4]. Due to the dynamic nature of this type of memory, after some period of time it will revert to its most stable state and erase the information previously stored. Hence, it is vital to optimize this parameter and make sure that all the cells inside a memory achieve or exceed this requirement. 1T-DRAM is known for presenting some challenges due to the long-tail distribution of retention times in a chip [5]. In order to improve retention time and the overall performance of the device, the first step is the correct identification of the best biasing points for a specific type of device. Four different states must be defined:

• Write "1": Stores charge in the floating body (FB) of the SOI transistor (when the FB is charged, the memory is said to be in the "1" state). This can be achieved either through GIDL or Impact Ionization.

• Write "0": Erases all the charge previously stored in the floating body (the memory is in the "0" state) by forcing all charge out of the region.

• Read: Enables a sensing circuit to measure the source/drain current and decide if the transistor is in the "0" (I_0) or "1" (I_1) state based on a threshold. In this paper, this is achieved by evaluation the triggering or not of the parasitic BJT.

• Hold: Keeps the charges (or lack thereof) stored in the floating body constant while the memory cell is not being addressed.

These four states can be measured with the setup presented in Figure 1 and can be seen in Figure 2.

Although many authors have characterized either by simulation or experimentally the read windows of their respective devices [6-8], very little has been published about the existence of a two-sided IT-DRAM read window. As will be explained further, when subjected to a special biasing condition, the studied UTBOX SOI 1T-DRAM devices can present a two-sided read window with a clear separation between the two read-enabling mechanisms: BJT and GIDL/BJT.



Figure 1. Experimental setup and connections



Figure 2. Example of program and read waveforms as measured on a UTBOX SOI 1T-DRAM device on the memory testing setup of the LSI/USP

II. EXPERIMENTAL SETUP

In order to perform the aforementioned measurements, it is necessary to change the gate and drain voltage levels while measuring the current flowing through the source. It is also important to establish a constant and reliable back-gate bias. In that sense, three different pieces of equipment are necessary, as shown below in Figure 1:

A. Signal Integrity

As the rising and falling edges of the signals can easily be faster than 10ns, some special precautions must be taken in order to preserve the waveform values and shield the signals from interference.

First of all, the rapidly changing signals should be transferred through low-loss 50Ω coaxial cables as seen in Figure 1. As the arbitrary waveform generator (DG1022 in Figure 1) has 50Ω outputs, this assures impedance matching at the source. One might note that the transistor at the end of the coaxial connection is not impedance matched; however, this is not a problem since the current flowing through the transistor is very small and, therefore, this branch of the coaxial cable can be modelled as an open end. This will obviously lead to a reflection, but it will only affect the signal source, which will promptly absorb the reflection completely. At the transistor, one gets a perfect signal with unaltered rising and falling waveforms.

Secondly, signals should not have long outside connections of coaxial cables. As the waveforms comprise fast rise and fall times, any exposed wire can lead to unwanted impedance mismatches, parasitic capacitance and crosstalk.

Finally, in order to measure the current flowing through the drain-source of the transistor (from 10 to 300μ A for the transistors under test) a 50Ω termination resistor internal to one of the channels of the oscilloscope is used. Voltage (V) is measured on this channels and drain current (I_{DS}) can be easily obtained from:

$$I_{\rm DS} = V/50 \tag{1}$$

Using the termination resistor from the oscilloscope greatly improves the Signal to Noise Ratio (SNR) as the signal is fed directly to the oscilloscope through coaxial cables.

It is worth noting that a custom PCB was built in order to facilitate the interconnections between the BNC-terminated coaxial cables and the microprobes as well as to tie all shielding to ground together close to the Device Under Test (DUT). As the rise and fall times of the signals applied to the DUT are very small, they are susceptible to ground bounce and crosstalk. Tying the grounds together close to the DUT improves the signal quality significantly and is vital for achieving reliable and accurate readings.

B. Measurement Example

As it can be seen from Figure 3, the measured device behaves as expected and has a sense margin (SM), defined as SM = I_1 - I_0 [9], of approximately 70 μ A for a gate voltage of -1.5V during the read pulse. In order to determine the maximum sense margin, one needs to reproduce the waveforms shown in Figure 2 for a series of different gate voltages (V_{Gread}). Once this process is complete, it is possible to plot I_0 and I_1 as a function of V_{Gread} . The V_G region on this plot where the sense margin is greater than 50% of the maximum sense margin is known as the read window. One can use the SOI transistor as a fully functional 1T-DRAM memory within this window.

III. EXPERIMENTAL RESULTS

Wafers containing nMOSFET transistors were manufactured on SOI substrates with a 20nm

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Table I. Sequence Of States And Biases For Measurement								
Time [ns]	V _G [V]	V _D [V]	V _B [V]	State				
10	0.5	1.8	2.8	Write "1"				
10	0	0.5	2.8	Write "0"				
10	-2.9 : -0.5	1.8	2.8	Read				
-	-2	0	2.8	Hold				



Figure 3. Measured read window with its two regions clearly visible

thick silicon film and 10nm Ultra-Thin Buried Oxide (UTBOX). Gate electrodes consisting of 5nm plasma enhanced atomic layer deposition (PEALD) TiN capped with 100nm poly-Si were deposited on a 5nm thick SiO₂ layer. The source and drain regions were subjected to Selective Epitaxial Growth (SEG) in a dopant-rich environment, leading to In-Situ doping of the source and the drain. This technique is known to yield a structure with less defects and hence improved retention times. The studied transistors have $l\mu m$ width (W) and 70nm gate length (L).

At 85°C, different bias conditions were applied to the device in order to identify the sweet spot where a two-sided read window would be possible and, by using the values in Table I, the read window shown in Figure 3 was obtained.

IV. SIMULATION RESULTS

A. Simulated Device Characteristics

The structure simulated in this work (UTBOX SOI) was based on the process information of reference [10]. The gate stack is composed of 5nm of SiO₂ under a TiN electrode. The channel doping level (N_A) is 1×10^{15} cm⁻³ and its dimensions (L x W x t_{si}) are equal to 100 nm, 1 μ m and 20 nm respectively. Below the buried oxide (t_{BOX}) of 10nm, there is a ground plane which is used as a back gate. Although the ground plane is not present in the measured devices, this does

Table II. Sequence of States And Biases For Simulation							
Time [ns]	V _G [V]	V _D [V]	V _B [V]	State			
10	0.5	1.9	1	Write "1"			
10	0	0.5	1	Write "0"			
10	-4.3 : -0.3	1.9	1	Read			
-	-2.5	0	1	Hold			



Figure 4. Simulated read window with its two-sided open region clearly visible and the 5 regions of interest indicated

not have an impact on the appearance or not of the two-sided read window.

B. Simulated Read Window

The results were achieved through numerical simulations, using the signals presented in Table II. The simulations were performed at a constant temperature of 85°C and included the following sequence of operations: write "1", hold, read "1", hold, write "0", hold and, finally, read "0". For each of the read states the current was stored, respectively, as I₁ and I₀.

V. ANALYSIS OF THE READ MECHANISMS

A. Parasitic BJT

In the early years of 1T-DRAM, reading was based on the different V_T caused by charge accumulation in the floating body. However, the second generation of those devices uses the parasitic BJT in a positive feedback loop, thereby greatly improving retention times and sense margins [11]. In every SOI structure, and especially in decananometer devices, a parasitic bipolar transistor is always present [10] as illustrated in Figure 5.

The parasitic BJT may also be used for writing "1" to the memory, as the augmented I/I will lead to a higher concentration of holes flowing to the floating body.



Figure 5. Example SOI structure and its parasitic BJT

B. Gate Induced Drain Leakage (GIDL)

Band-to-Band Tunneling (BTBT) or GIDL is a physical phenomenon where the energy-band bending near the interface between the silicon and the gate dielectric caused by a high positive drain voltage and a high negative gate one causes the Si valence-band electrons to tunnel towards the conduction band [12], leading to a current from the drain to the source.

Although GIDL is used by many authors for writing "1" [6, 11], reading data from a memory through a GIDL enhanced strategy is still a vast field. Nonetheless, it is important to understand that a high GIDL current outside of the read pulse is an unwanted phenomenon [13] and normally leads to data corruption.

C. The Standard Read Window

In Figure 6, a standard read window is presented based on a measurement done using the values in Table III. There is no clear separation of the two dif-

 Table III. Sequence Of States And Biases For Measurement



Figure 6. Measured read window with no clear division between the two operating mechanisms

ferent operating regions and one could think that the mechanisms acting on the open part of the window (i.e. where the sense margin is greater than 0 and measurable) are the same.

D. Analysis of the Read Window

The read window will be divided in 5 regions according to Figure 4 and each of the regions will be explained, starting with region 5 and decreasing V_{Gread} all the way to region 1.

A high positive level of V_{Gread} corresponds to Region 5. During the read cycle, the current crossing the channel is sufficiently high to trigger the positive feedback of the parasitic BJT (single transistor latch up) independently of the charge stored in the floating body.

Region 4 (the right-side open read window) is the usual read window based on the parasitic BJT, where if there is charge stored in the floating body the positive feedback loop (MOSFET-BJT) will be triggered and I_1 will jump to a much higher value than I_0 . One can see the current distribution for a gate pulse of -1.3V in Figure 7.

If we continue sweeping the gate voltage during the read pulse, thus entering into region 3, we will end up with such a small MOSFET current (i.e. the current before the BJT amplification) that it will not change V_T enough in order to trigger the positive feedback loop of the BJT, even if there is charge stored in the floating body. Hence, I_0 and I_1 are almost the same except for a slight current change due to the minimally different V_T .

The left-side open read window corresponds to Region 2. In this region, we have two effects occurring at the same time: GIDL and parasitic BJT current amplification. The dependence of the GIDL current on the parasitic BJT was reported in 1992 in [14]. This dependence is fundamental to the correct understanding of the reason for the existence of this second open window.

In region 3 the channel was already too small to trigger the parasitic BJT positive feedback loop. However, in the right part of region 2, GIDL current becomes more significant and augments the channel current. This increase, coupled with a positive charge stored in the floating body can in effect trigger the parasitic BJT and give rise to a second read window for a much lower gate voltage.

In Figure 8, the current density during the reading of "1" for a gate pulse of -2.9V is presented. It can be seen that the current distribution, with its maximum close to the back-gate, is typical for a read cycle based on the BJT.

The left-most part of the read window, Region 1, presents an already closed window. As V_D-V_G is very high, the GIDL current is significant. Therefore,



Figure 7. Current density during read "1" for a gate pulse (V $_{\rm Gread})$ of -1.3V



Figure 8. Current density during read-"1" for a gate pulse (V $_{\rm Gread})$ of -2.9V

whether there was charge stored in the floating body or not, GIDL is so high that as soon as the read cycle starts the floating body is charged and I_0 is practically the same as I_1 . Read pulses in this region can be compared to a write pulse using GIDL.

It is important to consider that the back-gate voltage (V_B) and the drain voltage (V_D) are the two most important parameters when trying to reproduce the two-sided read window because of their impact on the parasitic BJT triggering point. If V_B was very high one would get no window, a bit too high and one would get a single window and if too small one would get no window at all [15]. Likewise, a high V_D makes it easier to trigger the parasitic lateral BJT whereas a small V_D can render the triggering almost impossible to achieve.

VI. CONCLUSIONS

A measurement system capable of characterizing transistors for 1T-DRAM usage was successfully specified and built. Through the use of this system, the two-sided read window was successfully studied, for the first time, both experimentally and by simulation. This rare phenomenon has been measured, described in detail and the factors leading to its occurrence have been explained. Although during normal operation the device behavior for read and writes is the same independently of the valid read window used, the understanding of this behavior allows for greater device optimization during the design phase.

Usually, we expect to see a standard read window with only one opening. However, it has been shown that with the correct read pulse engineering (mainly selecting V_D and V_B) it is possible to create enough separation between the beginning of the GIDL effect and the parasitic BJT turn off zone.

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