The Roles of the Gate Bias, Doping Concentration, Temperature and Geometry on the Harmonic Distortion of Junctionless Nanowire Transistors Operating in the Linear Regime

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ABSTRACT

The linearity of Junctionless nanowire transistors operating in the linear regime has been evaluated through experimental data and numerical simulations. The influences of the fin width, the gate bias, the temperature, the doping concentration and the geometry on the overall linearity have been evaluated. The increase of the series resistance associated both to the variation of the physical parameters and the incomplete ionization effect has shown to improve the second order distortion and degrade the third order one.

Index Terms: Junctionless Nanowire Transistors; Linearity; Harmonic Distortion; Tunable Resistor

I. INTRODUCTION

Although the development of ultimate MOSFET technologies is dictated by requirements imposed by their application in digital circuits, the increasing demand for Systems-on-Chip, where digital and analog circuits are designed to work together, makes mandatory the study of the analog behavior of novel devices. Most studies devoted to analog applications consider devices operating in the saturation regime mainly for amplifying purposes. However, the evaluation of MOS devices operating in linear regime is important in resistive applications due to the nearly linear dependence of the drain current to the drain voltage. In the case of anti-alias continuous time filters, which are prior to any analog-to-digital converters [1-2], for instance, MOS transistors can play the role of tunable quasi-linear resistors where the source and drain electrodes work as the resistor terminals and the overall resistance is controlled by the gate bias (V_{GS}). The targeted resistance is usually in the order of a few hundred kΩ, which can be attained through the application of long channel transistors. Several advantages are promoted with the use of MOSFETs in these applications with respect to conventional resistors such as the possibility of on-chip control of the on-resistance (according to the bias applied to the gate) and reduction in the die area [3]. In such application, the devices are biased in the linear region around zero DC bias. However, even biased in the linear regime, MOS transistors present significantly non-linear I-V characteristics, resulting in strong degradation of the output signal due to the harmonic distortion (HD). If a sinusoidal is applied in the input of a MOS transistor, for example, the output signal is composed not only by the fundamental signal, but by others of multiple frequencies.

The continuous down-scaling of the MOS transistors has imposed several challenges to the application of planar devices in recent technologies due to the occurrence of severe short channel effects (SCEs). Thus, planar transistors have frequently been substituted by multiple gate ones, which present a gate that covers more than one side of the channel, improving the control of the gate on the depletion charge and reducing SCEs [4]. Notwithstanding, for extremely scaled devices, i.e. sub-16 nm nodes, the ion implant performed to the formation of source/drain regions can become a fabrication process bottleneck since it needs to be very carefully addressed in order to avoid the impurities diffusion into the channel region.

Junctionless Nanowire Transistors (JNTs) have been developed aiming at simplifying the fabrication process for extremely scaled devices. JNTs physical structure consists of a heavily doped silicon wire ($\sim 10^{19}$ cm^{-3}) involved by gate stack, where source/drain and channel present the same doping material and concentration [5-8], as it can be seen in Figure 1, where a schematic view and the longitudinal section of an n-type JNT is shown. Junctionless transistors

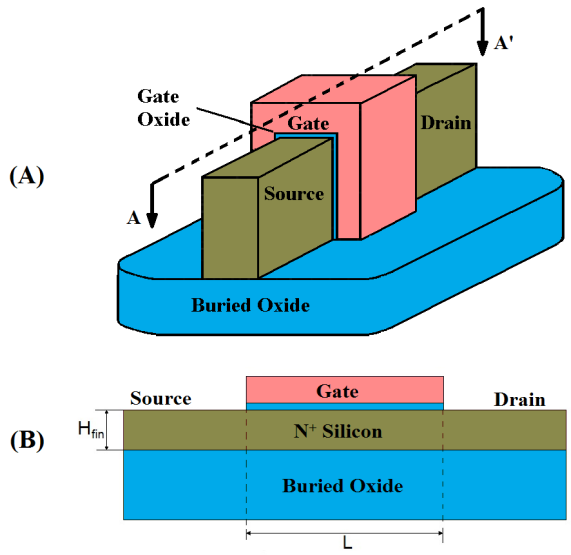

Figure 1. Schematic view (A) and longitudinal section (B) of an n-type Junctionless Nanowire Transistor.

work similarly to accumulation-mode devices, in which the difference between the gate and silicon film workfunctions induces the formation of a depletion layer that fully depletes the channel region when zero bias is applied to the gate, maintaining the transistor switched off. When the gate voltage is increased above threshold, the depletion depth is reduced, forming a neutral path near the center of the silicon layer, which gives rise to a bulk conduction. As the gate bias is raised, the neutral path is enlarged and, at flatband voltage (V_{FB}), the whole silicon layer becomes neutral. Above V_{FB}, an accumulation layer is formed close to the interface, inducing a superficial current flow component [9].

As JNTs present higher channel doping concentration than conventional inversion mode (IM) devices such as triple gate FinFETs, their on-resistance (R_{ON}) is higher than the one of IM multigate transistors of similar dimensions, allowing for the use of shorter transistors to attain the same R_{ON}. Additionally, the smaller doping concentration presented in the source/drain regions makes the series resistance (R_{SD}) of JNTs larger than their IM counterparts, improving the harmonic distortion when operating in saturation as amplifiers as stated in [10]. Other recent studies [11-12] have shown the great potential of JNTs for the application as tunable resistors due to its higher total resistance. The current work aims at verifying the influences of the temperature (T), the fin width (W_{fin}), channel length (L), channel doping concentration (N_D), R_{SD} and V_{GS} on the harmonic distortion of n-type JNTs operating in the linear regime. The entire analysis has been performed based on 3D numerical simulations validated through experimental measurements.

II. DEVICES CHARACTERISTICS AND SIMULATIONS

The 3D simulations presented in the current analysis were performed in the TCAD Sentaurus [13]. Along the simulations, all the devices were biased in the linear region, playing the role of tunable transistors. The curves of the drain current (I_{DS}) were simulated as a function of the drain voltage (V_{DS}) in the interval between -0.2 and 0.2 V for different gate overdrive voltages ($V_{GT} = V_{GS} - V_{TH}$, being V_{TH} the threshold voltage). The simulated devices present fin height (H_{fin}) of 10 nm and gate oxide of 2 nm. The channel length has been varied between 100 nm and 1 μm and the fin width between 10 nm and 20 nm. The simulation considered n-type devices with three different doping concentrations (from $5x10^{18}$ up to $2x10^{19}$ cm^{-3}) in the temperature range between 200 K up to 500 K. The simulations have also taken into account the effect of R_{SD} in the I-V characteristics by considering devices with different source/drain lengths (L_{sd} = 1 and 100 nm). Also, the effects of the bandgap narrowing, the incomplete ionization and the lateral electric field were included in all the simulations. The mobility has been assumed to be constant with V_{GS} and set to 85, 100 and 125 $cm^2/V.s$. for doping concentrations of $2x10^{19}$, $1x10^{19}$ and $5x10^{18}$ cm^{-3}, respectively, according to the values estimated in [14]. In JNTs, the mobility degradation is observed only above flatband and is overlaid by the effect of the series resistance [15]. Quantum confinement related effects have been neglected in the simulations since, according to [4], carriers' quantization is only expected to be significant in devices where one of the silicon layer dimensions is smaller than 7 nm.

In order to validate the simulations, the I-V characteristics of experimental devices, with identical physical characteristics to the simulated ones (H_{fin} = 10 nm, W_{fin} = 20 nm, L = 1 μm and N_D = $1x10^{19}$ cm^{-3}), have been measured. The experimental transistors were fabricated in the Tyndall National Institute, Ireland according to the fabrication process described in [5, 7]. The I_{DS} *vs.* V_{DS} curves of both experimental and simulated devices are presented together in Figure 2 for different

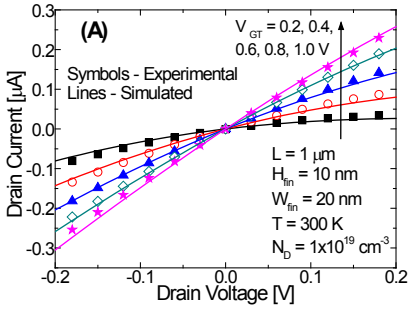

Figure 2. I_{DS} as a function of V_{DS} for experimental and simulated devices biased at different V_{GT}.

gate biases in the V_{DS} range between -0.2 and 0.2 V. As one can see, simulated curves have fitted very well the experimental ones validating the simulations. The maximum error between simulated and experimental curves has been inferior than 3% and 6% for V_{DS} = -0.2 and 0.2 V, respectively.

The simulated I_{DS} *vs.* V_{DS} curves of JNTs with different source/drain lengths biased at several temperatures are shown in Figure 3 (A) whereas the ones for devices with different channel doping concentrations are shown in Figure 3 (B). In both cases, the simulations have considered a device with W_{fin} = 10 nm biased at V_{GT} = 0.5 V. It can be observed that the effect of the L_{sd} variation from 100 nm down to 1 nm is more pronounced in the I-V characteristics than the temperature variation mainly for negative drain biases. Such behavior could be expected since at the same time that JNTs mobility have shown a weak dependence with the temperature [14, 16], the series resistance presented by JNTs can reach the order of hundreds kohms [17], strongly impacting the I-V characteristics. For example, the increase of L_{sd} from 1 nm (for L_{sd} = 1 nm the device is practically not susceptible to R_{SD}) to 100 nm has resulted in a decrease of $|I_{DS}|$, due to the raise of the source/drain series resistance.

The curves of I_{DS} *vs.* V_{DS} for devices with different doping concentrations shown in Figure 3 (B) demonstrate that the drain current increases with the reduction of N_D, which can be correlated to the mobility dependence on the concentration. Heavier doped transistors present smaller mobility due to the larger coulomb scattering [18]. Additionally, the effect of L_{sd} reduction becomes more pronounced as N_D is decreased, indicating an increment of R_{SD}, which can be correlated mainly to the reduction on the density of carriers. As shown in different papers [19, 20], the harmonic distortion can be strongly affected by both R_{SD} and mobility degradation.

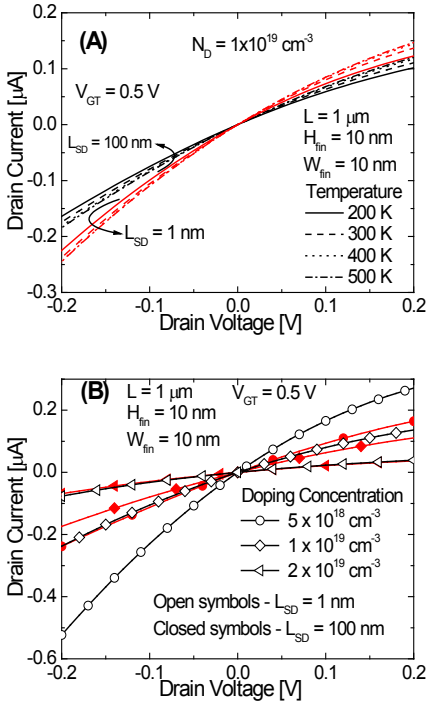

Figure 3. I_{DS} as a function of V_{DS} for experimental and simulated devices biased at different T (A) and N_D (B).

III. HARMONIC DISTORTION EVALUATION

The non-linearity observed in the output signal of a circuit composed by MOS transistors can be evaluated through the harmonic distortion analysis, which consists in determining the ratio of the higher order signals presented in the output to the fundamental one. Although this study is usually performed through the Fourier analysis, this approach requires AC characterization of the devices making the analysis more difficult. For that reason, in the present work, the non-linearity was evaluated through the application of the Integral Function Method (IFM) described in [21, 22], which consists in a mathematical approach that allows for the extraction of the harmonic distortion directly from DC characteristics of the devices. The IFM allows not only for the extraction of the total harmonic distortion (THD) that comprehends the whole non-linearity observed in the output, but also the second and the third order distortions (HD2 and HD3, respectively), which frequently are the main distortion components.

For the analysis of the devices operating in the linear region as tunable resistors, the IFM considers a sinusoidal input bias associated to a DC level applied to the drain of the transistor. In this case, the input signal considered in the drain of the devices is given by $V_{ds} = Vo \pm Va.\sin(x)$ with x varying between $-\pi/2$ and $\pi/2$, being Vo the DC bias (set to zero bias in the current work) and Va the amplitude of the sinusoidal input signal. Initially, the HD evaluation will address HD2, which is the main distortion source in most circuits and, in the sequence, HD3 which becomes the dominant non-linear component in differential circuits such as 2- and 4-MOS resistive structures [23-25].

A. Second Order Distortion

The IFM has been applied to the curves of I_{DS} *vs.* V_{DS} for simulated devices biased at different V_{GT} aiming at determining the best operating gate bias in terms of the second order distortion. The curves of HD2 *vs.* V_{GT} have been presented in Figure 4 (A) for devices of different L_{sd} biased at different T. Similarly to the results presented in the curves of I_{DS} *vs.* V_{DS}, the effect of the

source/drain length on the linearity has been much more pronounced than the temperature variation. The temperature increase from 200 K to 500 K has provoked a reduction of 1 dB in HD2 for the device with L_{sd}=1nm biased at V_{GT} = 0.8 V, whereas the increase of L_{sd} from 1 nm to 100 nm has reduced HD2 in about 5 dB for devices biased at similar V_{GT} with T = 300 K.

As the increment of L_{sd} from 1 nm to 100 nm intrinsically increases the series resistance of the devices and HD2 highly depends on R_{SD} as stated in [20, 26], the effective drain voltage ($V_{DSeff} = V_{DS} - R_{SD}.I_{DS}$) has been calculated for the device with longer L_{sd} in order to compensate the effect of R_{SD} aiming to verify if R_{SD} is the only parameter responsible for the HD2 shift when varying L_{sd}. By considering V_{DSeff} as the drain bias of the devices, HD2 was recalculated through the application of the IFM method. The series resistance of the devices has been determined according to the method described in [27] and resulted in about 100~200 kΩ. Figure 4 (B) shows the curves of HD2 as a function of V_{GT} for a device with L_{sd} = 100 nm with and without the R_{SD} compensation. Also, the HD2 *vs.* V_{GT} characteristic of the device with L_{sd} = 1 nm, where the effect of R_{SD} can be neglected, is presented. Indeed, the series resistance of devices with shorter L_{sd} was also calculated and resulted in values inferior than a hundred ohms. As one can see, by compensating R_{SD}, HD2 of the transistor of L_{sd} = 100 nm tends to the one of L_{sd} = 1 nm, demonstrating that the HD2 dependence on L_{sd} is essentially correlated to R_{SD}. Any increase in the series resistance, reduces the effective input bias, making the devices more robust to HD2 as described in ref. [26], which deals with FinFETs operating in saturation.

When HD2 is evaluated as a function of V_{GT} in Figure 4, it is possible to note a strong reduction of the distortion with the increase of the gate bias, which can be correlated to the operation regime of the device. For $V_{GT} \leq 0.1$ V (considering $V_{DS} = Va = 0.1$ V), the devices are biased in saturation and the drain current tends to a nearly constant value, increasing significantly the non-linearity in the output. For $V_{GT} > 0.1$ V, when the devices are biased in the linear regime, JNTs with larger R_{SD} present lower HD2 as previously mentioned. A similar behavior is presented in Figure 5 (A), where the curves of HD2 vs. V_{GT} are shown for devices of different W_{fin} and L. At low V_{GT}, HD2 is practically the same independently on W_{fin} *and* L, whereas for larger V_{GT} narrower devices exhibit smaller HD2 since these transistors intrinsically have larger R_{SD}. Also, the reduction of L from 1 μm to 100 nm has slightly degraded HD2 for transistors with shorter L_{sd} due to reduction of the total resistance and has strongly improved the distortion for longer L_{sd} since the series resistance becomes more effective in the total resistance.

Figure 5 (B) presents the behavior of HD2 as a function of V_{GT} for devices with different doping

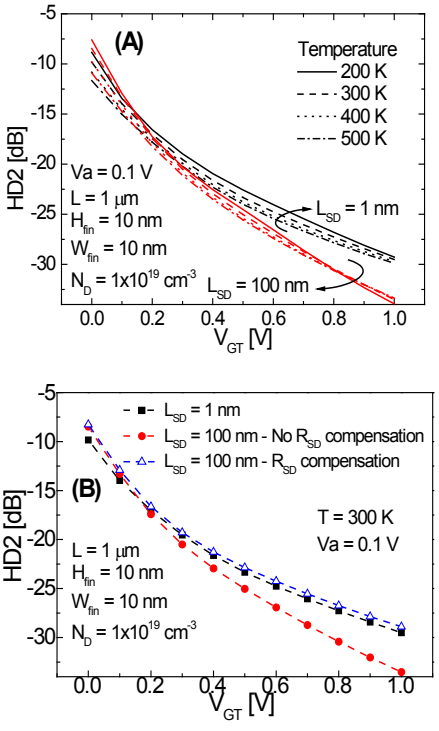

Figure 4. HD2 as a function of the gate voltage overdrive for simulated devices biased at different T and L_{SD} without R_{SD} compensation (A) and at T = 300 K considering R_{SD} compensation (B).

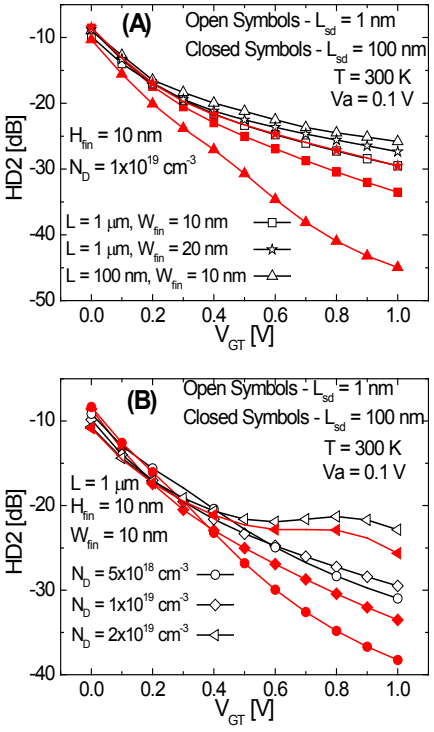

Figure 5. HD2 as a function of the gate voltage overdrive for simulated devices with different W_{fin} and L (A) and doping concentrations (B).

concentrations. HD2 clearly improves with the reduction of N_D thanks to the raise of R_{SD}. Although this behavior results mainly from the reduction on the carrier density, the effect of the incomplete ionization of carriers cannot be neglected. According to [28, 29], silicon layers with doping concentration in the order of ~10^{16} up to 5x10^{19} cm^{-3} are more susceptible to the incomplete ionization of carriers even at room temperature, whereas in layers with doping concentration higher or lower than the mentioned range, this effect only becomes important at low temperatures (T < ~200 K) [28]. In the JNTs, the effect of the incomplete ionization is especially important in the source and the drain regions, where the non-ionization of part of the dopants implies in an increase of R_{SD}, which acquires values extremely higher than the ones exhibited by conventional multigate inversion mode transistors [17], where the source/drain doping concentration is in the order of 10^{21} cm^{-3}.

To verify the effect of the incomplete ionization on R_{SD} of the evaluated devices, the curves of the on-resistance ($R_{ON} = V_{DS}/I_{DS}$, with V_{GT}=1V and V_{DS} = 0.1 V) as a function of the temperature, the fin width and the doping concentration are presented in Figure 6 for all simulated devices as well as R_{SD} for devices with longer L_{sd}. As one can see, R_{ON} and R_{SD} for JNTs with longer L_{sd} increase with both the temperature lowering and the reduction of W_{fin}, whereas for devices with shorter L_{sd}, R_{ON}, which is mainly composed by the channel resistance, is practically independent on the temperature and reduces with the decrease of W_{fin}.

In inversion mode devices, R_{ON} suffers a small reduction for lower temperatures down to 150 K due to the mobility dependence on T. In JNTs, the small dependence of the mobility on the temperature [14], makes R_{ON} nearly independent on T as shown for devices of L_{sd} = 1 nm. In the channel region, the JNTs present larger doping concentration than inversion mode devices, which could contribute for the reduction

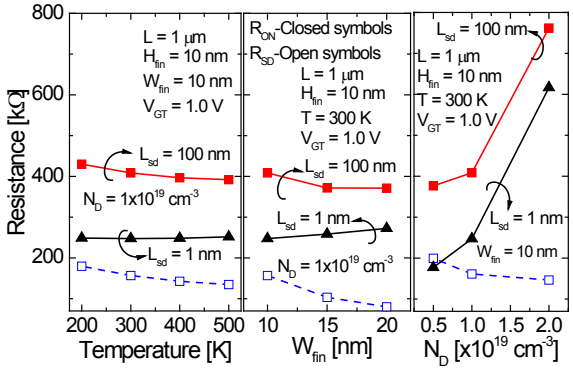

Figure 6. R_{SD} and R_{ON} as funtion of the temperature, W_{fin} and the doping concentration for devices with different L_{sd} biased at V_{GT} = 1.0 V.

of the on-resistance. However, the higher susceptibility of the JNTs channel region to the incomplete ionization phenomenon and the smaller mobility derived from higher N_D contribute for the R_{ON} increase.

The reduction of W_{fin} has led to opposite behaviors of R_{ON} and R_{SD} in devices with short and long L_{sd}. For longer L_{sd}, the resistances have increased with W_{fin} reduction whereas for shorter L_{sd} R_{ON} and R_{SD} have diminished for narrower devices. This behavior can be explained through the higher V_{TH} presented by narrower transistors, making such devices to be biased in deeper accumulation than wider ones at V_{GT} = 1.0 V where R_{ON} is smaller, since flatband voltage does not depend on W_{fin}. The operation regime of the devices is also important in the R_{ON} and R_{SD} analysis for transistors with different N_D. While R_{SD} increases with N_D reduction due to both the smaller carrier density and the incomplete ionization phenomenon, R_{ON} increases with the raise of N_D independently on L_{sd}. As the doping concentration is incremented, the accumulation layer becomes less important in the overall current at a given V_{GT} as described in [30]. As a consequence, an increase of the channel resistance is observed.

The larger R_{SD} presented by JNTs with respect to inversion mode devices have made these devices more interesting for analog applications where very linear characteristics are required, whereas the high values of R_{ON} meets the requirements for tunable resistor applications.

B. Third Order Distortion

Even presenting HD2 slightly smaller than inversion mode devices due to the higher series resistance, most analog circuits need even more linear transfer characteristics. Usually, the desired distortion level can be attained through the application of differential structures such as the 2-MOS one schemed in Figure 7 (A). In such structures, both devices have their gates tied and the input signal is applied symmetrically in the two transistors. Thus, the output signal (I_{DS}) is obtained through the subtraction of the currents that flow in each transistor (I_{DS1} and I_{DS2}) [23] as shown for the studied devices in Figure 7 (B). The application of symmetric signals between the devices leads to the suppression of HD2 in the output, making the total distortion to be dominated by HD3. For that reason, an analysis of the third order harmonic distortion of JNTs has been performed.

Similarly to HD2, HD3 has been obtained directly through the application of the IFM method to the I_{DS} *vs.* V_{DS} characteristics of the devices and is presented in Figure 8 as a function of V_{GT} for transistors with different physical characteristics and temperatures. Initially, HD3 has been shown for devices of different

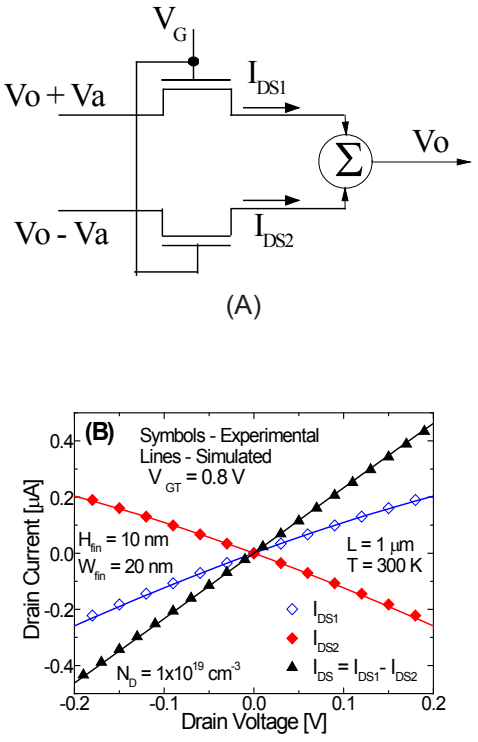

Figure 7. Schematic view of a 2-MOS differential structure typically applied in filters (A) and the drain current as as function of the drain voltage in each transistor and the total current presented in the 2-MOS structure schemed.

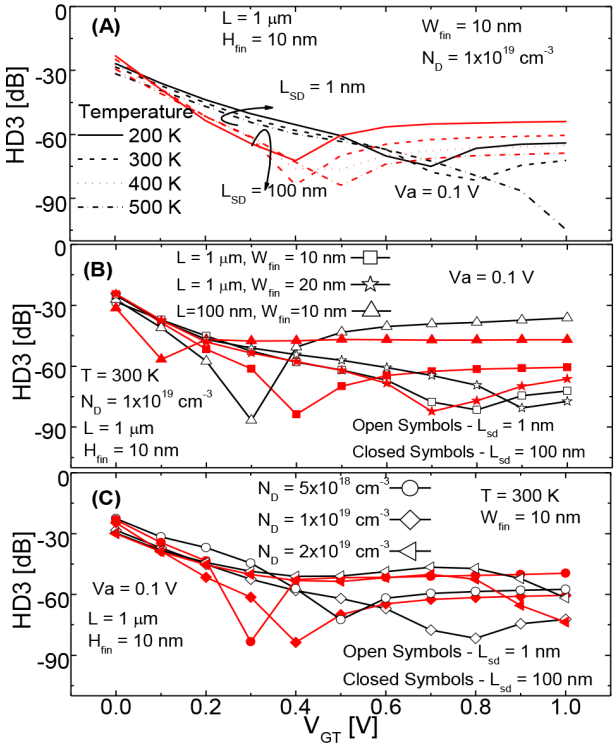

Figure 8. HD3 vs.VGT for simulated JNTs biased at several T (A), with different Wfin and L (B) and doping concentration (C).

L_{sd} biased at several temperatures in Figure 8 (A). It can be seen that the distortion reduces with the raise of V_{GT} at the left side of the distortion minima observed for all the devices as the operation regime of the devices moves deeper into linear region. In inversion mode transistors, the third order distortion at the left of the inversion minima is governed by the body effect [25]. This effect seems to be similar in JNTs. At the right side of the linearity peaks, HD3 tends to be nearly independent on V_{GT} at larger gate voltages. In this region of the curves, HD3 is given by both series resistance and mobility degradation [25]. In inversion mode devices, the effect of the mobility degradation seems to dominate HD3 [19,25]. However, as previously mentioned, the mobility degradation factor presented by JNTs is extremely smaller than the one shown by IM transistors and mobility degradation only becomes non-negligible above flatband voltage. For that reason, R_{SD} is expected to be the main responsible for the HD3 behavior in JNTs at the right side of the distortion minima. In the peaks region, the non-linearity sources compensate each other.

The influence of R_{SD} on the third order distortion can be confirmed through the curves from Figure 8 (A), which exhibit HD3 *vs.* V_{GT} for 10 nm-wide devices of different L_{sd} biased at several temperatures. As one can see, the curves of HD3 for devices with longer L_{sd} present linearity peaks at smaller gate overdrive voltages with respect to the transistors with shorter L_{sd}, demonstrating that R_{SD} starts to dominate the distortion at smaller V_{GT}. Corroborating to this fact, the distortion minima are slightly shifted to lower V_{GT} with the temperature reduction independently on L_{sd} what can be associated to the increase of the series resistance due to incomplete ionization. From the curves of Figure 8 (A), it can also be noted that the increase of R_{SD} leads to the degradation of HD3 at the right side of the distortion peaks, contradicting the improvement promoted in HD2. Thus, it can be conclude that, for JNTs, the increase of R_{SD} improves HD2 at the same time that HD3 is degraded. Although a lower distortion is obtained in the linearity peaks, the position of such peaks along V_{GT} depends on the temperature of operation and process variations. Also, at the left side of the peaks, the devices operation regime tends to the saturation. For that reason, it is more indicated to bias the devices at the right side of the peaks where HD3 is nearly independent on V_{GT}.

Figure 8 (B) shows HD3 *vs.* V_{GT} for devices of different W_{fin} and L, where it can be seen that the linearity peaks move to smaller V_{GT} with the fin width and channel length reduction. Once more, this phenomenon is associated to the increment of R_{SD}. Therefore, wider and longer devices exhibit better linearity than the narrower and shorter ones at the right side of the peaks. So that, whereas narrower and

shorter devices are more indicated for conventional applications where the distortion is dominated by HD2, wider and longer devices are more interesting to the application in differential circuits where the non-linearity is given mainly by HD3.

When HD3 is evaluated for transistors with different doping concentrations in Figure 8 (C), one can also observe the strong influence of R_{SD} in the distortion. As N_D is reduced, R_{SD} suffers an increase moving the linearity peaks from Figure 8 (C) to smaller V_{GT}. Once more, this behavior indicates that R_{SD} prevails over the body effect at smaller V_{GT}, becoming the mainly HD3 source for a larger gate bias range.

IV. INPUT SIGNAL AMPLITUDE

The harmonic distortion has not only been evaluated in terms of the DC gate bias, but also in terms of the amplitude of the input sinusoidal bias (*Va*). This analysis can determine the maximum input bias that can be applied to a transistor in order to attain a desired distortion level. As temperature has shown to play a negligible hole in HD, the current analysis was only performed for devices with different W_{fin}, L and N_D biased at room T.

The curves of HD2 and HD3 are shown in Figure 9 as a function of *Va* for devices of different physical characteristics. As it can be noted, the distortion improves for smaller input sinusoidal amplitudes what could be expected since the I-V transfer characteristics are more linear closer to zero DC bias. The degradation of HD3 and improvement of HD2 with the reduction of W_{fin}, L and N_D shown in Figures 5 and 8 seems to be not dependent on the input amplitude as demonstrated in Figure 9. In order to attain HD3 of at least -50 dB, for example, the maximum Va applied to the shorter JNT must be lower than 0.04 V, whereas the longer device with similar physical characteristics allows for a maximum amplitude of 0.12 V.

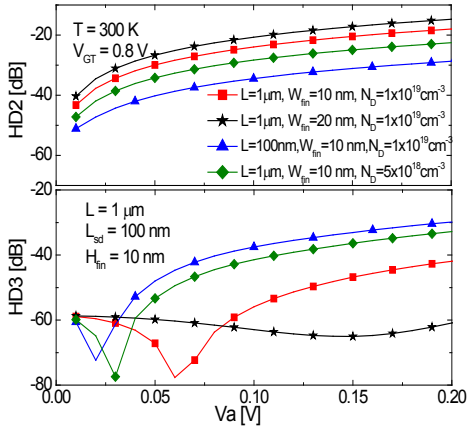

Figure 9. HD2 and HD3 as a function of the input signal amplitude for devices of different W_{fin}, L and N_D biased at 300 K with V_{GT} = 0.8 V.

V. CONCLUSIONS

In this work, an analysis of the harmonic distortion of JNTs operating in the linear region was carried out. The behaviors of HD2 and HD3 were evaluated with the variation of the temperature, gate bias, input signal amplitude, channel width, channel length, doping concentration and series resistance. It was shown that HD slightly depends on the T, but is sensitive to all the other parameters, mainly to the variation of R_{SD}. Indeed, the raise of the series resistance is responsible, at the same time, for improving HD2 and degrading HD3. Also, narrower and shorter JNTs have shown lower HD2 and poorer HD3 than wider and longer ones due to the higher effectiveness of R_{SD} with both W_{fin} and L reductions. Additionally, the reduction of N_D has also contributed to the improvement of HD2 and degradation of HD3 due to the R_{SD} increase. Anyway, the high values of R_{SD} and R_{ON} make JNTs promising for tunable resistor applications.

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