Parameter Extraction and Optimization for the EKV MOSFET Model

Alessandro Girardi, Fernando P. Cortes, Jung Choi, José G. Cipriano, Sergio Bampi {girardi, fpcortes, choi, gómez, bampi}@inf.ufrgs.br

Universidade Federal do Rio Grande do Sul - UFRGS / Instituto de Informática Cx. Postal 15064 - Av. Bento Gonçalves, 9500 - Campus do Vale - Bloco IV Bairro Agronomia - Porto Alegre - RS - Brasil - 91501-970

Abstract

This paper presents a extraction and optimization method for a set of electrical parameters of the EKV MOSFET Model. Electrical simulation are presented in order to compare the accuracy of the foundry supplied model and the extracted and optimized parameters with the experimental data.

1 Introduction

The electrical simulation is one of the most important phases during the design of integrated circuits. In the case of analog circuits, the resulting analysis must be accurate, and the device models used in the simulators must satisfy several criterias. Recent trends emphasize some aspects of MOS modeling for low-voltage digital and analog circuit design. Particularly, the necessity to realistically model the operation of the MOS device in the weak and moderate inversion regions, which have been ignored by most designers for years, has become very important. The advent of deep submicron devices created additional difficulties for modeling short-channel effects and sizing dependency. Moreover, the increase in frequency of operation has passed the limit of validity of quasi-static models and introduced a need for realistic but yet computationally efficient, non-quasi-static models for circuit simulation. The availability of a good MOS transistor model has thus become an important issue for the efficient design and simulation of high performance analog and mixed-signal integrated circuits. The EKV Model has recently found a larger availability as a publicdomain model, and a growing number of analog designers are using it in the academic research as well as in the industrial environments. The quality of the parameters extraction method is fundamental for the usefulness of the simulation model. The objective of the parameter extraction is to obtain a single parameter set which covers all the geometries and device operating regions. In next sections are described the EKV parameters extraction methodology, an optimization tool and electrical simulations using the extracted and optimized parameters.

2 The EKV Model

The EKV MOSFET model is oriented to the design and simulation of analog circuits, high speed digital circuits, mixed mode circuits and low voltage using sub-micron CMOS technology. It is formulated as a "single expression", which preserves continuity of first- and

higher-order derivatives with respect to any terminal voltage, in the entire range of validity of the model. The symmetry of the transistor is preserved by referring all voltages to the local substrate. The state of any point of the channel of a transistor is controlled by V_p - V_{ch} , where the non-equilibrium voltage V_{ch} , simply called channel "potential" is produced by drain and source voltages V_D and V_S , and V_p is the pinch-off voltage depending only on the gate voltage V_G . A general expression for the current is obtained in this model, assuming the mobility is independent of the x and y axis: $I_D = I_f(V_p, V_S) - I_r(V_p, V_D)$, valid for the weak inversion and the strong inversion regions. A complete description of the EKV model can be found in [BUC99]. The extraction techniques presented in this paper concentrate on the parameters that describe the intrinsic part of the MOSFET.

3 Extraction and optimization of the EKV parameters

There are several extraction approaches for the EKV model parameters. In [GOM96a], a strategy for extraction and optimization of the EKV model parameters was developed. The measurement system for MOSFET parameter extraction is based on the semiconductor analyzer HP 4145B and the SGC software [WIR94].

This work presents the same strategy mentioned above to extract the EKV MOSFET model version 2.6 [BUC99]. For the extraction and optimization were used NMOS transistors with L=6 μ , 1.2 μ and W=51 μ fabricated in 0.5 μ CMOS technology from MOSIS. First, an estimation of the parameters VTO, GAMMA, PHI, KP, THETA, UCRIT was made using incremental characterization of the collected DC current data. For COX and XJ parameters the nominal values were used and for the others parameters, default values .

Table 1 – Elky parameters values extracted and optimizated.					
PARÂMETER	SYMBOL	DEFAULT	INITIAL	OPTIMIZATED	UNIT
			VALUE	VALUE	
Parallel multiple device number	COX	0,7e-3	3.5938e-003	3.5938e-003	F/m ²
Series multiple device number	XJ	0,1e-6	2.0000e-007	2.0000e-007	m
Oxide Capacitance	VTO	0,5	0,72682	0.69039	V
Junction depth	GAMMA	1	0,66978	0.70781	$V^{1/2}$
Threshold voltage	PHI	0,7	0,86465	0.93982	V
Body effect parameter	KP	50e-6	2.4926e-004	1.1399e-004	A/V ²
Bulk Fermi potencial	THETA	0	0,18635	0.1676	1/V
Transcontuctance paremeter	UCRIT	2e6	1.5478e+007	2.5695e+005	V/m
Mobility reduction coefficient	DW	0	0	1e-10	m
Longitudinal critical field	DL	0	0	1.669e-9	m
Channel width correction	LAMBDA	0,5	0,5	2.0761	-
Channel length correction	WETA	0,25	0,25	0.25	-
Depletion length correction	LETA	0,1	0,1	0.4944	-

Table 1 – EKV parameters values extracted and optimizated.

After that, it is necessary a parameter fitting procedure. The fitting consists in the optimization of the parameters, using the initial values, by fitting the modelled and the measured drain current. The relative error between measured and modelled data must be computed. Therefore, a direct search optimization algorithm was developed using this strategy [GOM96a]. The simplex method for non linear optimization was used. This algorithm creates points of geometrical 'simplex" using initial values of the parameters with

a small perturbation and a function of each parameter is evaluated in every point. The final routine allows to make not only a global optimization but a local optimization.

The best optimization sequence strategy developed by [GOM96a] is used here. For a long channel device, with L=6 μ and W=51 μ , the extraction is made in two steps: 1) in weak inversion, VTO, GAMMA and PHI must be optimized using I_D vs. V_G curve characteristics; 2) in strong inversion, KP and THETA must be optimized using I_D vs. V_G curve characteristics. After that, a short channel device, with L=6 μ and W=51 μ , must be used: 3) in weak inversion DL and WETA must be optimized using I_D vs. V_G curve characteristics; 4) in strong inversion, UCRIT must be optimized using I_D vs. V_D curve characteristics; and finally, 5) LAMBDA must optimized using I_D vs. V_D curve characteristics have 61 points, V_D=0.05V and V_S=0, 0.25, 0.5, 0.75 and 1V. The I_D vs. V_D curve characteristics have 61 points, V_S=0.V and V_G=1, 1.5, 2, 2.5 and 3V. The other parameters are kept fixed. The resulting values are shown in Table 1.

4 Simulation

In order to evaluate the extracted parameters, electrical simulations are required. Figure 1 shows some simulations results using MATLAB tool with the parameters shown in Table 1.

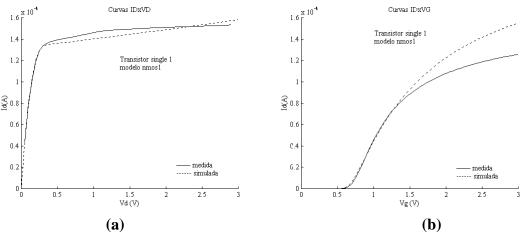


Figure 1 – Comparison between measured and simulated curves (a)I_D vs. V_G (b)I_D vs. V_D

5 Future Work and Conclusion

The public domain EKV MOSFET model is presently available in several commercial circuit simulators. This model includes the most important properties for a good MOS simulation model, such as accuracy and continuity on all operation regions, which makes it suitable for analog design. A parameter extraction methodology for this model has been presented, based on the work in [GOM96a]. Experimental data validate the static model and the associated parameter extraction and optimization.

These extracted and optimized parameters will be used to improve the transistor model and will be used for electrical simulations of several transistors and functional blocks, such as operational amplifiers, comparators. and specifically for TAT transistor on the SOT arrays [GAL94].

6 References

- [SUC80] Paul I. Suciu, Ralph L. Johnston, "Experimental Derivation of the Source and Drain Resistance of MOS Transistors", IEEE Transactions on Electron Devices, Vol. Ed-27, No 9, September 1980.
- [ALL87] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design", New York: Holt, Rinehart e Winston, 1987.
- [BAM87] S. Bampi, "Métodos de Medida e Extração de Parâmetros Elétricos para Dispositivos MOSFET VLSI, 7. Congresso da Sociedade Brasileira de Computação, Anais, Bahia, 1987.
- [ANT88] P. Antognetti, G. Massobrio, "Semiconductor Decive Modeling with SPICE", New York: McGraw-Hill, 1988.
- [GAL94] C. Galup-Montoro, M. C. Schneider, I. J. B. Loss, "Series-Parallel Association of FET's for High Gain and High Frequency Applications", IEEE Journal of Solid-State Circuits, Vol. 29, No 9, Set. 1994.
- [GOM95] J. L. Gómez, "Modelamento do MOSFET Visando à Simulação Elétrica de Circuitos VLSI", Trabalho Individual: PPGC, UFRGS, Porto Alegre, Jan. 1995.
- [WIR94] G. Wirth, "SGC Um Ambiente para a Automação de Procedimentos de Caracterização e Teste", Dissertação, PPGC, Instituto de Informática, UFRGS, Porto Alegre, Dez. 1994.
- [GOM95a] J. L. Gómez, "Extração e Otimização de Parâmetros de Transistores MOS", Trabalho Individual: PPGC, UFRGS, Porto Alegre, Nov. 1995.
- [GOM96] José L. Gómez, Sergio Bampi, "MOSFET Parameter Extraction for the EKV Model with a Direct Search Optimization Method", XI Conference of the Brazilian Microelectronics Society: Proceeding, August 1996.
- [GOM96a] J. L. Gómez, "Estudo Experimental dos Modelos DC para MOSFET com Escalamento de Tensão", Dissertação, PPGC, Instituto de Informática, UFRGS, Porto Alegre, Ago. 1996.
- [BUC99] M. Bucher, et al, "The EPFL EKV MOSFET Model Equations for Simulation -Version 2.6", Technical Report, Lausanne: EPFL, Mar. 1999.