On the design techniques of CMOS integrated inductors

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Abstract— **Inductors are an important passive component in RF IC design. They are used in matching networks and to improve gain capability, for instance. In some applications it is desirable to have both analog and digital circuits on the same chip. In the last decade, CMOS technology has improved its RF performance, and has become a good technological choice for RF IC design. Besides, it is capable of mixing analogical and digital circuit. Unfortunately, inductor performance in CMOS process is very poor due to its low Q-factor and low inductance value per unit area. One can also add the lack of inductor models provided by the foundry, which is necessary for simulation in order to obtain "first-time-right" CMOS RF IC's. In this paper, we discuss the design techniques of CMOS integrated inductors, and present simulation results on inductors, we have designed.**

Keywords—**integrated inductor, planar technology, CMOS, inductor modelling**

I. Introduction

Inductors play a significant role in the realization of Radio Frequency (RF) integrated circuits, as elements in matching networks, and to increase gain capability, nulling out device and parasitic capacitances, for instance. The increasing RF performance observed in MOS transistors, the ability of CMOS to integrate, analog and digital circuits in the same substrate, its high density of integration, low cost and low power consumption, are particularly interesting in smart sensors implementation. In this class of sensors, the sensing element, conditioning circuitry, processing, and communication electronics are on the same chip. CMOS technology is traditionally used and optimized mainly for digital integrated circuits. This situation has left to the CMOS RF IC designer with limited options of passive components and with poor quality, especially regarding inductors. Currently available CMOS integrated inductors have low inductance per unit area, low unloaded quality factor, and low frequency of operation [1]. Furthermore, inductors are not considered standard devices as transistors, resistors and capacitors. Thus, designers do not have at their disposal from the foundry, inductors properly characterized, with appropriate parameters and models for design and simulation [2]. Therefore, we need to carefully study inductors implementation, case by case, in order to obtain "first-time-right" CMOS RF IC's.

In this work, we review the *state-of-the-art* of inductor design techniques in CMOS RF IC's and present the design and simulation of inductors in a standard CMOS process. This paper is divided in six parts. The first part is this introduction. In the second part we describe inductor models, and in the third part inductor topologies are presented.

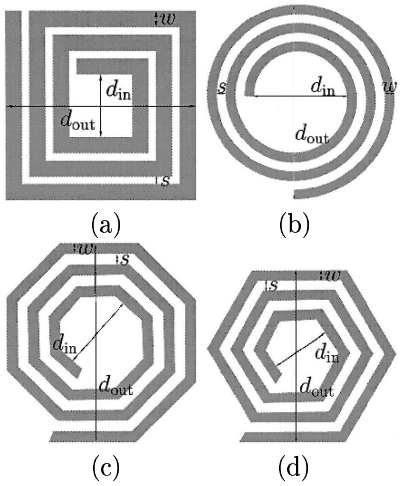


Fig. 1. Examples of commonly used inductor geometries.

In the fourth part we discuss inductor characterization. Next, we present a case study. Finally, the conclusions.

II. Inductor topologies

The most used inductor geometry is the planar, in spiral and squared one (see Figure 1a). Although the circular geometry (Figure 1b) provides a Q-factor $10-20\,\%$ higher [3], non-Manhattan geometries are not allowed (or expensive) in some technologies and layout tools. In this case, the octagonal and hexagonal geometries (Figures 1c and d) can be a compromise between the square and circular ones.

A metal with higher thickness or higher conductivity increases the quality factor at low-frequency. We can increase the Q-factor of an inductor by increasing its area and reducing the dc resistance, using wider metal lines. However, the parasitic capacitance increases with the wire width. Besides, there is an increase in the eddy currents with the wire width, increasing the RF resistance. Therefore, the parasitic capacitances and RF resistance set an upper limit to wire width [4], [5]. A substrate of higher resistivity and an oxide of higher thickness help to better isolate the device from the substrate at high-frequencies and the Q-factor increases [6].

At low frequency, we usually use the minimum spacing between wires to maximize magnetic coupling. However, at high-frequency, proximity effects favor a larger spacing between wires [6]. A large inductor area allows wider metal widths and the designed inductance value can be obtained with a lower series resistance value and, therefore, a

higher Q. On the other hand, at high-frequencies, the Q-factor is dominated by substrate losses and smaller areas are favorable. This fact is more critical for high conductivity substrates, where losses by eddy currents are higher at high-frequency [6].

Based in the observations made above, some improvements can be made to increase inductor performance.

- Use of high conductivity metal layers to reduce resistive losses [7];
- Shunting metal layers to increase the effective thickness of the metal wire in order to reduce resistive losses [5];
- Use of multilevel metal structures in series to reduce inductor area [8];
- Use of low loss substrates to reduce losses at high-frequency [7];
- Use of a higher oxide thickness or suspended inductors to better isolate the inductor from the substrate [12];
- Use of a well, reversely biased, under inductor. The reversely biased well-substrate junction adds a capacitor in series with the metal-substrate capacitance and decrease the effects of capacitive coupling [9];
- Use of a grounded shield between the inductor and the substrate to avoid electric field penetration in the substrate, which implies in losses. We must not use a solid shield, because it degrades the magnetic field, but a special patterned shield of conductor strips orthogonal to the spiral [17].

The connection between spirals in different metal layers can be made in several ways [10]:

- Connect metal layers in parallel with vias all over metal traces or with only connecting the endings. In this way, the effective thickness of the track will be higher than technology allows and as a result, ohmic losses due to the series resistance will be reduced and the quality factor will increase;
- Connect in series spirals from different metal layers in order to reduce the inductor area.
- Build the inductor in the topmost metal level, increasing the spacing between the inductor and the substrate and thus reducing the losses;

III. Inductor model

Integrated circuit design rely extensively on simulation because bread-boarding is impossible and we need "first-time-right" chips as prototyping is expensive. This assumes that models are available for both active and passive devices. Therefore, a scalable physical model, which estimate with accuracy the behavior of inductors with different structural parameters over a wide frequency range, is a valuable design tool. The model presented in [11], [2] is scalable with the inductor geometry with each model element being physically consistent. It takes into account for eddy current effect in the spiral conductor, overlapping capacitance between the spiral and the underpass conductor, capacitance between the spiral and the substrate, ohmic losses of the substrate, and capacitance of the substrate [11].

We show in Figure 2 the physical model of an inductor with inductance value L_s [2]. The other elements are parasitics. The series branch is composed by L_s, R_s, and C_s. The series resistance, R_s, takes into consideration the skin depth of a conductor with finite thickness and the current distribution in a microstrip conductor. The series feedforward capacitance, C_s, is approximated by the

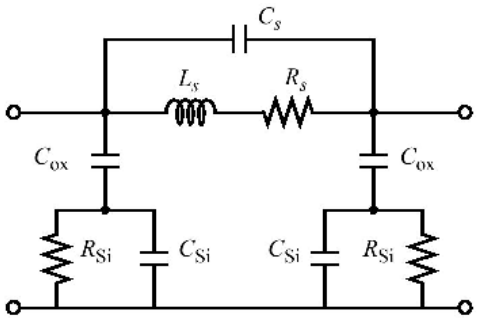


Fig. 2. Physical model for a planar inductor with inductance L_s.

capacitance of a parallel plate capacitor composed by the spiral and the underpass conductor. The capacitor C_{ox} represents the capacitance between the spiral and the substrate. The silicon substrate is modeled by C_{si} and R_{si}. The elements C_{ox}, C_{si}, and R_{si} are proportional to the area covered by the spiral. The parameters C_{sub} and G_{sub} are properties of the silicon substrate and are a result from experimental data fitting. The presented model is limited to substrates with weak doping level and uniform doping profile [2].

The model parameters are calculated as follow [2]:

$$R_s \approx \frac{l}{w \cdot \sigma \cdot \delta(1 - e^{-t/\delta})} \quad (1)$$

$$C_s \approx n \cdot w^2 \cdot \frac{\epsilon_{ox}}{t_{ox_{M1-M2}}} \quad (2)$$

$$C_{ox} = w \cdot l \cdot \frac{\epsilon_{ox}}{t_{ox}} \quad (3)$$

$$R_{Si} \approx \frac{2}{w \cdot l \cdot G_{sub}} \quad (4)$$

$$C_{Si} = \frac{1}{2} \cdot w \cdot l \cdot C_{sub} \quad (5)$$

where l is the wire length in cm, w is the wire width in cm, t is the wire thickness in cm, ρ is the wire metal resistivity, δ is the skin depth, n is the number of superpositions between the spiral and the underpass conductor, $t_{ox_{M1-M2}}$ is the oxide thickness between the spiral and the underpass conductor, C_{sub} and G_{sub} are the capacitance and the conductance by unit area of the silicon substrate, and ϵ_{ox} and t_{ox} are the dielectric constant and thickness of the oxide between the inductor and the substrate.

The inductance calculation is a function of the geometry and accurate calculation either require numerical methods usage (e.g. finite element method, etc.) or the classical Greenhouse method [13].

In the Greenhouse technique, the total inductance of a spiral is calculated adding each wire segment self inductance with all mutual inductance (positives and negatives) between all possible pair of wire segments. The Greenhouse method is sufficiently accurate and of adequate speed (if the algorithm is implemented for computer calculation) for the design and simulation of practical inductors. However, it is quite cumbersome for an initial design and do not provide design insight.

An alternative to Greenhouse method is to use the expressions developed by Mohan et al. [16]. In

TABLE I

MOHAN'S FORMULAS FOR SPIRAL INDUCTANCE CALCULATION [16].

Modified Wheeler
$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1+K_2\rho}$
Current Sheet
$L = \frac{\mu n^2 d_{avg} c_1}{2}\left[ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right]$
Data-fitted Monomial
$L = \beta \cdot 10^{-3} d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}$

TABLE II

COEFFICIENTS FOR MOHAN'S FORMULAS [16].

	Square	Hexagonal	Octagonal	Circle
K_1	2.34	2.33	2.25	-
K_2	2.75	3.82	3.55	-
c_1	1.27	1.09	1.07	1.00
c_2	2.07	2.23	2.29	2.46
c_3	0.18	0.00	0.00	0.00
c_4	0.13	0.17	0.19	0.20
β	1.62	1.28	1.33	-
α_1	-1.21	-1.24	-1.21	-
α_2	-0.147	-0.174	-0.163	-
α_3	2.40	2.47	2.43	-
α_4	1.78	1.77	1.75	-
α_5	-0.030	-0.049	-0.049	-

these expressions, given a geometry, an inductor is completely specified by the number of turns n, wire thickness w, spacing between wires s and one of the following parameters: outer diameter d_{out}, inner diameter d_{in}, average diameter $d_{avg} = 0,5(d_{out}+d_{in})$ or filling ratio $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$. See Figure 1 to better understand these parameters. We summarize Mohan formulations in Table I, where coefficients K_i, c_i, β, and α_i are functions of the layout geometry, according to Table II.

IV. CHARACTERIZATION

The inductor is characterized in general using a network analyzer. A network analyzer is an equipment that measures scattering parameters (S-parameters). S-parameters define input and output variables in function of incident and reflected waves, rather than voltage or currents, which are difficult to measure at RF [15].

In inductor test structures, grounded bars are present near the inductor (Figure 3). These structures allow two kinds of measurements: GS/SG (*Ground-Signal/Signal-Ground*) and GSG (*Ground-Signal-Ground*). The measurements of type GS/SG can be done using either terminals 1, 2, 3, and 4 (GS1 measurement) or terminals 3, 4, 5, and 6 (GS2 measurement). We connect terminals 1 and 3 or terminals 3 and 5 to port 1 for GS1 and GS2 measurements, respectively. For GS1 measurement, current flux in the grounded bar is in the same direction of current flux in the adjacent inductor track and thus the mutual inductance is positive. However, for GS2 measurement, current flux in the grounded bar is in the opposite direction of current flux in the adjacent inductor track and thus the mutual inductance is negative. For GSG measurement, both mutual inductances (positive and negative) tend to cancel each other and a more accurate measurement is obtained [5].

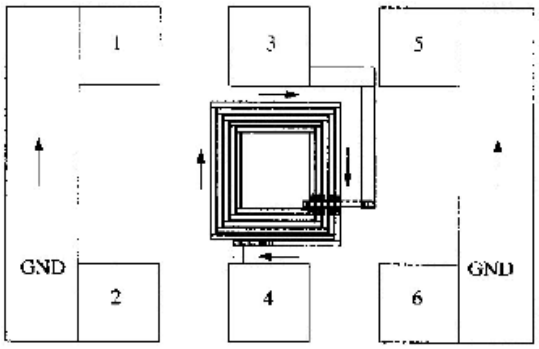


Fig. 3. Inductor layout for GSG measurements [5].

According to [14], there is a relationship between inductor self-resonance frequency and the distance between grounded bars and inductor. As the bar are moved apart from the inductor, the self-resonance frequency increases. For a given distance, the self-resonance frequency saturates. Therefore, it is important to keep these grounded bars near the inductors, in order to have a predictable and well defined self-resonance frequency.

Before using the measured S-parameters for parameter extraction, we need to de-embed the GSG pad effects. This is achieved by measuring the open GSG structure, i.e., without the inductor structure inside. This is usually done by subtracting inductor Y-parameters from the open structure Y-parameters. Then an optimization software can be used to fit inductor model parameters to the measured S-parameters.

There is no unique definition to quality factor Q of an inductor that can be used over a wide range of frequencies. The most used definition is

$$Q = 2\pi \cdot \frac{\text{Energy stored}}{\text{Energy lost in one oscillation cycle}} = \frac{Im[Z_{11}]}{Re[Z_{11}]}. \quad (6)$$

The Z_{11} parameter can be calculate from the measured S-parameters, according to the Equation 7.

$$Z_{11} = \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}. \quad (7)$$

V. CASE STUDY

Now, we present the simulation results of three spiral inductors we designed for the $0.8\,\mu$m CMOS CYE process from AMS (Austria Mikro Systeme International AG). This process has two metal layers and two polysilicon layers. The inductors layouts were drawn using IC Station software from Mentor Graphics. One of the layouts (L3)

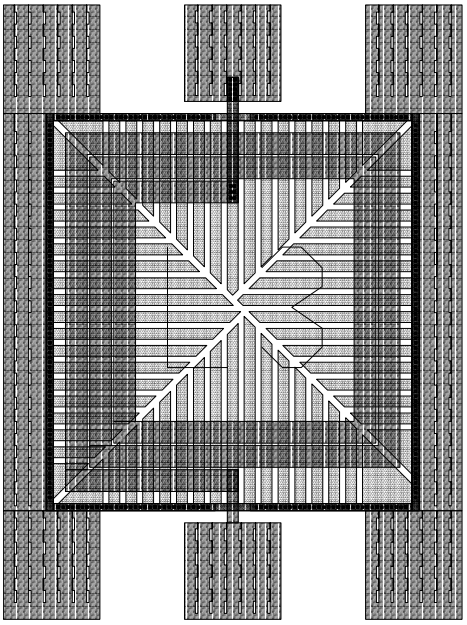


Fig. 4. Layout of the designed two-turn square spiral inductor L3.

TABLE III

DESIGNED INDUCTORS PARAMETERS.

Inductor	d_{out}	w	s	n
L1	210 μm	8 μm	2 μm	4.375
L2	225 μm	4 μm	2 μm	7.375
L3	277 μm	18 μm	2 μm	2.375

is presented in Figure 4. Note that we used a polysilicon patterned ground shield. Inductors parameters are provided in Table III. The inductors were simulated using ASITIC [6] software, where S-parameters were obtained from 100 MHz to 3 GHz. Next, we extracted model parameters from ASITIC simulated data using the model presented in Figure 2 and the optimization software tool Opsim from Mentor Graphics. After that, we obtained new simulated S-parameters using the equivalent circuit with optimized values and Eldo software from Mentor Graphics.

The simulation results can be seen in Figure 5. As can be seen, the simulated results from ASITIC match very well the results from the extracted model. That is, the extraction procedure was done succesfully and the extracted model can now be used in RF circuit simulation.

Simulation results of Q-factor and inductance value are presented in Figure 6a. Note that the inductor with best Q-factor performance has the largest conductor width and therefore low series resistance R_s. It is even important in this technology because it doesn't have a high-thickness metal layer and as it is limited only to two metal layers we can't use shunted metal layers. So, we have to increase metal width in order to have a high Q-factor, but remembering the compromise between Q-factor and self-resonance frequency while using this strategy. We expect that inductance value de-

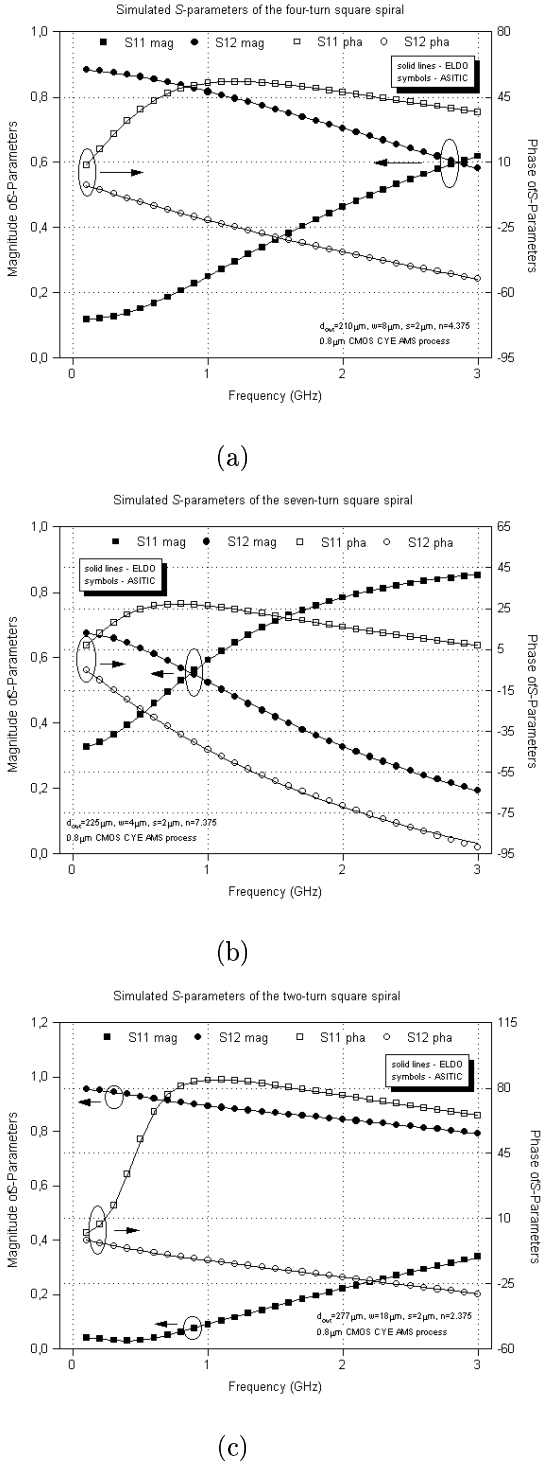
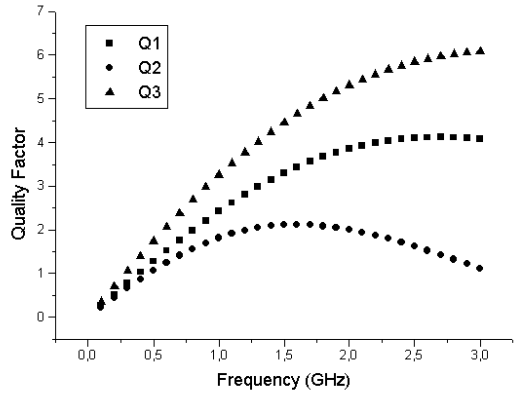
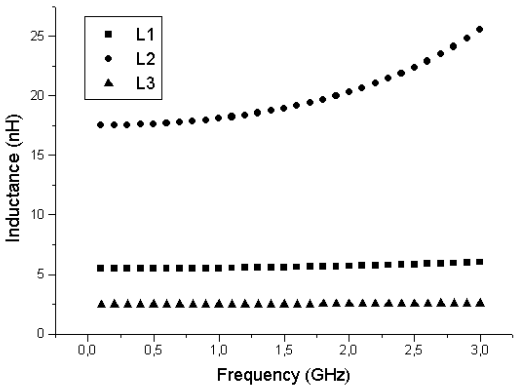


Fig. 5. Simulated S-parameters of the designed inductors (a) L1, (b) L2, and (c) L3.



(a)



(b)

Fig. 6. Simulated Q-factor and inductance of the designed inductors.

creases with frequency due to eddy current effects. But, as can be seen from Figure 6b, the inductance increases with frequency (as more noticeable with L2 due to figure scale). It happens because ASITIC uses an inductor π-model where the inductance is not physically based [6].

VI. Conclusions

We have reviewed some important topics regarding integrated spiral inductor implementation in CMOS technology. Although inductors are not standard components in CMOS process, the current research literature in modeling and simulation turns the task of obtaining "first-time-right" RF IC's more feasible as inductor performance can be accurately predicted.

Mohan's formulations are very appropriate for hand and computer calculation because of their simplicity and accuracy [16]. Square geometry is the easiest to design and modify in most layout tools and suitable for most applications. In the case of AMS CYE process, the only improvement we could use, regarding topology, was a polysilicon patterned ground shield to reduce losses to the substrate. The next step is an optimization of inductors geometry parameters.

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