Process and Electrical Characterization of Diode in NMOS Technology

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***Abstract*—This paper describes the fabrication process and electrical characterization of diodes in a conventional nMOS process. A total of four masks is required to the overall process. An analysis on the series resistance effect and ideality factor is performed.**

I. INTRODUCTION

ALL the manufacture process and characterization was done at AIME during a week whereas the characterization process in this study was realized at LSI.

A total of four masks is necessary for the overall NMOS process and four different chips are processed together:

- C1 and C2 contain elementary devices for electrical characterization;
- C3 and C4 neither contain some integrated circuits based in NOR gates.

This paper is specific about the diode (item1) of chip C1 that contains:

1) One diode N+/P- with 200µm to 200µm;
2) One square capacitor with 500µm to 500µm;
3) One square rectangle capacitor with 146µm to 854µm;
4) One transistor court NMOS (length 6µm, with 180µm);
5) One transistor long NMOS (length 18µm, with 180µm);
6) One diffused resistance N+ with square 878 µm x 28 µm;
7) One group of 24 minimum contact dimensions for diffused N+;

The figure 1 shows the devices disposition of Chip 1

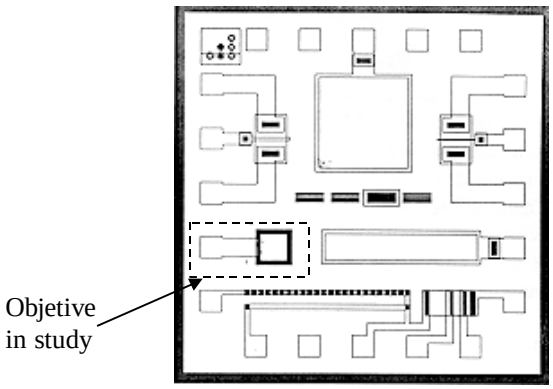

Figure 1 - Chip 1 devices disposition

II. PROCESS DESCRIPTION

The overall nMOS process is described for the sake of clarity instead of the fact that not all the process steps would be required for the diode fabrication.

This chip was fabricated in a p-type substrate with an initial concentration of about $9x10^{15}$ cm^3. After the wet oxidation the photolithography one (used to open the chip active zones). Following, a 65nm thick gate oxide is grown. Polysilicon is deposited and n-type doped with phosphorus.

Photolithography two is made to define the polysilicon and to determine source and drain regions and consequently the canal length.

The drain and source diffusion process is performed and a protection SiO_2 layer L.T.O. (Low temperature Oxidation) is made over the whole the wafer.

In the photolithography three the contact holes are opened

followed for the metalization where a 500nm thick aluminum layer was deposited.

Thereon in the photolithography four we make the metal definition and it is annealing. The oxide thicknesses measured after the process are:

1) Mask oxide e_m = 5.39 μm;
2) Gate oxide e_g = 0.665 μm;
3) Diffusion oxide e_d = 0.752 μm;
4) L.T.O deposition oxide e_n = 2.836 μm;

To form the characterized diodes, the cathode region is similar to drain and source of nMOS transistor and the anode contact is the substrate. The cathode connection is accessible by a ring-shape that has a window to permit expose the diode to light to use it as a photodiode.

III. EXPERIMENTAL RESULTS ANALISIS

We extracted the diode I-V curve applying an anode varying voltage from –1V to 2V (steps of 0.2 mV).

Figure 2 presents the I-V curve obtained for the fabricated diodes.

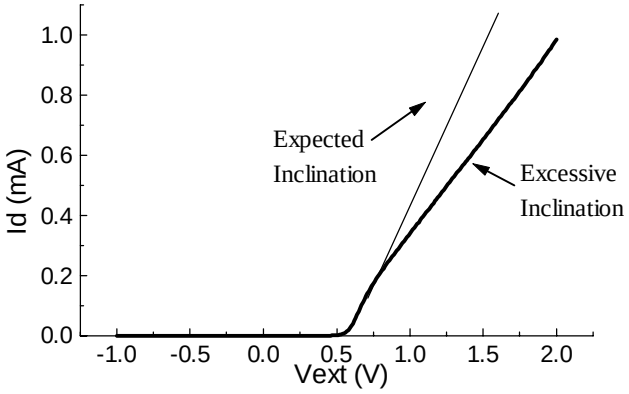

Figure 2 - I-V Characteristic of p-n junction diode in study

We can note an abnormal conduct on this diode when it is forward biased represented by an excessive inclination. Probably it occurs due an effect of ohmic losses in the series resistances associated to the intrinsic diode.

The series resistance effect influence the output current for applied biases larger than 0.85 V.

The intrinsic diode current is described by equation (1):

$$I = I_0\left(e^{qV_D/nkT} - 1\right) \quad (1)$$

where I_0 is the reverse bias current, q is the electron charge, V_D is the effective diode voltage, k is the Boltzmann constant, T is the absolute temperature and n is the ideality factor.

We can represent the ohmic losses in a diode adding a simple resistance in series with the junction, as indicated in figure 3.

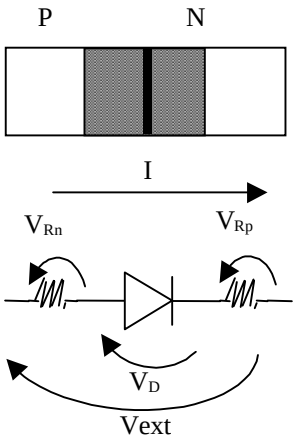

Figure 3 – The voltage drop in parasitic resistances when the diode is forward biased

If we represent a resistance in series of the p and n regions by R_p and R_n, respectively, we can write the effective diode voltage (V) as:

$$V_D = Vext - I[Rp(I) + Rn(I)] \quad (2)$$

Extrapolating the current in the linear curve when the diode is forward biased and considering the diode resistance is the sum of parasitic resistances ($R_D = R_p + R_n$) we find the diode resistance $R_D \cong 1600\ \Omega$.

We can find the effective voltage applied in the diode for the difference between the external voltage applied and the voltage drop in R_D . For example, considerate the point where Vext = 1.27V we know that the voltage drop in the parasitic resistances is V (R_D)= 0.82 V, so the difference between the external voltage applied with the drop voltage in parasitic resistances results in the drop voltage in diode junction V_D=0.45V equation (2).

This reduction in V_D lowers the level of injection so that the current increases more slowly with increased bias. A further complication in calculating the ohmic loss is that the conductivity of each neutral region increases with increasing carrier injection, since the effects of R_p and R_n are most pronounced at high injection levels.

We can design devices by appropriate choices of doping and geometry, in this case it occurs only for very high currents, outside the normal operating range device.

By monitoring the inverse slope extrapolating the linear

region in the same I-V curve but in logarithmic scale (Figure 4) one can extract the ideality factory. The measured slope is 66 mV/dec, which results in n≈1.1 what demonstrates the efficiency of this diode.

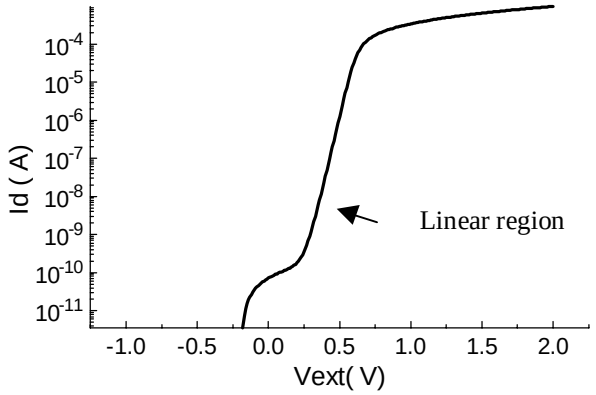

Figure 4 - I-V Characteristic of p-n junction diode in study in the logarithmic scale.

IV. CONCLUSION

This paper performed an electrical characterization of diodes fabricated under a conventional four masks nMOS process. The fabrication process has been described and the resulting diodes were reversely and forwarded biased. An excessive series resistance associated to the neutral diffusion regions and contact resistance has been observed and the value of this parasitic resistance has been estimated. The diode presented good ideality factor.

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