DESIGN AND DISCRETE IMPLEMENTATION OF A SIMPLE SIGMA-DELTA ADC

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ABSTRACT

In this work the top-down design and discrete implementation of a Sigma-Delta (ΣΔ) oversampling ADC is presented. The main feature of these converters is that they can yield a moderate resolution using simple analog circuits, trading the need for accurate analog components for more complicated digital circuitry. Here, a VHDL behavioral description is used to build an all-digital circuitry implemented in programmable logic.

1. INTRODUCTION

The basic Sigma-Delta A/D conversion process is the conversion of a continuous analog signal into a discrete signal (in both time and amplitude). This analog signal is sampled at many times the Nyquist rate with the multiple M defined as the oversampled ratio in Sigma-Delta converters [1]. These Sigma-Delta converters relax the requirements placed on the analog circuitry at the expense of more fast and complex digital circuitry, which is well suitable with VLSI technology. Another advantage is that they simplify the requirements on the analog anti-aliasing filters for ADC (in most cases, a simple RC filter suffices), and a sample-and-hold circuit is usually not required in virtue of its high input sampling rate and negative feedback [1,2].

2. THE SIGMA-DELTA ADC ARCHITECTURE

In Sigma-Delta ADC, whose block diagram is presented in Figure 1, a Sigma-Delta modulator (ΣΔM) is used working to a sampling frequency ($fs=Mf_N$) many times higher that the Nyquist frequency (f_N). In these converters there is not a one-to-one correspondence between input and output samples, they inherently include digital low-pass filter, and hence each input sample value contributes to a whole train of output samples. This output digital filter attenuates quantization noise, signals of interference and undesirable high frequency components.

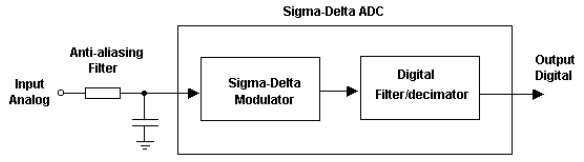

Figure 1 Oversampling Sigma-Delta ADC.

This project has the goal to show the high capacity of Sigma-Delta ADC to achieve moderated precision in its simpler version, even using discrete components. Therefore, a topology of first-order is selected and analyzed. The structure of the basic first-order Sigma-Delta ADC is shown in Figure 2(a). This structure uses a continuous-time Sigma-Delta modulator, which consists of a continuous integrator and a comparator, with a 1-bit DAC employed in the feedback path. Because of the negative feedback, in the time domain the error signal (delta) tends to be minimized, and the output oscillate in such a way that its half value follows the input signal. The digital filter that follows performs, digital low pass filtering and down sampling (decimation) of the 1-bit data stream generated by the ΣΔM.

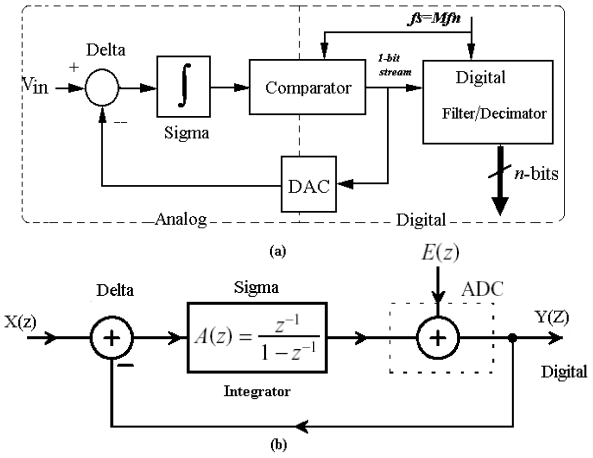

Figure 2 a) First-order ΣΔM and output digital filter
b) linearized model of the first-order ΣΔM

To estimate the maximum precision of the Sigma-Delta ADC it is necessary to carry out an analysis of this structure to calculate the signal-to-noise ratio (SNR), and this way to know the effective number of bits. Diverse authors carried out this analysis type using a linear model for the comparator [1,2]. The quantization process performed by the comparator is associated to a white additive noise, and the integrator is an accumulator of the differences between the input and output signals. The transfer function of this linear model (figure 2(b)) in the frequency domain is given by

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \quad (1)$$

Then, while the input signal passes suffering just a delay, the quantization error is attenuated in the low frequency range (high pass filter). It must be noticed that this error includes also the offset voltage of the opamp (to form the integrator). Therefore, a lossy integrator makes this error be partially canceled, and produces a decrease in the SNR, which restricts the gain of the opamp to be higher that 2M [1], where M is the oversampling ratio.

Of the equation (1), the necessary minimum oversampling ratio (M) for an effective number of bits (N_{eff}) is given by [1]

$$M \geq 10^{(0.2\,Neff)} \quad (2)$$

However, it should be kept in mind that equation 2 corresponds to an ideal SNR that does not consider noise generate by clock jitter, thermal noise, distortion caused by the non idealities of the devices, and also supposing a ideal digital filter (or, a very high order digital filter). Therefore, in the final

project a tolerance margin should be used to reach the desired resolution, the one obtained after the digital filter.

The comb filter was proposed as a down sampling filter for Sigma-Delta converters because of its simple operation and linear phase characteristic [1]. It can be decomposed to a cascade of K integrators and K differentiators (comb) that can be implemented only with sum (or subtract) and delay operations without any multiplication [4]. The order of differentiators can be reduced to one when they come after the down sampling of ratio R, as shown in equation (3)

$$H(z)=\left[\frac{1-Z^{-R}}{1-Z^{-1}}\right]^{K} \equiv \frac{1}{(1-Z^{-1})_1}\cdots\frac{1}{(1-Z^{-1})_K}\{\downarrow R\}(1-Z^{-1})_1\ldots(1-Z^{-1})_K \quad (3)$$

These features allow one to design any order comb filter, that can further be described directly in VHDL and implemented in programmable logic.

3. FUNCTIONAL SIMULATION

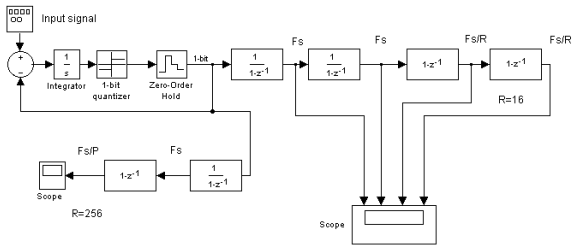

Figure 3 Modeling for functional simulation

Functional simulations are realized to characterize the overall system performance using the Simulink tool of Matlab. The first-order ΣΔ converter functional implementation is illustrated in Figure 3 using both first-order and second-order cascaded integrator comb (CIC) filter. The frequency response of both CIC filters is show in Figure 4. These CIC filters down sample the modulated signal stream from *fs* to an intermediate frequency (minimum f_N) to produce a high-resolution output digital signal.

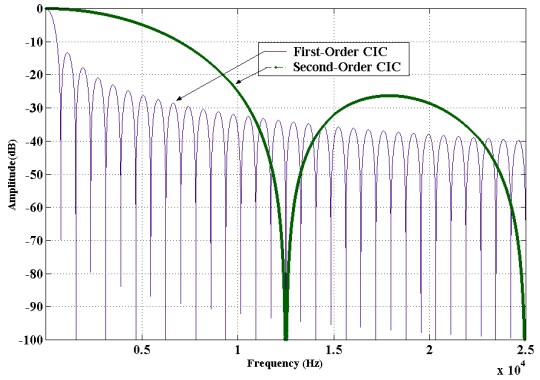

Figure 4 Frequency response of first-order and second-order CIC filter.

4. DISCRETE IMPLEMENTATION

The first-order Sigma-Delta converter implementation is illustrated in Figure 5. The continuous-integrator and comparator are implemented with CI LM358 and all digital part is implemented using a FPGA (EPM7128SLC84). In order to avoid register overflow in the integrators section, the word length has to be equal to ($b_o + K\,log_2\,R$) bits [3], where b_o is the number of bits at the filter input.

The time constant of the integrator is give by:

$$RC = \frac{1}{fs} \quad (4)$$

Where *fs* is the sampling frequency.

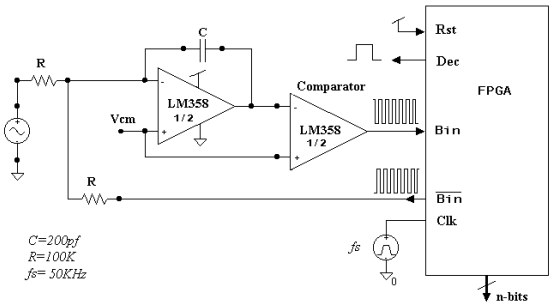

Figure 5 Discrete implementation of the first-order sigma delta converter.

5. EXPERIMENTAL RESULTS

The experimental results are shown in Figure 6. The input signal is 12.5Hz, sampling frequency is 50KHz and an oversampling ratio of 500 is used.

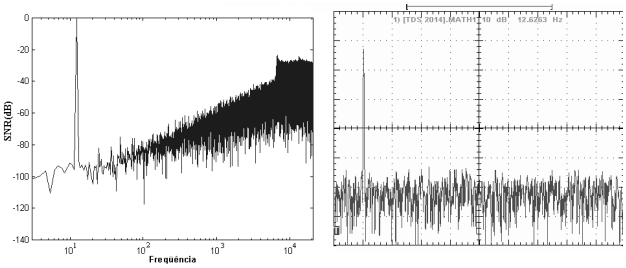

Figure 6 Frequency spectrum a) sigma-delta modulator output b) filtered sigma-delta modulator output.

The final first-order sigma-delta converter achieves a SNR of 44-53 dB for first-order and second-order digital filtered, respectively, for a –3dB full-scale signal power. It is equivalent to a resolution of 8-9 effective bits.

6. CONCLUSIONS

The design and discrete implementation of a simple first-order sigma-delta converter was presented. The viability of this technique was demonstrated to reach moderate resolution in low frequency, even in its simpler version. Based on the results we have demonstrated that sigma-delta converters leads to relatively simple design specifications for the analog circuitry, and are a viable solution for integrated implementation in VLSI technologies.

7. REFERENCES

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