LAMPIÃO = LDN - ARQUITETURA DE MICROCONTROLADOR E PROPRIEDADE INTELECTUAL PARA AUTOMAÇÃO

Hércules S. Padilha Jr e Edval J. P. Santos

Laboratório de Dispositivos e Nanoestruturas, Departamento de Eletrônica e Sistemas
Universidade Federal de Pernambuco

ABSTRACT

In this paper we will present the architecture of the LAMPIÃO microcontroler. It was developed to be used in Smart Sensors. The architecture was written and simulated in VHDL using XILINX® environment. In this enviroment, LAMPIÃO was used to control the cooling system of a machine.

1. INTRODUCTION

Smart Sensors, as we can see in the Standards of the IEEE 1451, are devices that have in the same IC the measuring element, the compensation functions, data processing and lan comunication subsystems. Today, these devices are largely used in the industry. They can be projected to be self adjusted, do self test, use technics of digital processing, ... These kind of sensors have become possible because the exponential reduction in price that the microelectronics' technology has caused in the electrocnics processing systems. In this context, we idealized LAMPIÃO, the abbreviation of LDN - Arquitetura de Microcontrolador e Propriedade Intelectual para automaçÃO. (LDN - inteclectual property of microcontroler's architecture for automation) LDN is the abreviation of nano structures' laboratory.

The paper is divided in five parts, where this introduction is the first. In the second part is made a discription of the project's metodology. In the third part is presented the microcontroler's specifications, followed by the schematic of the microcontroler's architecture. We defined the instructions with the corresponding operation codes, and finally, each part was simulated, where their speed is measured. The paper ends apresenting an example of aplication en automation and finally, our conclusions.

2. METODOLOGY

The LAMPIÃO microcontroller is described in VHDL. The development using a hardware description language becomes easy of being simplified and make the project be very dynamic, fastest and easy of being understood. This because it's simple, in the time that you have the code ready, modify it, add or remove functionalities. Therefore, the microcontroller can be changed to attend a specific demand. In this form of project, when you have the project implemented in programmable devices, they automatically incorporates the technological

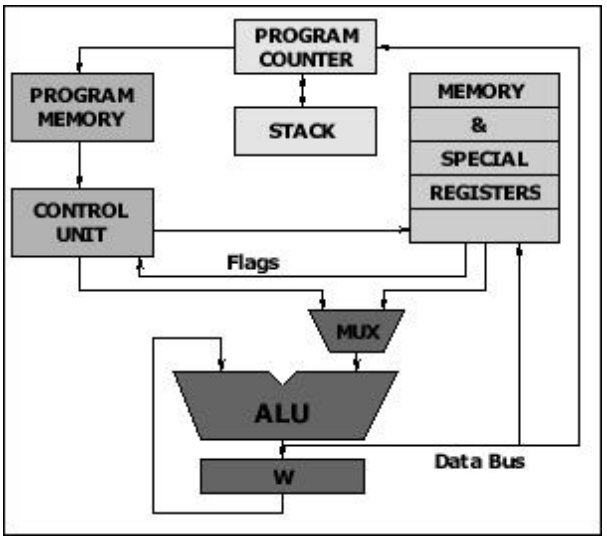

Figure 1. Block Diagram of the LAMPIÃO microcontroler

advances that the same ones will have, without any modification, besides becoming possible the industrial implementation of the device because many companies today accept the VHDL, as the discription of the project of Integrated Circuits.

The VHDL was written and simulated in XILINX®'s environment, available inside of the university program of the company. The proposed architecture was the Harvard one, using somethings found on the architecture of the PIC microcontroller of Microchip®. In this architecture, the data and instructions bus for transference are separated, saving the number of accesses to the memory and increasing the speed, even so losing in area. The instructions are implemented in ortogonal mode, making possible to each one of them uses all kinds of addressing available.

3. LAMPIÃO MICROCONTROLER

For the development of microcontroller's description, the first step was establish its specification. In summarized way, the specification is as it follows: Harvard architecture, 2 I/O ports of 8 bits (each bit configured separately), watchdog timer, timer, 2 inputs for external interruption, program memory with 256 positions and a stack with 8 levels.

The strategy used in the description was to divide LAMPIÃO in some blocks(each block is represented with a different color in Figure 1), make the description of each block and its simplification. Later, all the blocks are combined in only one block. The microcontroller was divided in the following blocks: control unit with program memory, arithmetic and logical unit, memory, program counter and stack. The program memo ry has an input bus of 8 bits for the address position and an output bus of 10 bits for the code of the corresponding operation saved in that position. This code is delivered to the control unit that will command the state of all the other blocks. For this , we choose a set of 19 instructions made its contents of logical operations, arithmetical operations, program flow instructions and storage ones. Later, it was attributed to the each instruction, operation codes, including in itself the arguments. In this way, with an only access, the microcontroller already have the instruction and arguments to it, as address, for example, what it becomes the access fastest.

To define the number of bits of the operation codes, each instruction was analyzed on the number of arguments that it can have. For example, instructions that uses the bank of registers had 32 codes attributed to itself, while the program flow instructions have 256 codes, what reflects the size of the data memory and the program memory respectively. Thus, after analyzed each instruction we found 1016 different codes, what results in instructions of 10 bits. These operation codes had been distributed using Karnaugh map, as in the Table 1. Using this, the instructions with similar functions have similar codes, facilitating the synthesis and reducing the final space placed in the FPGA.

Table 1.Map of the opcodes from $00B_7B_6B_5B_4$0000 to $00B_7B_6B_5B_4$FFFF.

	00	01	11	10
00	outras	BCLEAR/BSET	ADDWF	ADDWF
01	ANDWF	ANDWF	SUBWF	SUBWF
11	MOVWF	MOVWF	ORWF	ORWF
10	MOVFW	MOVFW	XORWF	XORWF

This block of the Arithmetic Logical Unit is purely combinacional, with exception of work register "W". The third block is the data memory and special registers. In this block, we have 29 positions of common use and also the peripherals as the I/O ports, the status register and the acess to the timers. In this way, the microcontroller don't need to use specific instructions to have access to them and the program is facilitated. The last block is the program counter and stack. The stack was implemented with 8 levels that is a number of interruptions or calls that LAMPIÃO can do without losing the way to return to the original position.

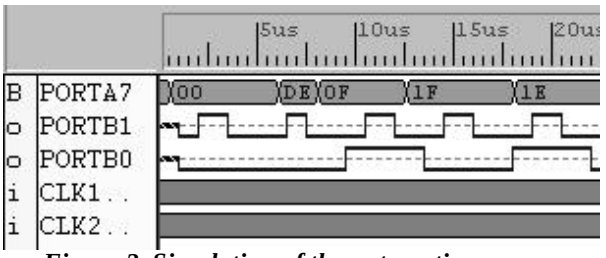

Figure 2. Simulation of the automation program

4. SIMULATION

To test the microcontroller, we made a program based on a small system of automation for temperature control. The microcontroller commands a cooling system of a machine from the value of temperature read by a sensor through a A/D converter. Observing the presented diagram in Figure 2, the microcontroller gives to beginning the conversion of the temperature through a pulse in the B1 pin. The microcontroller waits a small period, reads the value through the A port, makes the calculation to see if the temperature reached the value of activation and acts through the output pin B0, setting in motion or not the cooling system. In this example, the predetermined value in the program was "1F" and the cooling system is activated in high level. The final result of the compilation showed that this system uses half of the FPGA device used, virtex XC50, and reaches the performance of up to 50 MHz.

5. CONCLUSIONS

Due to simplicity of project using VHDL the use of the LAMPIÃO is possible easily to include new operations extending. The current project uses 50% of the FPGA, what gives a good edge of work to develop other functions, peripherals, or to extend its memory. Also, in accordance with the simulator, in the current version, LAMPIÃO can work in up to 50 MHz, what it represents a superior speed to the demanded one in many applications in automation. We have a code written in a world-wide used language that can be implemented in modern devices extendig its capacity or serving of the beginnig for devices of a bigger capacity.

6. REFERENCES

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