DEVELOPMENT OF A COMPUTATIONAL TOOL FOR THE EVALUATION OF EMC PARAMETERS IN INTEGRATED CIRCUITS – COMPARISON AMONG SOME CAPACITANCE MODELS

G. S. Beserra; R. M. D. Rangel; L. R. A. X. de Menezes

Universidade de Brasília

ABSTRACT

In this paper it is proposed the development of a CAD tool that allows the extraction, from the layout, of parameters that affect the performance of integrated circuits. Empirical formulas were used to estimate the parasitic capacitance between two or three lines, as well as the total capacitance in each one of them. Formulas to calculate the self and mutual inductances were also used. As an example, the mutual capacitance between two interconnection lines was calculated using the program, and the results were compared to other results from different models. This paper is a first approach to the study of EMC (Electromagnetic Coupling) in integrated circuits.

1. INTRODUCTION

The advance of technology has allowed a better performance of integrated circuits. However, as the level of complexity increases, the effects caused by capacitive coupling between interconnection lines become much more significant. These effects were showed in several types of CMOS circuits in [1], where a model to calculate the crosstalk is proposed. Moreover, the effects caused by inductance have become worse as the clock frequency increases [2]. Then, it is crucial to develop new techniques to extract those parameters.

The parasitic capacitances can be calculated by numerical or analytical methods. Analytical methods are restricted to certain geometries, while numerical methods are robust but demand a large computational power when they are implemented in CAD tools. Because of that, empirical formulas [3] were developed. As these empirical formulas depend only on physical dimensions of the circuit, it is possible to develop an efficient computational tool to evaluate the EMC parameters of interconnection lines from its layout. The layout consists of a set of graphical patterns that represent active and passive components, and the interconnection among these elements. The parameters that affect the crosstalk are the length *L* and the width *W* of the channel of the MOS transistors, the thickness *T* of the lines, and the distance *S* between the lines.

2. EMC PARAMETERS EXTRACTOR SOFTWARE

In this work a first approach of a CAD software was developed, based on the analysis of conductive lines placed in parallel on a semiconductor surface.

The main electromagnetic interference phenomenon in this configuration is the crosstalk between lines, whose most relevant parameters are the capacitances due to the presence of conductors with a dielectric material between them. In order to achieve these parameters, the mathematical formulas proposed by Sakurai [4] were used.

Since electric current flows on the conductive lines, inductances appear, especially in the case where a great loop is made on a chip. However, for this first software version, an inductance analysis (self and mutual inductances) was done by the use of Ruehli's mathematical approach, for self-inductance calculation, and Grover's formulas for mutual inductance [2]. The limitations due to the use of empirical formulas were used as delimiters of the physical parameters inserted by the user.

From these specifications, the software was developed using the Microsoft Windows operational system and the C++ programming language. The CAD software main algorithm can be described by the following sequence:

- *Selection of EMC parameters and quantity of conductive lines;*
- *Input of physical parameters;*
- *Test routines for input data;*
- *Mathematical calculations;*
- *Presentation of the results in graphical and numerical ways.*

The software was divided in three forms. The data input fields are enabled according to the parameters' type and conductor lines number's selection, in order to avoid accidental data input. The last form (Fig. 1) shows the results of a schematic corresponding to the coupled line configuration. With these values, the designer is able to identify the critical areas in the layout design, and try to optimize the circuit to achieve a better solution minimizing the EMI.

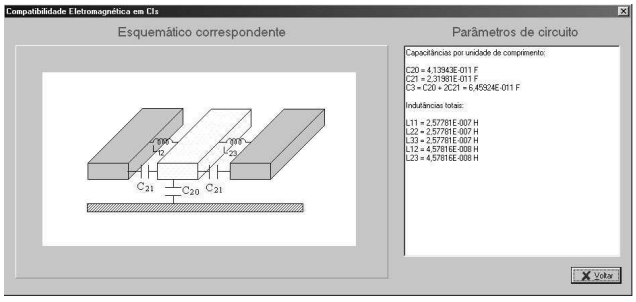

Fig. 1 – Presentation of the results

3. THE CAPACITANCE MODELS

The dimensions of two identical interconnection lines (Fig. 2) from CMOS 0.35 micrometers AMS (Austria) technology were used as examples to compare the results of Sakurai's

formulas [4] given by the developed program to the results given by an applet, available on the website Eecircle [5], that calculates the inductive and capacitive coupling between two parallel microstrips, and also to the results calculated by the software *Serenade SV 8.5 for Windows*, by Ansoft Corporation. The field oxide thickness *H* is 0.29 micrometers, and the metal 1 thickness *T* is 0.67 micrometers. The width *W* and the distance *S* between the lines were varied according to the range given by Sakurai [4] and to the limits given by the technology. The results are presented in Tables 1 and 2, where *Cm* and *Cp* mean mutual and self capacitances, respectively. Fig. 3 and Fig. 4 show the comparison among the different methods used to calculate the mutual capacitance.

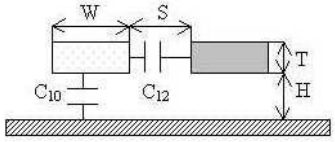

Fig. 2 – Interconnection lines and their parameters [4]

S	Sakurai		Eecircle		Serenade	
(um)	C_{12}	C_{20}	Cm	Cp	Cm	Cp
0.45	79.0	183.7	5.8	140.6	5.9	129.4
0.55	63.3	190.8	4.2	140.5	3.8	128.5
0.65	52.3	196.1	3.1	140.4	2.6	128.2
0.75	44.2	200.3	2.3	140.3	1.6	128.0
0.85	38.1	203.6	1.7	140.3	1.1	127.9

Table 1 – Mutual and self capacitances (all in pF/m) calculated for W=0.8 micrometers

W	Sakurai		Eecircle		Serenade	
(um)	C_{12}	C_{20}	Cm	Cp	Cm	Cp
0.70	40.6	188.6	1.9	127.8	1.0	115.0
0.75	40.8	195.3	1.9	134.1	1.1	121.6
0.80	41.0	202.0	2.0	140.3	1.3	127.9
0.85	41.2	208.7	2.0	146.5	1.4	134.2

Table 2 – Mutual and self capacitances (all in pF/m) calculated for S=0.8 micrometers

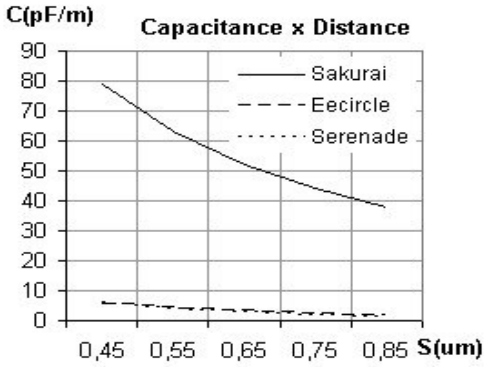

Fig. 3 – Mutual capacitances for W=0.8 micrometers

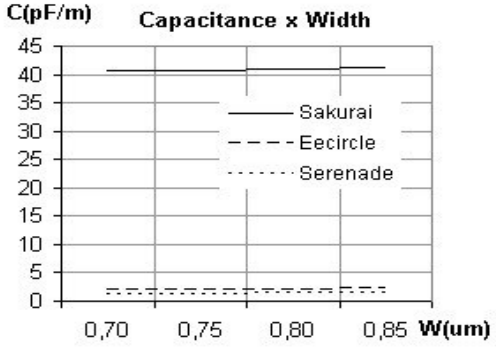

Fig. 4 – Mutual capacitances for S=0.8 micrometers

4. CONCLUSION

The EMC parameters extractor software is a first approach to the CAD program that will be developed to improve the design of integrated circuits. Efforts have been done to improve the software functionalities in order to accept layouts designed by others CAD tools as input files, using them as sources to calculate the EMC parameters according to their geometry.

The difference between the mutual capacitances calculated using Sakurai's formulas [4] and the results of Eecircle [5] varies from 92.6% to 95.5%. The difference varies from 92.5% to 97.5% when compared to the results of *Serenade*. Further studies will be done to compare more models and to include more mathematical algorithms for the calculus of capacitive and inductive coupling between the lines.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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