A RAPID PROTOTYPING METHODOLOGY FOR EMBEDDED SYSTEMS DESIGN

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ABSTRACT

In recent years there has been a growing need for design methodologies that can reduce the "time-to-market" of embedded systems designs. In this way, the development and the use of new tools for specification, synthesis and verification is essential to help designers to save time into their conception. In this paper, the focus is the use a "top-down" design workflow that goes from the high-level description of the system, based on SystemC, to its physical implementation on a reconfigurable platform. An example, elevator's control unit, and the synthesis results are presented.

1. INTRODUCTION

With the increasing in the complexity and size of the embedded systems, more powerful CAD (Computer Aided Design) tools are needed to speed up their design processes and consequently the prototyping. From high-level description to prototyping, a lot of new techniques have been suggested, since new description languages [3, 4], to synthesis and validation tools [7, 8, 10]. The main focus of this work is to show one of these possible design flows based on a top-down approach from SystemC to prototyping.

SystemC consists in a collection of C++ libraries that permit us to create models of various embedded systems features, including the hardware architecture, system interfaces, and software algorithms, among others. By using SystemC it is possible to create an "executable" specification the system's behavior, which can be tested, validated and optimized. After that, the code is then refined into a VHDL (Very High Speed Integrated Circuit HDL) RTL code. So, at this stage, a concise representation of the different abstraction levels is generated. Finally, the system can be synthesized and prototyped in a target technology.

In this work, a top-down design flow approach is presented aiming the development of an application, a digital elevator controller, from its specification and preliminary analyses in SystemC, VHDL synthesis, to its rapid prototyping on an Altera Flex10K20 FPGA family platform.

In section 2, a methodology overview is presented. Sections 3 and 4 present results and conclusions respectively.

2. METHODOLOGY OVERVIEW

In order to provide a new system from the scratch, a design team has, besides the proper will of each teammate, to know the complete design process and each of its phases' available tools and concepts, in order to offer a fully functional system model that satisfy the design constraints and its time-to-market.

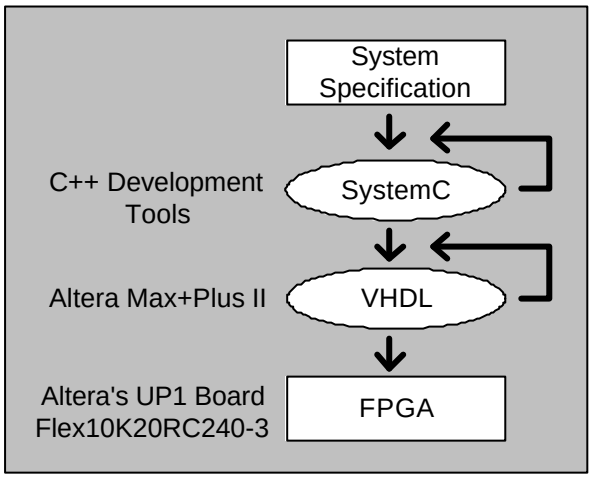
Considering the above approach, the functionality of the system is described using SystemC 2.0. Using this powerful C++ library, we are able to perform an ongoing refining process on this "executable version" behavior specification of the system using conventional C++ development tools such as the well-known compiler GCC. By doing so, each optimization had to be carefully tested in order to ensure the maintenance of the system's expected behavior, so it was required several waveform analyses using GTKWave [9]. SystemC played a fundamental key role in the optimization process because we could verify the correctness of the system algorithm without any need to worry about physical details such as the system clock or debounce mechanisms.

After the SystemC high-level description was validated, a manual parsing to a VHDL RTL model is performed. By doing this, obviously, we could not use the advantages observed in high-level languages and should, as well, involve several aspects directly connected to hardware. It is also needed the inclusion of some additional circuits that would be required the proper operation of the system when implemented in the prototyping board, such as a frequency converter and the debouncing circuit.

Like the SystemC model, this one had to be verified to check if its observed behavior was compatible with the desired one. For verification purposes it was used the waveform editor present in Altera Corporation's CAD tool, Max+PlusII [10]. Optimization, at this stage, required a more notorious effort among the development team in order to maintain the consistency between the VHDL and the SystemC model, which needed to be reviewed every time the VHDL model changed.

The latest stage of the methodology consists on the technological mapping (physical design) of the module itself. To achieve that artifact it was used the Max+PlusII FPGA features that provide a consistent environment in witch the VHDL model could be implemented into Altera Corporation's UP1 Prototyping Board [6]. This board contains an Altera's FPGA model EPF10K20RC240-3, of the Flex10K20 device family.

The methodology we referred above is summarized in the following picture:



3. EXAMPLE

In order to test the adopted methodology, a prototype of a commercial elevator's control unit was developed. This prototype is capable of answering calls from four different floors, and it has a 7-segment display to indicate the current floor. In each floor, there is a button to call the elevator and a LED to indicate whether the elevator is going up or down. The mechanic element responsible for the elevator movement is a step motor trigged with correspondent exit signal. There is also a magnetic sensor present in every floor to indicate when the elevator is stopped in the floor in question.

For this example, the differences between each implementation of the system are notorious. The SystemC model is written in approximately 600 lines of code and the VHDL model has about 900.

The physical implementation in the FPGA target technology resulted in approximately 220 logic elements. Externally, it uses the same clock frequency of the UP1 board, 25 MHz, which is then converted internally to the actual elevator's control unit clock, which is about 100 Hz.

4. CONCLUSIONS

A rapid prototyping methodology for embedded system has been presented. This works shows how easy is the development of such systems in a top-down design methodology approach, from a high-level specification language to its prototyping in a reconfigurable platform. Based on C++ libraries and GTKWave, SystemC environment design has shown be very efficient during the specification and system analysis before synthesis, taking advantages of software engineering optimization and simulation techniques respectively. A successful example has been presented. The design flow, from SystemC, to a refined VHDL synthesized code and its mapping on a Flex10K20 device has been successfully used.

More powerful examples are under development, and also the use of more reliable tools for analysis such Modelsim [7] and Testbuilder [8]. Such tools, integrated to SystemC will allow the development of new and more complex designs.

5. REFERENCES

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