ELECTRICAL CHARACTERIZATION OF SOI MOSFET AT HIGH TEMPERATURE

Carolina Davanzzo Gomes dos Santos [1], João Antonio Martino[2] and Marcelo Antonio Pavanello[3]
Laboratório de Sistemas Integráveis - Escola Politécnica da Universidade de São Paulo
email: [1] carolina@lsi.usp.br , [2] martino@lsi.usp.br , [3] pavanel@lsi.usp.br

Abstract – Electrical measurements were performed using a L-array transistor as a function of temperature from 300K to 550K. Threshold voltage (V_t), maximum transconductance (gm_{max}), maximum mobility (μ_{max}), subthreshold slope (S), and zero temperature coefficient (V_{ZTC}) were extracted from experimental results and compared to the literature models.

1. INTRODUCTION

High temperatures electronics is presents in a large field of applications, such as in automotive, aviation, and aerospace industries. The SOI MOSFET operation in high temperatures has been extensively studied in the past few years and the advantages over the bulk counterpart are remarkable: lower threshold voltage shift (V_t) (variation is 2 to 3 times lower) and 3 to 4 order of magnitude lower junction leakage current. [2]

Electrical measurements in SOI MOSFETs with several channel lengths (L=1µm, 1.5µm, 2µm, 3µm, 5µm, 10µm and 20µm) were performed in the temperature range of 300K to 550K. The used measurement setup consists of a Variable Temperature Micro Probe System, K20 model of MMR Technologies and a HP-4156 semiconductor parameter analyzer.

2. EXPERIMENTAL RESULTS

Several electrical measurements were performed using a L-array of transistors with constant channel width (W) of 20µm, silicon thickness (t_{Si}) of 80nm, buried oxide thickness (t_{ox}) of 390nm and gate buried oxide (t_{oxf}) of 30nm.

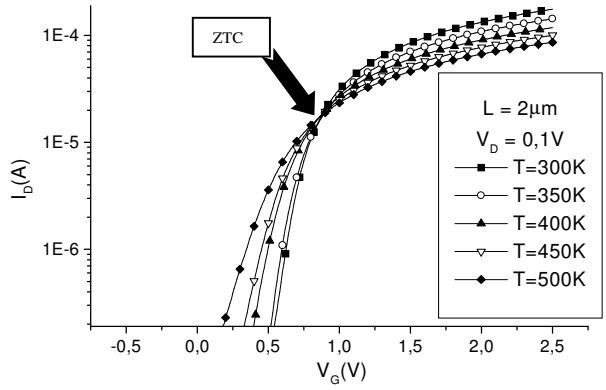

Figure1: I_D x V_G curve with V_D= 0,1V and L = 2µm

From the drain current (I_D) x front gate voltage (V_G) curves threshold voltage (V_t), maximum transconductance (gm_{max}), maximum mobility (μ_{max}), Subthreshold voltage (S) and zero temperature coefficient (V_{ZTC}) were extracted.

In I_D x V_G curve (Figure 1) was observed for all channel length that in subthreshold regime, the drain current (I_D) increases while temperature increases due to diffusion current. But after subthreshold regime while temperature increases, drain current decreases, due to mobility degradation at high temperature.

The transconductance gm (Figure 2), is a measure of effectiveness of drain current control by gate voltage. This was extracted from the first derivative of I_D xV_G curve. It was observed that while temperature increases, gm decreases, due to direct relation with mobility of carriers that decreases with the temperature increase. This behavior is expected as show in equation (1)

$$gm = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_D \qquad (1)$$

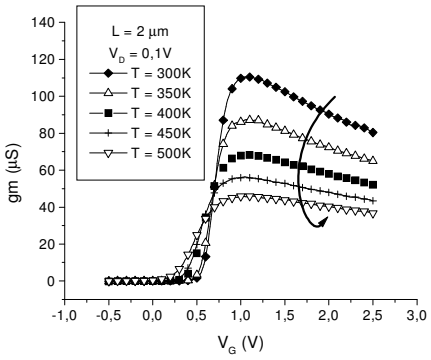

Figure 2: gm x V_G curve varying temperature

The degradation of mobility at high temperature occurs due to the larger crystalline lattice vibration, due to minority carriers shock.[1]. This degradation is shown in Figure 3. The maximum mobility has been extracted from the maximum transconductance in figure 2.

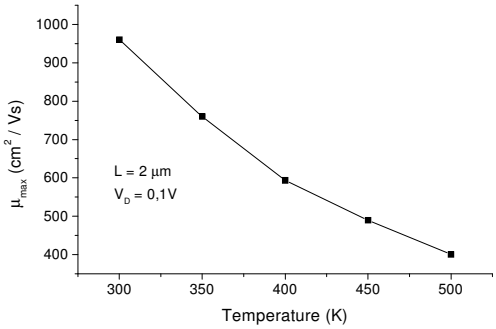

Figure 3: μ_{max} x Temperature curve

The threshold voltage (V_t) (Figure 4) is extracted through maximum peak of second derivative of I_D xV_G curve [3]. As expected, the threshold voltage (V_t) decreases when temperature increases. This fact occurs due to the intrinsic carrier concentration increase and the resulting Fermi level decrease.

The figure 4 also shows the subthreshold slope in function of temperature. It is observed that subthreshold slope (S) increases while temperature rises due to diffusion current and due to the direct temperature influence, as is shown in equation 2.

$$S = \frac{kT}{q}\ln(10).(1+\alpha) \qquad (2)$$

where: α is the net capacitance ratio in the fully depleted SOI MOSFET.

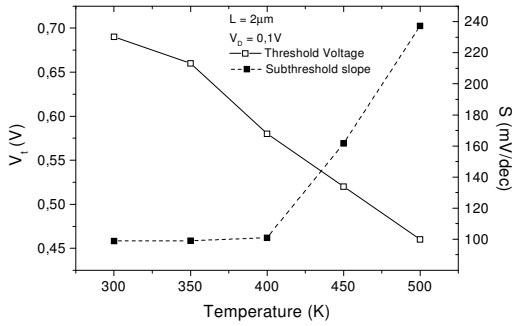

Figure 4: Threshold voltage and Subthreshold slope in function of Temperature curve

Figure 5 shows the drain current (I_D) in function of gate voltage (V_G) varying temperature. The drain current decreases while temperature increases. It was observed that in 550K there was a lower breakdown voltage, in this moment the fully depleted device becames partially depleted above a critic temperature, (T_K) that is aproximately 514K and the transistor behaves similarly to the bulk one.

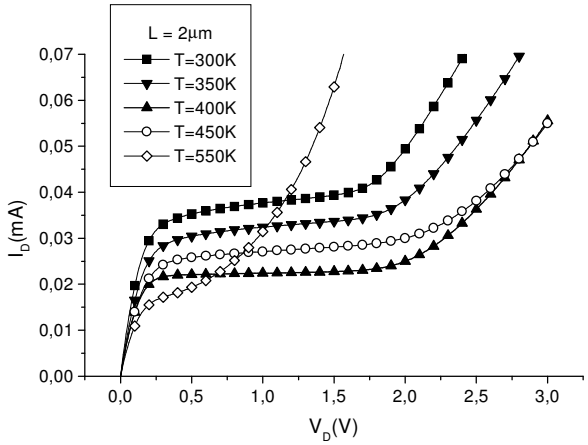

Figure 5: Drain curent (I_D) in function of drain voltage (V_D)

3. CHANNEL LENGTH REDUCTION INFLUENCE

The Zero Temperature Coeficiente (ZTC) (Figure 6) is the point on I_D x V_G curve (Figure 1) where for any temperature, the drain current is the same for each L-array device.

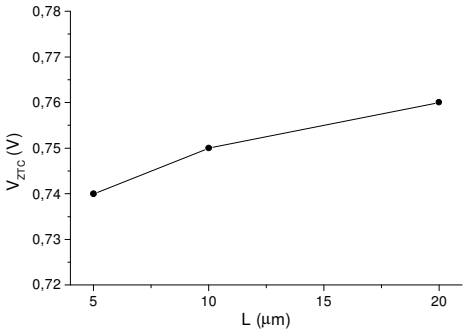

Figure 6: V_{ZTC} x L curve

Analising the dependence of V_{ZTC} with the increase of channel length was observed an increase of 20 mV for longer channel length.

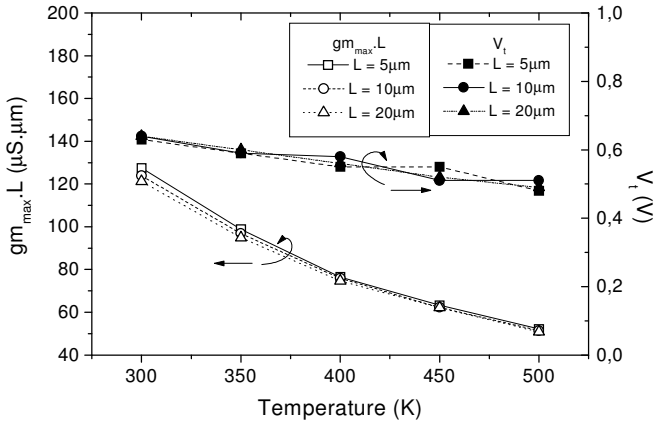

Figure 7: Maximum transcoductance and Threshold voltage in function of temperature varying channel length.

Figure 7 shows the maximum transconductance (gm_{max}) and threshold voltage (V_t) in function of temperature varying channel length. In this curve was observed that maximum transconductance decreases while channel length increases.

4. CONCLUSION

Electrical measurements of a L-array transistor SOI nMOSFET at high temperatures were used to study some electrical parameters such as threshold voltage, transconductance, subthreshold slope, maximum mobility and zero temperature coefficient.

It is observed that threshold voltage reduces due to the Fermi potencial decrease, the transconductance decreases with temperature due to its dependence with mobility that decreases due to the larger crystalline vibration, the subthreshold slope increases due to large diffusion current.

Analising these parameters was possible to verify that all of results were coerent with literature models.

5. REFERENCES

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6. ACKNOWLEDGEMENTS

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