Embedded Systems Power Estimation and Calculation Using SystemC

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Abstract

The estimation of the power consumed by embedded systems in early stages of the design becomes hugely necessary. Especially in portable systems, where the designer needs to estimate and maximize the battery lifetime. Traditionally the design flows wait more accurate models of the embedded systems to evaluate the power consumption. This paper presents a component library described in SystemC hardware description language using power consumption evaluation techniques. The utilization of SystemC language using the methodology presented makes it possible to estimate the power consumption very early at the beginning of the simulation and verification of the system description and functionality.

1. Introduction

The sprouting of hardware description languages allowed to describe and simulate entire systems providing higher productivity to the designers' teams. This additional productivity allowed these same teams to add, still in the initial phases of the project, concerns that go beyond the simple correction of the described system.

For some systems, the requirement goes beyond the traditional commitments between cost and performance. In embedded systems the consumed power needs to be always the lowest possible. Therefore, having the knowledge of how much power the system consumes, or even which parts of the system are the major responsible for this consumption, can be essential for the development of new solutions of better performance in the phase of project space's exploration.

This work presents a set of descriptions of SystemC components capable to estimate the power consumed in a cycle. For that some techniques already used by some simulators are applied [1].

This paper is organized in 5 sections. In section 2 is presented one brief motivation for the power consumption estimation from high level descriptions of the projects. Section 3 presents the techniques used for measurement of the power in components. Finally in section 4 the final conclusions.

2. Power Calculation

With the embedded systems increasing popularity, the estimation of system power consumption is becoming more common in hardware's projects of this category [2] [3] [4]. Even when this study is made before the implementation, it allows the designer to evaluate the expense of the power of its system since the beginning of the project.

Many ways and techniques already had been presented to extract the power consumption in the beginning of the project cycle, as in [5] and [6]. There are techniques that congregate parts of each solution as the CACO-PS simulator (Cycle-Accurate COnfigurable Power Simulator) [1], that calculates the power consumption in each described component with the aid of a table of in and out signals history.

3. Power Calculation Techniques in SystemC

The motivation for the execution of this work came from the perception that the techniques for power consumption estimation described in [1] could advantageously be used in descriptions using the SystemC language. In this section is presented the application of the techniques used for the CACO-PS in a SystemC description.

As SystemC already does accurate simulations cycle-by-cycle, the effort was focused on the application of the techniques presented in [1], for the development of a components library, allowing the power calculation in any description level.

In the synchronous components the power calculation is made through the verification of the input bits in each cycle. The current input value and the previous input value are compared [1]. However the input bits switched is not the only condition that makes a component to consume power. A register, for example, consumes power

in others two situations [1]: static consumption only because it is in the architecture and enable bit switching. The designer must then describe the consumption of each component in a power calculation function that also must be enclosed in the component SystemC description.

In the asynchronous components, that do not possess clock signal, these components' outputs are calculated using the inputs sensitivity method available in SystemC. If the power was also calculated this way, it would not have called the power calculation method when the inputs remained unchanged. So the variable that accumulates the simulated consumed power cannot be initialized, making the power consumption calculation inaccurate.

The solution was to encapsulate the asynchronous components in a higher component with a clock input. In these components the clock input is used for the power consumption calculation. In this way the calculation function remains sensible to the clock transition and, as the register, to keep the value of the previous input. So, the input values changes are verified all cycles.

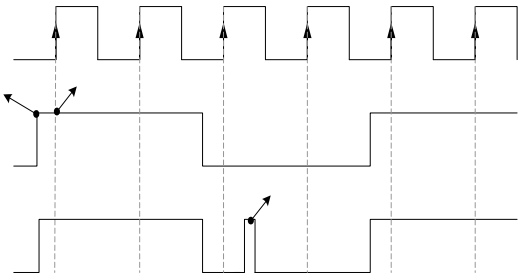

Figure 1. Invertor waves graph

The Figure 1 shows the bit switching verification in the clock transitions, where a clock signal and a input signal (In A) represents the input of an inverting logical gate. It is verified that in the moment **m1** the In A signal changed from one to zero, immediately (using the input sensitivity) is attributed to the output logical gate the negation of this value. In the moment **m2** occurs the positive clock transition, and in this moment the power function is invoked and, from the comparison between the input values in the current cycle and in the previous cycle, it is calculated how many bits had been modified. Later the variable that represents the input value in the previous cycle is updated. The written process continues until there are no more inputs, or cycles. In the case of the moment **m3** occurs a fast alteration of the input that immediately returns to its previous value (known as glitch), before the next clock transition. When the clock transition occurs, the values that will be compared are equal, not having the possibility to consider the power consumed in these cases.

4. Conclusions

This paper presented the implementation of a power calculation methodology of the power consumption of a device, circuit or embedded system from its description in SystemC language. Allowing the formation of a components library that can calculate the power of the described architecture.

To validate the methodology usage of the chosen language, case-studies were tested in simple architectures and later in an elaborated architecture. So the power calculation techniques implementation could be validated. Is needed to be notice that this paper did not present the case-studies in details because of space limitations.

The final results in the case-studies showed that the methodology presented in [1] can be applied the simulation in SystemC. The use of this language guarantees to the designer the use of only one language for description, simulation with power consumption calculation and synthesis.

5. References

[1] Beck F., A.C.S., Mattos, J.C.B., Rosa J., L.S., Wagner, F.R. e Carro, L. (2003). "CACO-PS: um avaliador de potência". In Seminário Integrado de Software e Hardware (SEMISH)

[2] Carro, L., Corrêa, L., Cardozo, R., Moraes, F. e Bampi, S. (2003). "Exploiting reconfigurability for lowpower control of embedded processors". In IEEE International Symposium on Circuits and Systems (ISCAS)

[3] Gervini, A. I., Corrêa, E. F., Carro, L. e Wagner, F. R. (2003). "Avaliação de Desempenho, Área e Potência de Mecanismos de Comunicação em Sistemas Embarcados". In XXX Seminário Integrado de Software e Hardware (SEMISH)

[4] Shiue, W.-T. e Chakrabarti, C. (1999). "Memory Exploration for Low Power, Embedded Systems". In IEEE International Symposium on Circuits & Systems (ISCAS).

[5] Tiwari, V., Malik, S. e Wolfe, A. (1994). "Power Analysis of Embedded Software: a First Step Towards Software Power Minimization". IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol. 2, No. 4, pp 437-445.

[6] Simunié, T., Benini, L. e De Micheli, G. (1999). "Cycle-Accurate Simulation of Energy Comsumption in Embedded Systems". In ACM Transaction on Design Automation Conference (DAC)