CHARACTERIZATION OF A NMOS EMC TEST CHIP

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ABSTRACT

The subject of this work is the test and measurement of an integrated circuit originally developed to evaluate Electromagnetic Compatibility. The chip was fabricated with nMOS technology at CCS-Unicamp.

1. INTRODUCTION

The work described in this paper is part of the development process of a large System-on-Chip (SoC), including microprocessors, memories, RF structures and others. The SoC design is part of the SCMN Millenium Institute Project. This project started in 2001 [1] as part of the practical activities of the Electronics undergraduate course at Universidade de Brasília. The design was completed and sent to fabrication in 2002. The integrated circuit was fabricated in 2003 and is under characterization now by another group of undergraduate students.

The purpose of the system was to study Electromagnetic Compatibility (EMC) and Electromagnetic Interference (EMI) phenomena inside an integrated circuit. The study is intended to identify the means to optimize EMC and minimize EMI inside the chip.

2. THE INTEGRATED CIRCUIT

The integrated circuit contains several functional blocks, digital and analog, built around two high-frequency oscillators that work as a noise source. In this way, it was expected to maximize the interference caused by the oscillators on the other circuit blocks. The electrical simulations of the circuit was done using a SPICE based circuit simulator while the layout was edited using the LASI tool. The technology is a 5 µm nMOS from CCS-Unicamp [2].

The final layout is shown in Figure 1. The functional blocks are numerated from 1 to 10 according to the list below. In order to drive the input impedance of an oscilloscope, buffer circuits are connected to the output of each block.

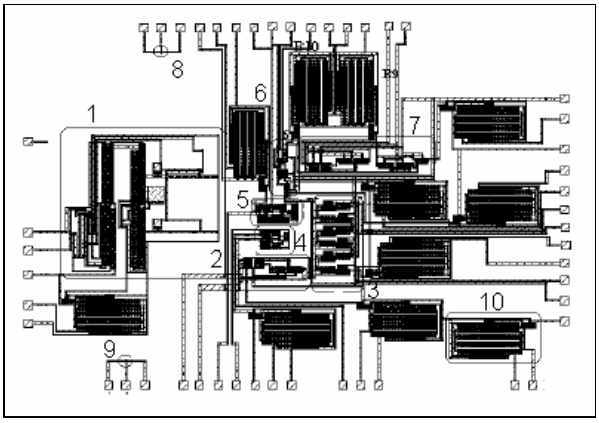

Figure 1 – Integrated circuit final layout with identified functional blocks

1. Operational Amplifier
2. XOR gate
3. 3-stage Shift Register
4. L = 7 µm Oscillator
5. L = 5 µm Oscillator
6. NAND, NOT and NOR gates
7. 1-bit Adder
8. Isolated Enhancement Transistor
9. Isolated Depletion Transistor
10. Isolated Buffer

3. THE MEASUREMENT PROCEDURE

The test of the integrated circuit shown in Figure 1 was initialized by the static characteristic of both isolated enhancement and isolated depletion transistors. Due to a variation on the fabrication process the transistors had an offset on their threshold voltage (Vt) value. To correct the Vt value a substrate voltage (Vsub) of 10 V was applied. The test equipments available are one function generator HP3310A, one oscilloscope HP54600A and two variable laboratory DC power supply. The oscilloscopes graphs are saved in the computer using the HP BenchLink Software.

The measurement setup that was used to plot a Ids x Vds characteristic can be viewed in Figure 2. The current Ids is obtained by measuring the voltage drop across Re

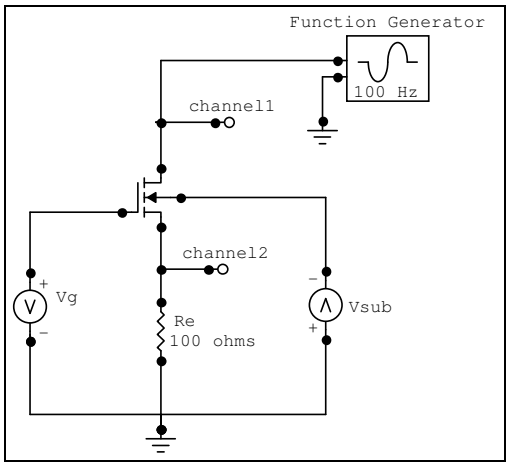

Figure 2 - The measurement configuration for a transistor

(oscilloscope's channel 2) and dividing it by Re. The oscilloscope's channel 1 measures Vds, assuming that the voltage drop across Re is small compared to Vds. Utilizing the plot XY function of the oscilloscope it is possible to plot the channel 1 in the X axis and channel 2 in the Y axis. To vary Vds from 0 V to 5 V a function generator was used. The gate voltage (Vg) was manually changed from 0 V to 5 V in 1V steps. The resulting Ids x Vds characteristic for the enhancement transistor is shown in Figure 3.

The Ids x Vgs was plotted connecting the function generator to the gate of the transistor and connecting the variable DC source to its drain. For this setup the oscilloscope's channel 1 should be connected to the gate terminal. The function generator was set to a ramp from – 2 V to 3 V and the drain voltage was kept in 3 V. The resulting characteristic Ids x Vgs for the enhancement transistor is shown in Figure 4. The results measured for both characteristic agree with the tests previously carried out at Unicamp.

4. CONCLUSIONS

The development of this Electromagnetic Compatibility project has an important impact on the undergraduate student formation on microelectronics at Universidade de Brasília. Up to this moment, basic static characteristics were obtained and a complete static and dynamic characteristic of the whole chip is expected in the near future.

5. ACKNOWLEDGMENTS

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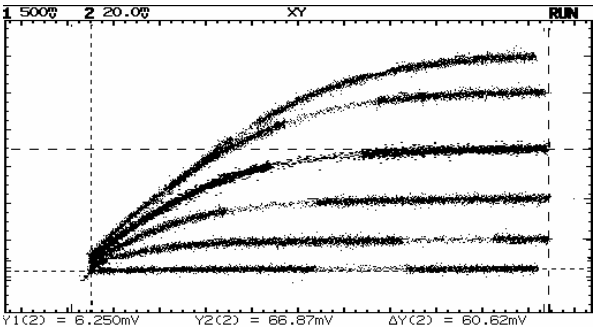

Figure 3 - Ids x Vds characteristic of the enhancement transistor

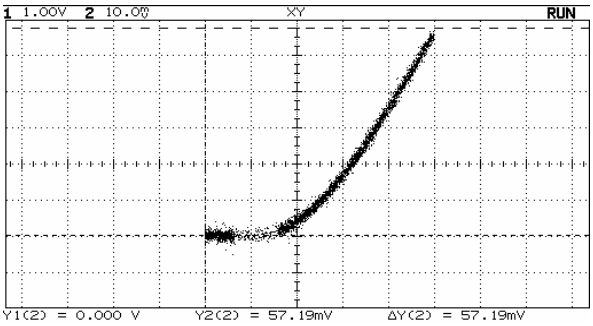

Figure 4 - Ids x Vgs characteristic of the enhancement transistor

6. REFERENCES

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