A Test Chip for Analog Blocks in VLSI CMOS

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Abstract

The design of an analog circuit depends on several factors such as good device modeling and technology characterization. In this context, in order to validate the design methodology and the electrical models of a target technology, electrical characterizations based on measurements are necessary. This paper addresses the development of a test chip with several designed blocks and test vehicles. The chip was implemented in 0.35µm CMOS technology, using the CADENCE environment.

1. Introduction

The development of ultra-scaled VLSI technologies, coupled with the demand for more signal processing integrated in a single chip, has set the trend for integrating analog circuits below 0.13um digital CMOS. Systems-on-chip integration requires analog sub-systems such as amplifiers, comparators, filters, oscillators, digital-to-analog and analog-to-digital converters to be designed with standard digital CMOS.

Several analog basic circuit blocks were designed using two different design methodologies: a full-custom design methodology based on the g_m/I_D characteristics [1]; and design methodology based in a pre-diffused transistor array [2]. In the first experimental results, the technology characteristics and circuits performance were obtained with Spectre simulations using the foundry-supplied typical BSIM3v3 model parameters for the target technology AMS0.35um CMOS technology. The methodologies were validated with electrical simulations (schematic and post-layout) for all blocks, including Monte Carlo simulations.

However, in order to validate the design methodology and the electrical models, electrical characterizations based on measurements are necessary. We sent to fabrication a test chip with the designed blocks and test vehicles in AMS0.35µm technology. The goal is to perform characterization and modeling optimization through electrical measurements to fine tune the basic design curves and validate the blocks performance.

2. Test Chip Structures

Several analog basic circuits were designed using different design methodologies. A test chip with the designed blocks and test vehicles in AMS0.35µm technology was developed to characterize and model the design through electrical measurements. Each block that composes the test chip is briefly described in the following sections.

2.1. Bandgap Reference

A bandgap reference architecture was implemented in 0.35µm CMOS technology [3]. The circuit generates a stable 1.223V voltage reference with a low, 40ppm/ºC temperature coefficient. It can operate with supply voltages in the 2.3 to 3.3V range and between -50ºC and 150ºC.

2.2. Miller OTA

A Miller Operational Transconductor Amplifier (OTA), a two-stage operational amplifier with a feedback capacitor, was design using different design methodologies.

The first full-custom version of the circuit design is based on the g_m/I_D characteristics [1], where the transistors lengths L are considered 5 times the minimum-length allowed by the technology. The second full-custom version of the circuit design has an additional optimization in the design phase: choosing the transistor lengths (L) to minimize power [4]. A TAT version of the Miller OTA based on the full-custom design with fixed transistor lengths L (full-custom version 1). Following, each single transistor of the circuit is substituted by an equivalent TAT. Using the LIT tool [2] for the synthesis, each single transistor can have more than one equivalent association. Several associations in test structures will be characterized with this test chip.

2.3. Comparator

A track-and-latch analog comparator was implemented in 0.35µm CMOS technology in both full-custom and TAT versions [1]. The design optimizes both the speed and the power consumption, as long as reasonable sensitivity and gain are achieved. Once the design operating frequency is reached, the power consumption is set by the current Itail [1].

2.4. Gm-C Filter

A fully-differential continuous-time Gm-C band-pass filter with a biquad circuit topology was designed an included in the test chip[1]. This topology was selected to provide a simple structure that demonstrated the capabilities of the

technology and the transconductor design methodology. The design procedure followed the method developed in [1]. Simulation results shows that the center frequency has a range of operation from 4.5MHz and 5MHz while the simulated filter quality factor is about 250.

2.5. Test Structures

Several test structures were designed in order to allow the extraction of the transistors parameters applicable to all operation regions and all device sizes.

The test structures inside the test chip include long, wide, short and narrow channel transistors. New geometries are also present, such as series-parallel associations of transistors of different sizes and shapes. The trapezoidal and T-shaped associations were designed for model evaluation. These structures will be used to characterize the behavior of the drain current, gate transconductance, output conductance, noise, matching and intrinsic frequency in terms of geometry, association of unit transistors and layout strategies. For the measurement of mismatch, the test chip includes a few current mirrors composed by different associations of regularly-sized transistors. The test structures will be measured through microprobes, and smaller micro-pads were included to access the structures terminal and to save test chip area.

3. Test Chip Overview

The test chip with the designed blocks and test vehicles was designed in AMS0.35µm technology. Table 1 gives an overview of all blocks that compose the test chip, including the PADs (which were obtained from the foundry library).

Table 1 - Blocks that composes the test chip.

	Block	Area (µm²)	PADs	µPADs
1	Miller OTA Ver. 1	83 x 119	5	-
2	Comparator	41 x 70	7	-
3	OTA	56 x 82	8	-
4	GM-C Filter	90x70	9	-
5	Miller OTA TAT – Ver. 1	77 x 198	5	-
6	Comparator TAT	93 x 108	7	-
7	Miller OTA Ver. 2	90 x 125	5	-
8	Ring Oscillator	29 x 165	3	-
9	Test Structures	1100 x 1150	-	84
10	Band-gap	300 x 400	8	-
	PAD	95x340	-	-
	µPAD	90x90	-	-
	Total	**2134 x 2134 (4,55 mm²)**	56	84

Figure 1 shows the complete layout of the proposed chip test. The full-custom layout was implemented in Cadence CAD environment, and all modules fitted to 4,55 mm^2 total area.

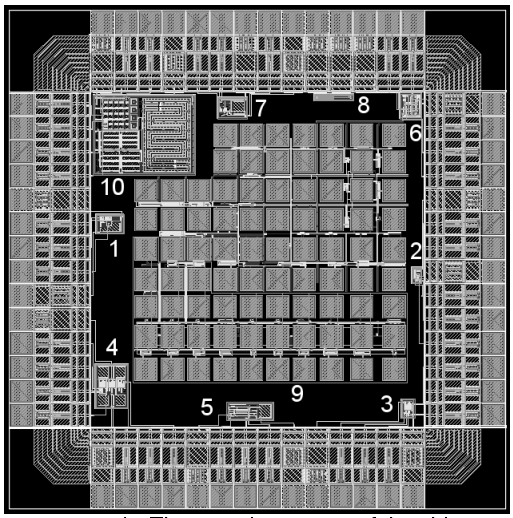

Figure 1 - The complete layout of the chip.

4. Conclusions

Electrical characterizations based on measurements are indispensable for the complete validation of an analog integrated circuit. Test chips measurements are expected after CMP-provided silicon prototyping. This paper presented a test chip with the designed blocks and test vehicles in AMS0.35µm technology.

Future work includes characterization and modeling optimization through electrical measurements to validate electrical performance of each block. Test structures include trapezoidal, square and T-shaped transistor associations for modeling work.

5. References

[1] PAIXÃO CORTES, F.; FABRIS, E.; BAMPI, S. *Applying the g_m/I_D Method in the Analysis and Design of a Miller Amplifier, a Comparator and a Gm-C Band-Pass Filter*. IFIP VLSI Soc 2003, Darmstadt, Germany, December 2003.

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