An Analog Test Chip for Device Modeling and Characterization

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Abstract

The design of an analog circuit depends on several factors such as good device modeling and technology characterization. In this context, in order to validate the design methodology and the electrical models of a target technology, electrical characterizations based on measurements are necessary. This paper addresses the development of a test chip with several designed blocks and test vehicles. The chip was prototyped in AMS 0.35μm CMOS technology. Preliminary measurements of the designed blocks and test vehicles are presented.

1. Introduction

The development of ultra-scaled VLSI technologies, coupled with the demand for more signal processing integrated in a single chip, has set the trend for integrating analog circuits in below 0.13um digital CMOS.

Several analog basic circuit blocks were designed using two different design methodologies: a full-custom design methodology based on the g_m/I_D characteristics [1]; and a design methodology based in a pre-diffused transistor array [2]. In the first results, the technology characteristics and circuits performance were obtained with electrical simulations using the foundry-supplied typical BSIM3v3 model parameters for the target technology AMS0.35um CMOS.

However, in order to validate the design methodology and the electrical models, electrical characterizations based on measurements are necessary. A test chip was prototyped in AMS 0.35µm CMOS technology. The objective here is to use the electrical measurements to perform characterization and modeling optimization to fine tune the basic design curves and validate the performance of the blocks.

2. Test Chip Structures

A test chip with the designed blocks and test vehicles in AMS0.35µm CMOS technology was developed to characterize and model the design through electrical measurements. Each block that composes the test chip is briefly described as follows.

There are 9 analog building blocks implemented: a Miller Operational Transconductance Amplifier (OTA) and a track-and-latch comparator (using different design methodologies, one based on the g_m/I_D characteristics [1], and other using a pre-diffused transistor array [2]), a fully-differential continuous-time Gm-C band-pass filter with a biquad circuit topology [1], a Band-gap voltage reference [3], and a Ring Oscillator. All the design optimizes both the speed and the power consumption, as long as reasonable sensitivity and gain are achieved.

Several test structures were designed in order to allow the extraction of the transistor parameters applicable to all operation regions and all device sizes. The test structures inside the test chip include long, wide, short and narrow channel transistors. New geometries are also present, such as series-parallel associations of transistors (TAT or TST) of different sizes and shapes[4]. These structures will be used to characterize the behavior of the drain current, gate transconductance, output conductance, noise, matching and intrinsic frequency in terms of geometry, association of unit transistors and layout strategies. For the measurement of mismatch, we included some current mirrors composed by different associations of transistors. The test structures will be measured through microprobes, so we used micropads to access their terminals (the PADs, which were obtained from the AMS0.35um technology library).

Figure 1 shows the chip microphotography, with a total area of 4.55 mm². Most of the chip area is due to the micropads.

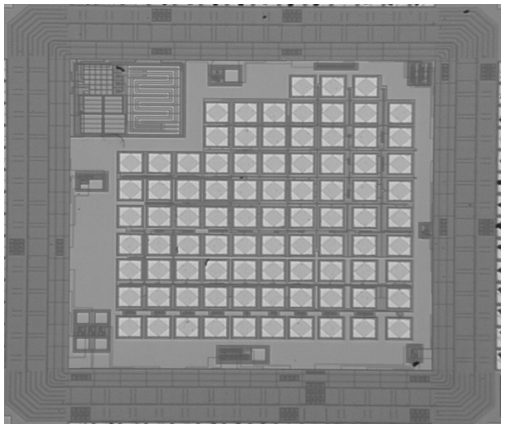

Figure 1 – Chip microphotography.

3. Test Characterization Procedure

The test and characterization procedure will follow two main steps. The first step is the characterization of the target process. Using a Parameter Analyzer combined to a Microprobe Station, the behavior of basic transistor

parameters can be obtained, such as measurements of *Id x Vd*, *Id x Vg* and *Id x Vs* curves

Therefore, the process in use can be fully characterized, and the parameters of CMOS simulation models (such as ACM, EKV models) can be obtained. This can be used to fine tune the basic design curves and validate performance of the designed blocks. Drain current, gate transconductance, output conductance, noise, matching, etc., can be obtained direct from the MOS transistors structures measurements. The maximum frequency for this target process can also be obtained, using the Ring Oscillator structure. Figure 2 shows some preliminary results for the MOS transistors characterization.

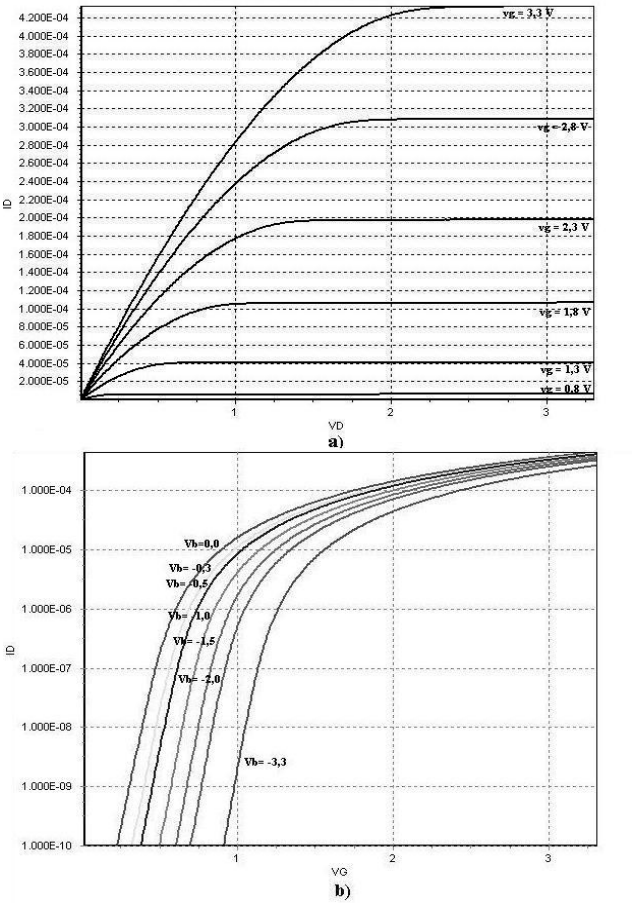

Figure 2 – (a) Id vs.Vd and (b) Id vs.Vg measured curves for NMOS (W=10 and L=10 µm)

The next step is the block validation. Each block should be fully characterized. Table 1 shows the measured performance obtained for the Miller OTA block. The parameters of the amplifier, like open loop gain, offset voltage and power consumption were obtained through measurement of five samples. We observed the agreement between measured, simulated and the desired performance specifications.

Table 1 – Miller amplifier performance

Parameters	Specs	Simulation	Measurements
GBW(Mhz)	15	14.6	10
Av (dB)	> 80	85.42	80.3
Offset(mV)	< 20	7.2	1.92
Settling Time(µs)	-	-	320.2
SR (V/us)	18	18	7.51
I_{DD} (µA)	325.5	339.4	282
CMRR(dB)	-	89.9	86.9
ICMR (V)	-0.5 to 1	-0.52 to1.45	-1.4 to 0.99
Vout range (V)	-	+0.9 to -1.4	+1 to -1.6

4. Conclusions and Future Work

Electrical characterizations based on measurements are fundamental for the complete analysis of an analog integrated circuit. Only measurements can determine the real circuit functionality.

The prototyped test chip is currently under testing, and preliminary measurements of the designed blocks and test vehicles were presented, showing good performance.

As future work, we intend to perform a fully characterization and modeling optimization through electrical measurements to fine tune the basic design curves and validate the blocks performance. In order to obtain more accurate results, new instruments are been added to our test setup, including digital oscilloscope, function generator, RF microprobe station and others.

Acknowledgements

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