A CMOS Switched-Current Cyclic A/D Converter for Irrigation Control Application System on Chip

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Abstract

A CMOS VLSI System on Chip, designed for Irrigation Control Applications was developed. This paper describes the project of an 8 bit cyclic ADC that will be integrated in the chip to realize the sensor signal acquisition feature.

1. Introduction

Our University, together with seven other institutions, is developing a system to control irrigation on crops [1]. The system is composed by a base station, field stations and nodes [2]. The field stations gather information from the nodes through a wireless link, accurately identify areas of moisture deficiency and send instructions to the nodes, determining which ones should act on latch solenoid valves, in order to deliver the required amount of water to the plants. Each node is composed by a CMOS 0.35µm [3] SoC (System on Chip), a tensiometer with a solid state pressure sensor, an actuator which controls the water flow through a solenoid valve, a solar powered power supply, a RF antenna, and embedded software. The SoC consists of a RISC microprocessor, memories, a RF transceiver, digital interface and A/D interface.

This paper presents an overview of the new A/D interface that will be integrated to the SoC on its next prototype phase. Based on the systems requirements, an 8 bit 250 kilo sample per second small-area and low-power A/D converter was specified. This paper describes the core circuitry that was used to achieve this goal. The paper outlines as follows. Section 2 gives a small description o the converter architecture and section 3 shows the proposed ADC architecture. Finally, section 4 presents the simulation results and conclusion.

2. Switched-Current Cyclic ADC Design

A class of low-impedance analog circuits wherein current rather than voltage is the primary signal medium is receiving considerable attention as an alternative to conventional high-impedance analog circuitry [4]. Such switched-current circuits can operate with low power supply voltage because of small voltage swings associated with low-impedance nodes.

In other to achieve the necessary resolution within a small silicon area, a RSD cyclic or algorithmic conversion was chosen over the other possible architectures.

The conventional cyclic conversion algorithm consists of the multiplication by two of the signals to be converted, followed by a comparison of the result with a reference voltage (current). If the signal is larger than the reference, the most significant bit (MSB) of the output code is set to 1, and the reference is subtracted from the signal; otherwise, the MSB is set to 0, and no arithmetical operation is carried out. The remaining part of the signal, the so-called residue voltage (current), corresponding to the partial remainder of the division, undergoes the same operation for the next bit decision and the loop is run until the least significant bit (LSB) is obtained. For the modified RSD cyclic conversion algorithm, two conversion levels are used. If the input signal, twice of the residue voltage (current), is larger than the higher level, the output code bits is set to 10 and the reference is subtracted; if it is smaller than the lower level, the output code is set to 01 and the reference is added; otherwise, the output code is set to 00 and no arithmetical operation is carried out. Several ADC's with switched-capacitor and switched-current techniques adopt this algorithm. The modified RSD conversion algorithm provides a large tolerance for the comparator's inaccuracy, thus higher levels of noise, error effects, and even hysteresis are allowed [5].

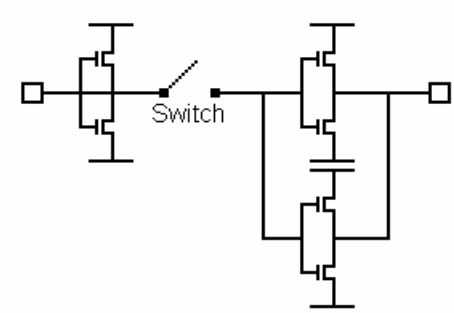

Figure 01 – Two Unity Gain Current Buffer Switched Current Cell

3. Proposed ADC Design

Based on the modified RSD cyclic ADC architecture a switched-current approach was proposed to realize the stages of the converter.

In order to generate the control signals a state machine based on a 4 bit counter was also designed. To receive the results of the converter's comparison a special RSD to two-complement shift register was designed too. Finally an output buffer interfaces directly with the microprocessor's registers.

To design the analog core of the converter, switched-current memory cells where used to execute the sample and hold function through out the converter cycles. In order to realize a precise multiplication by two, two unity gain current buffers where used and their results added. This detail of the circuit is shown in figure 01. High-swing cascaded current source and sink were used as positive and negative current references respectively which were added to the result of the multiplication based on the result of the output code of the comparator.

The comparator used current references exactly equal to the others described before, giving the comparator more precision. The comparisons were made against 3 times the residual current, resulting in 1/3 of the positive and negative current references to be the positive and negative levels of comparison. This way the three output codes are equally possible. The multiplication by three of the residual current was also made adding the output of three unity gain current buffers. The full design is presented in the schematic shown in figure 02.

This design results in two cycles per bit residual amplification and conversion and in 16 cycles for an 8 bit conversion. Each cycle consumes two clock periods, which in this SoC is 62.5 ns (16MHz). So, the converter reaches the 1 mega sample per second limit.

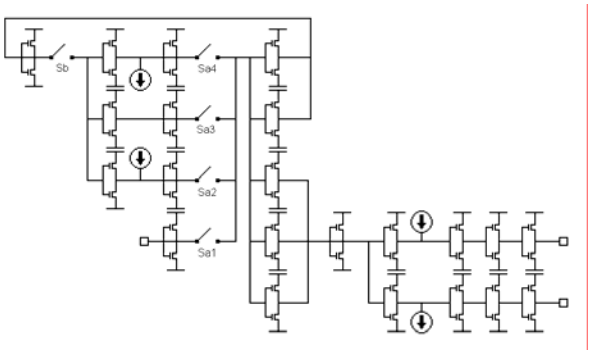

Figure 02 – Analog Circuitry

During the design a special attention was giving to the switching. CMOS switches were designed using minimum device dimensions. All cells were designed to 50ns switching period and were able to keep the necessary SNR. The design also tried to reduce the number of switches to eliminate most of the errors.

4. Conclusion

The proposed design has not been fully simulated yet. The digital part of the system was tested and worked as expected. The analog design simulation has encountered problems concerning the size of the capacitors, the quiescent current, and the linearity of the unity gain current cells. This decisions are been taken in order to guarantee the necessary speed and dynamic range. In the continuity of this project, the simulations will be finished and the layout phase will start. In this phase, the real area and power consumption will be determined. The author would like to acknowledge CAPES, CNPq, and PADCT/Millennium Institute (Brazilian government agencies) for financial support.

5. References

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